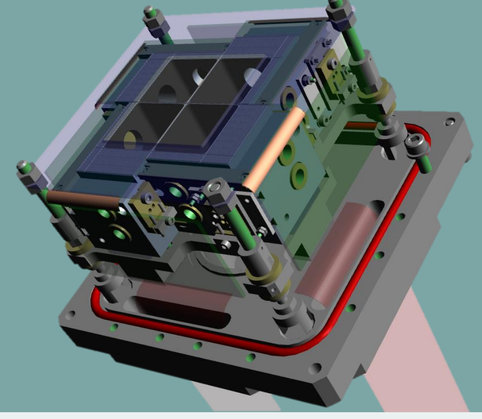
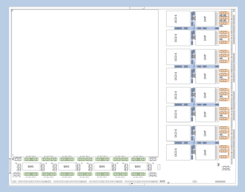
EDET80k DAQ. Front-end electronics.



ASM

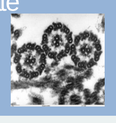
& gummy bears

- Matrix 512x512
- 4 x switcher footprints
- 8 x DCD footprints
- 8 x DHPT or pin to pin compatible DMC footprints
- Interconnections



DePFET matrix

- 4 independent tiles x 512 x 512 pixels = 1Mpixel FPA
- 80 kHz framerate (100 images burst)
- 100 Hz burst rate

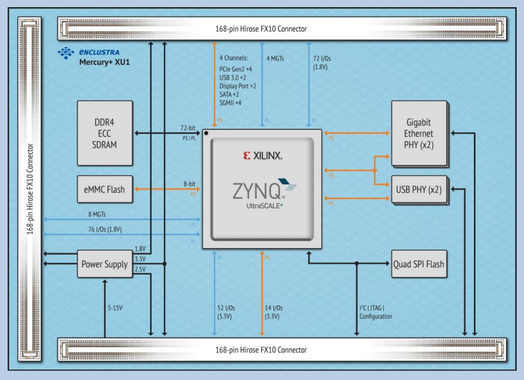


EDET80k

- 12.5 µs/frame resolution
- Stroboscopic illumination
- Dynamic effects analysis
- Biological and chemical reactions in motion observation

Hardware platform.

Xilinx® Zynq Ultrascale+™ MPSoC
ARM® quad-core Cortex™-A53
ARM dual-core Cortex™-R5
Mali-400MP2 GPU

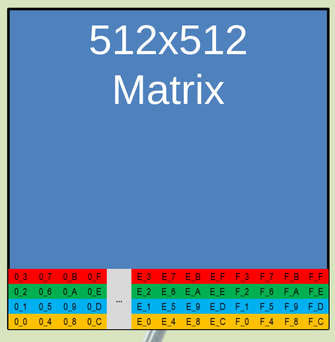


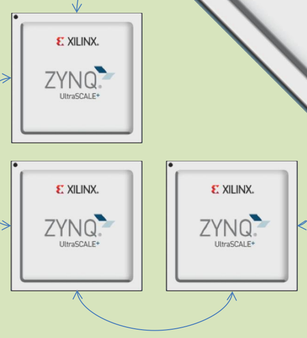
16nm FinFET+ FPGA fabric
2 GB DDR4 ECC SDRAM
64 MB QSPI flash
16 GB eMMC flash
16 × 15 Gbit/sec MGT
2 × Gigabit Ethernet
5 to 15V single supply
Small form factor (74 × 54 mm)

Glossary

ANN – artificial neural network
ASM – all-silicon module
CNN – convolutional neural network
DCD – drain current digitizer (ASIC)
DHP(T) – data handling processor (ASIC)
DMC – DePFET movie chip (ASIC)
EDET – electron detector
FPA – focal plane area
IML – inter-module link
MGT – multi-gigabit transceiver
PL – programmable logic
PM – power module
PS – processing system
SoC – system on a chip
TEM – transmittion electron microscopy

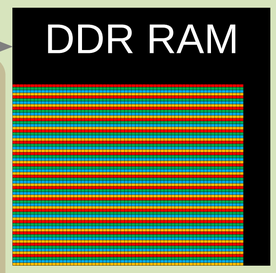
Firmware capabilities.





1. On-the-fly image stitching and buffering in RAM

The data coming from ASICs is sorted not in the right order and the firmware does stitching through the pipelined alogrithm, passing it via two ring buffers(per ASIC). One is registers-based buffer of 32 bytes and the second is internal SRAM-based of 8192 bytes. Such approach allows to avoid an additional bottleneck in terms of the data throughput, in the same time drastically reduces the amount of data preprocessing on the host and economizes the resources of the SoC. Allows reconfigurations within a user software, runinig in OS. Vivado HLS toolset was used to design, test and implement the scheme. Overall PL occupancy by the module is 4/2/10% RAM/FF/LUT.



Up to 1000 images can be buffered.

2. UDP/IP/MAC data framing.

The full stack of 10Gb/s Ethernet layers includes UDP CRC calculation, Jumbo packets transeiving feature and ARP embedded. Works independently in PL, configurable by user application from PS. Pure VHDL.

3. Two 10GBase-SR interfaces.

Stream movies to the storage system via two high-speed MGTs. Data source is selectable between image stitching scheme output and DDR RAM buffer. Payload rate 1,97 Gbytes/s* per tile.
* Measured by RTL simulation.

4. Inter-module link.

IML organized in ring topology offers the tool configuration and online monitoring data using one dedicated ethernet channel. Clock and trigger signals are distributed over additional dedicated lines.

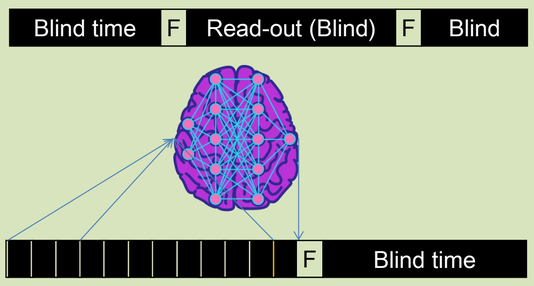
10G links connect each pair of SoCs.

5. Configuration and state logging.

Configuration of the device counts more than 5000 registers spread over 80 ASICs, 4 SoC PLs‘ modules, PM ICs and user software running on PS. Database structure is chosen to store and represent the configuration dataset. There are several datasets: a. actual configuration written to the places; b. replica of the actual configuration stored in DDR, where user changes the settings and which is compared with the actual one all the time; c. initial configuration saved in flash device, which allows to restore factory settings; d. mirrored data to be shown for the user. The tools used EPICs and CS Studio.

6. ANN-based trigger generator.

The trigger signal launches the electrons illumination and data readout procedure. In order to increase valuable data ratio and examinated object life length a smart signal is generated by ANN from the previous images data. ANN aims on the features valuable for the observer like an object shape, speed, interval and generate a signal which starts a full speed burst. Below the comparison of blind filming and smart trigger generation approaches.



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