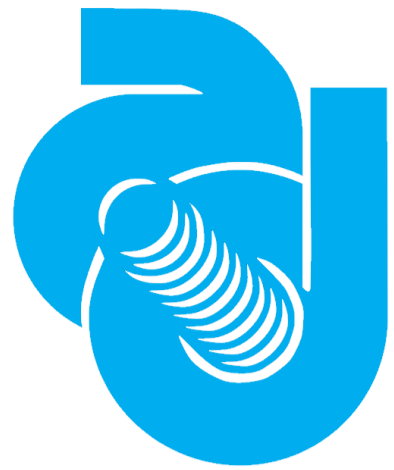


# Experimental Test and Characterization of "BASIC64", a New Mixed-Signal Front-End ASIC for SiPM Detectors



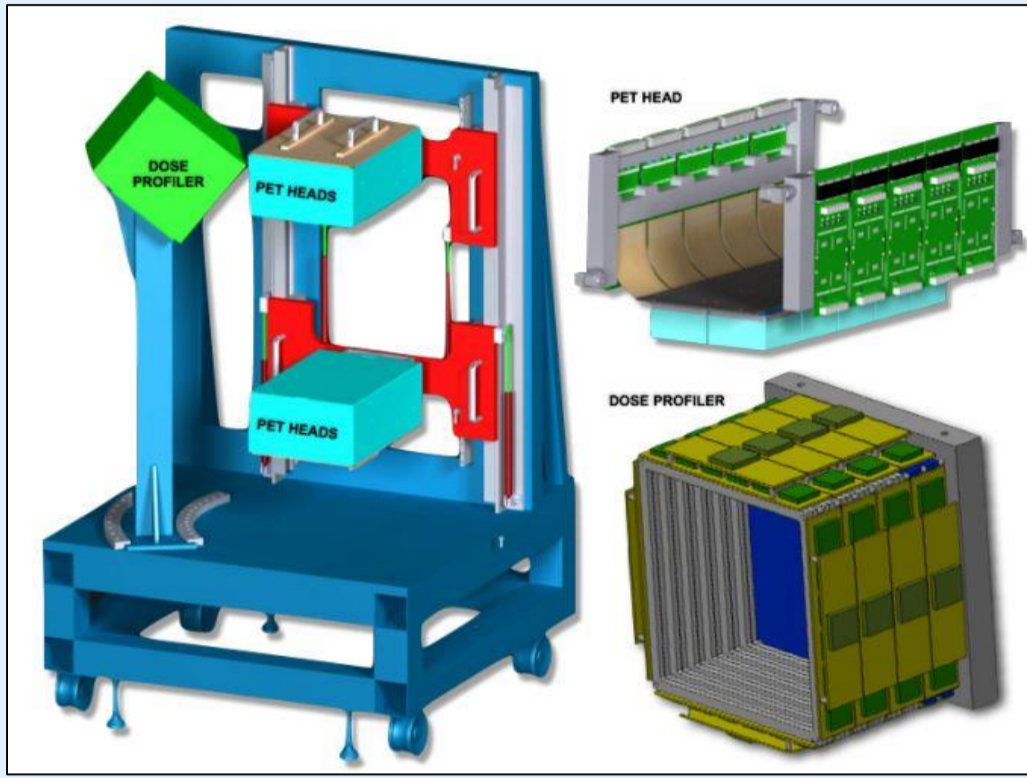
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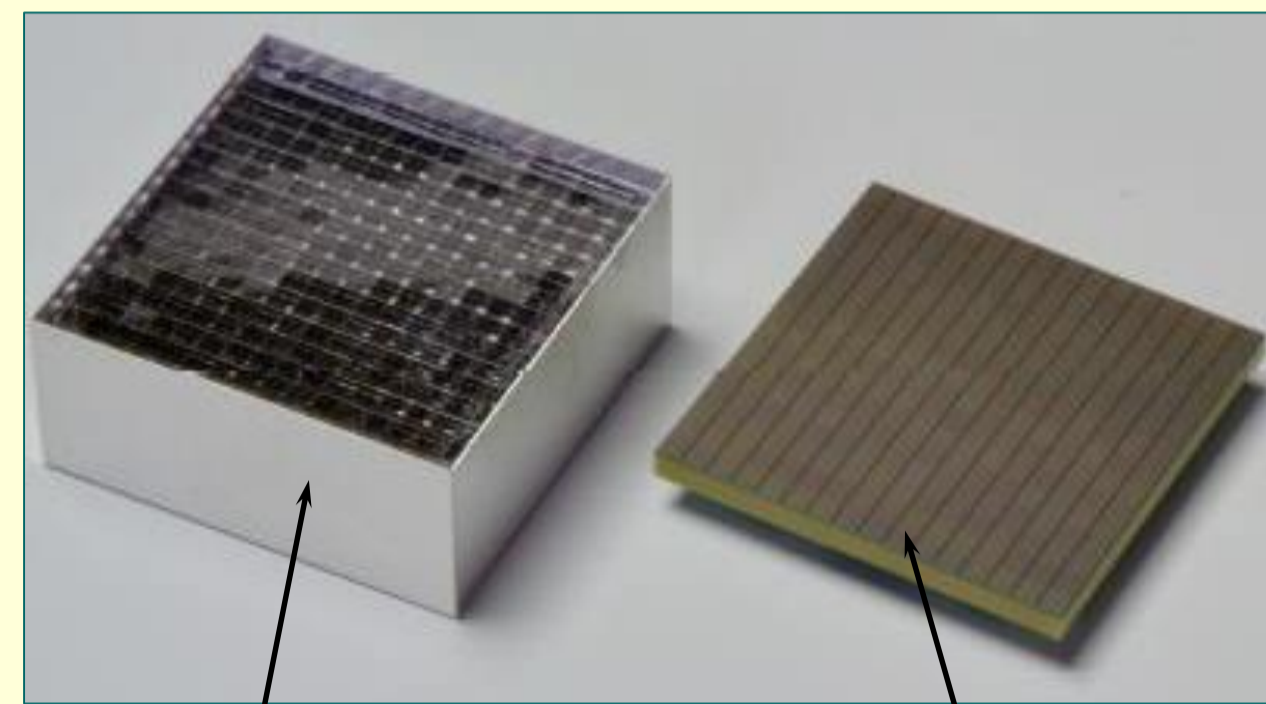
Frontier Detectors for Frontier Physics  
14th Pisa meeting on advanced detectors  
La Biodola • Isola d'Elba • Italy  
27 May - 2 June, 2018

## The INSIDE collaboration (INnovative Solutions for Dosimetry in hadrontherapy)



- Aimed at online dose monitoring in particle therapy
- Online measurements of released dose and Bragg's peak position via secondary particle emitted during the treatment
- Two planar 10x20 cm<sup>2</sup> PET heads for detection of back-to-back  $\gamma$ 's and a dose profiler for tracking charged particles and prompt  $\gamma$ 's

## PET detectors: based on pixelated LFS crystals read out by SiPM detectors



16x16 LFS pixel crystals  
(3x3x20 mm<sup>3</sup>)

16x16 array of 3x3 mm<sup>2</sup>  
Hamamatsu SiPMs (MPPCs)

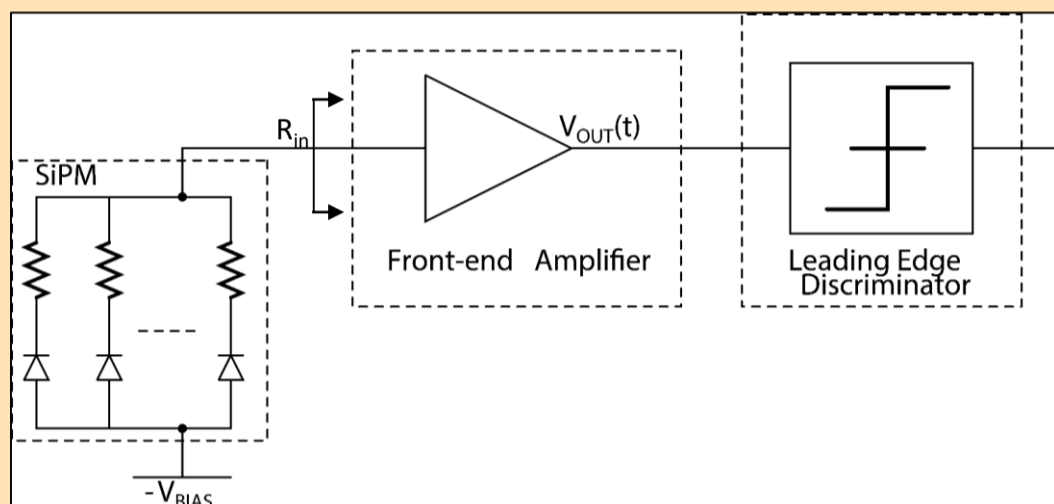
## Development of front-end electronics for the SiPMs: BASIC64

- 64 channels, 0.35  $\mu$ m standard CMOS technology
- Outputs: accurate trigger signal generated by valid events and associated energy (in digital)
- Both "p-on-n" and "n-on-p" SiPMs
- Fine tuning of the SiPM bias

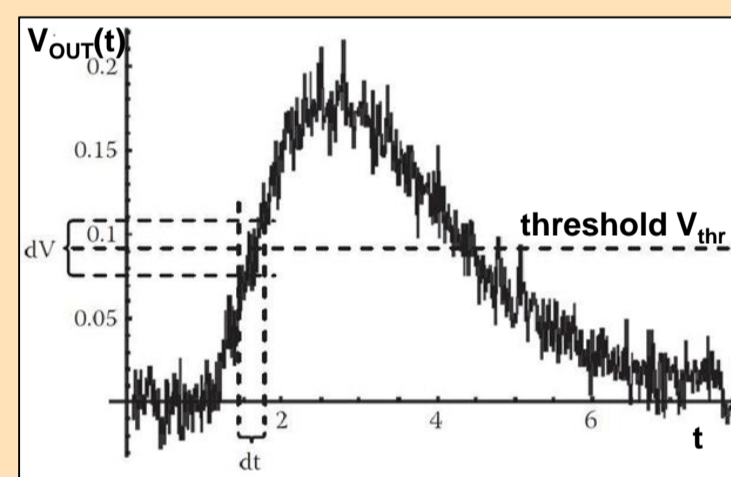
Power supply	3.3 V
Dynamic range	$\approx$ 2500 p.e.
Minimum threshold level	Single p.e.
SNR for single photon signals	20 dB
ADC resolution	10 bits
Power consumption	< 10 mW/channel
External communications	100 Mbit/s LVDS link

BASIC64 main specifications

## Design guidelines for the front-end electronics

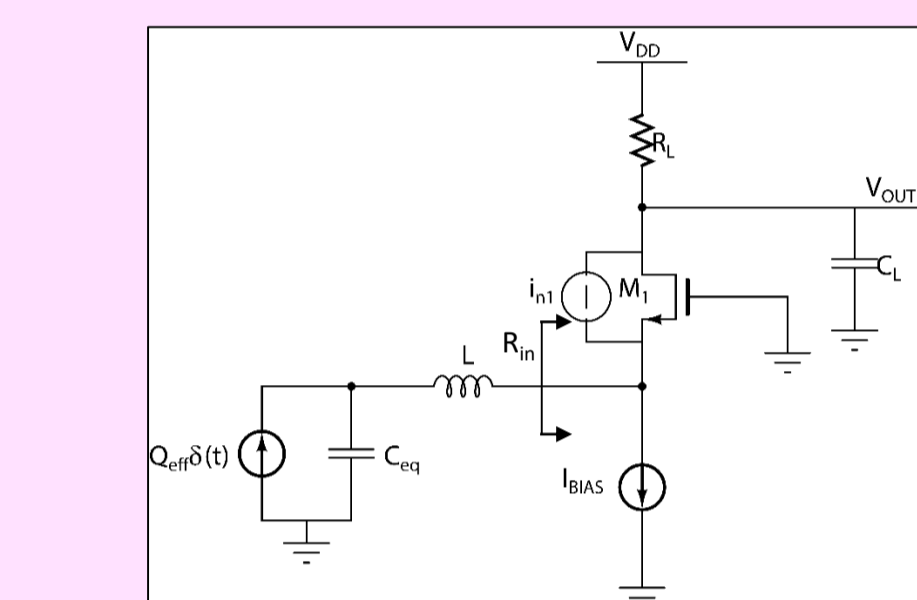


- Current-mode front-end, with low  $R_{in}$  and large bandwidth, for good time accuracy and dynamic range



$$\sigma_t = \frac{\sigma_{no}}{(dV_{OUT}/dt)_{V_{thr}}}$$

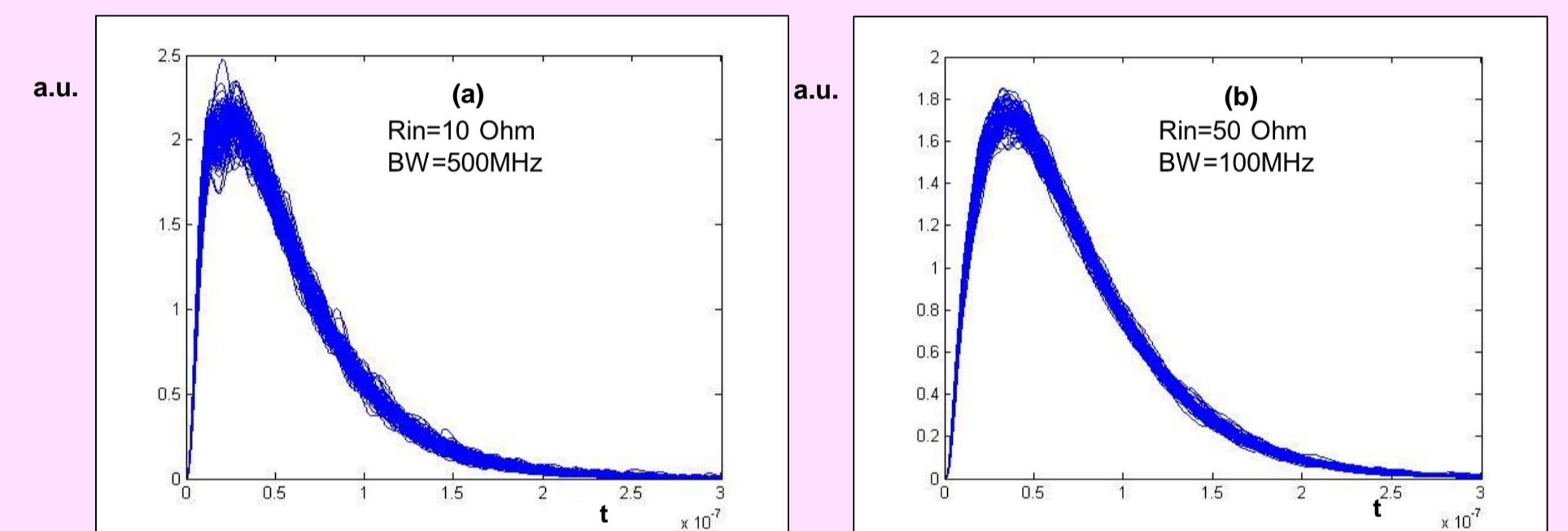
Time jitter  $\sigma_t$   
( $\sigma_{no}$  = r.m.s. output noise)



Schematic diagram of a simple current-mode preamplifier

- SiPM array coupled to the front-end electronics via flexible flat cable, with parasitic inductance  $L \approx 100$  nH
- Reducing  $R_{in}$  in presence of L slightly improves the slope of the single photon response, but increases power consumption and noise
- Also, increasing the bandwidth in presence of L slightly improves the slope of the single photon response, but increases noise

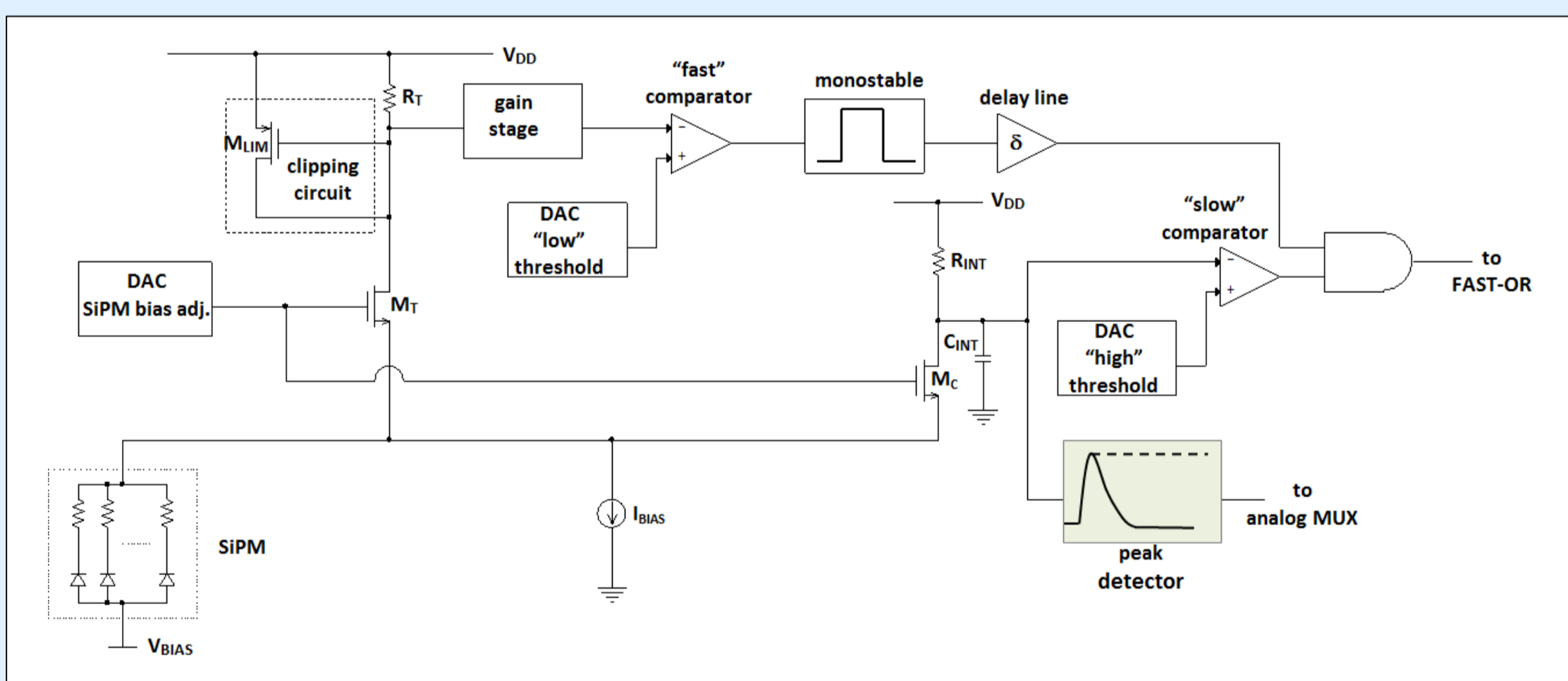
## In our case ...



Monte Carlo simulation of the output pulse of a current-mode preamplifier in response to a scintillation event (1000 p.e.) for different values of  $R_{in}$  and bandwidth BW (scintillator with 40ns time constant and 100 ps rise time)

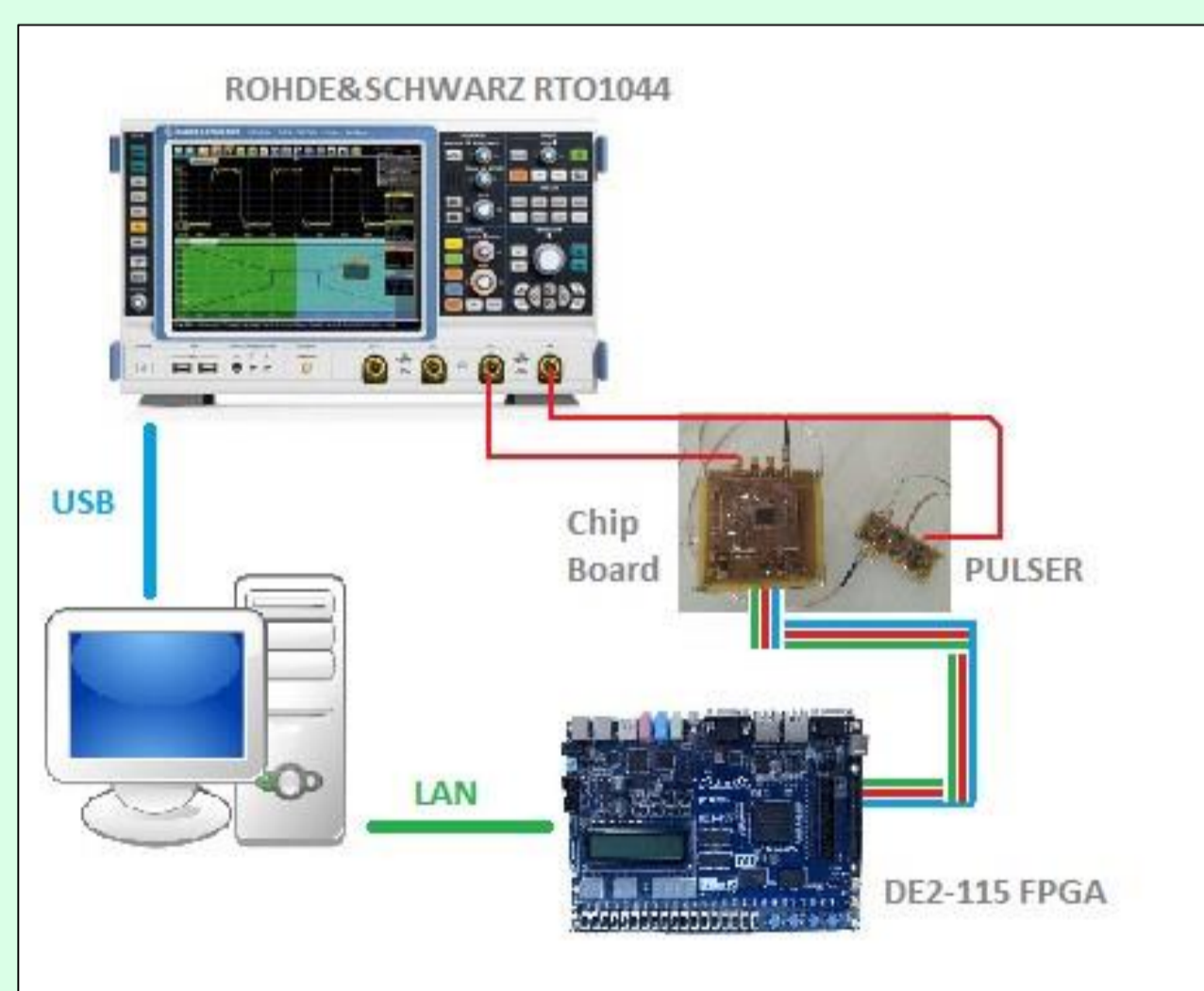
- Placing the threshold at 50% of the single photon response amplitude, we have  $\sigma_t = 130$  ps FWHM in case (a) and  $\sigma_t = 200$  ps FWHM in case (b), without considering the effects of noise (which is worse in case (a))
- In our conditions, it is not convenient wasting power to achieve very small  $R_{in}$  and very large BW

## Architecture of the analog channel (n-on-p version)



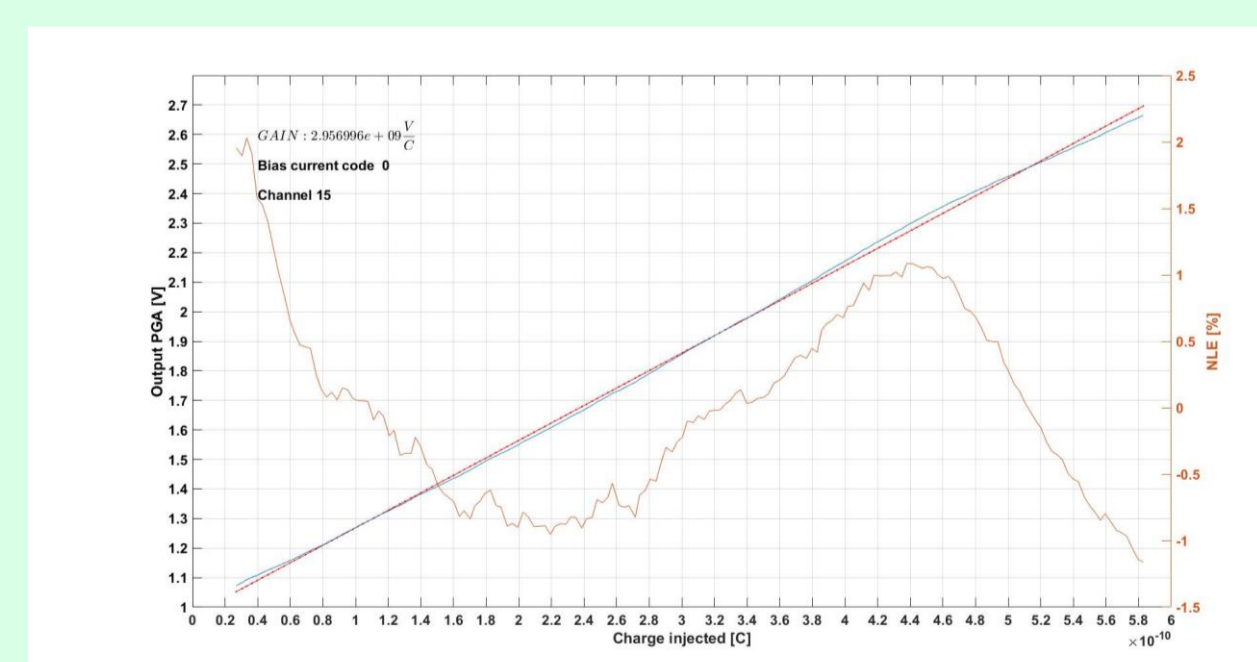
- Two signal paths, for time and charge measurement, obtained with two matched common gate MOSFETs,  $M_T$  and  $M_C$  respectively, to contain power consumption ( $R_{in} = 50 \Omega$ )
- Signal ratio between  $M_T$  and  $M_C$  set at 20:1 for increasing time accuracy and dynamic range
- Clipping circuit to avoid operation of  $M_T$  in triode region in presence of large current signals, which can compromise the signal path for charge measurement
- 8 bit DAC for SiPM fine bias adjustment
- Time measurement path (BW = 100 MHz) completed by a gain stage and a fast comparator, with programmable "low" threshold (10 bit DAC)
- Timing accuracy dominated by the statistic behavior of the scintillator
- Estimated timing jitter (MC simulations of the scintillation pulse with 1000 p.e.)  $\approx 300$  ps FWHM, taking into account a 0.9 ns rise time for the scintillator
- Integration time constant of the charge path equal to 170 ns
- Trigger signal from the channel disabled if the associated charge does not overcome the programmable "high" threshold (8 bit DAC)
- Peak detector operation: a) voltage follower, while waiting for a valid event; b) peak detector, soon after the detection of a valid event; c) analog memory after the peak has been reached

## Experimental test & characterization

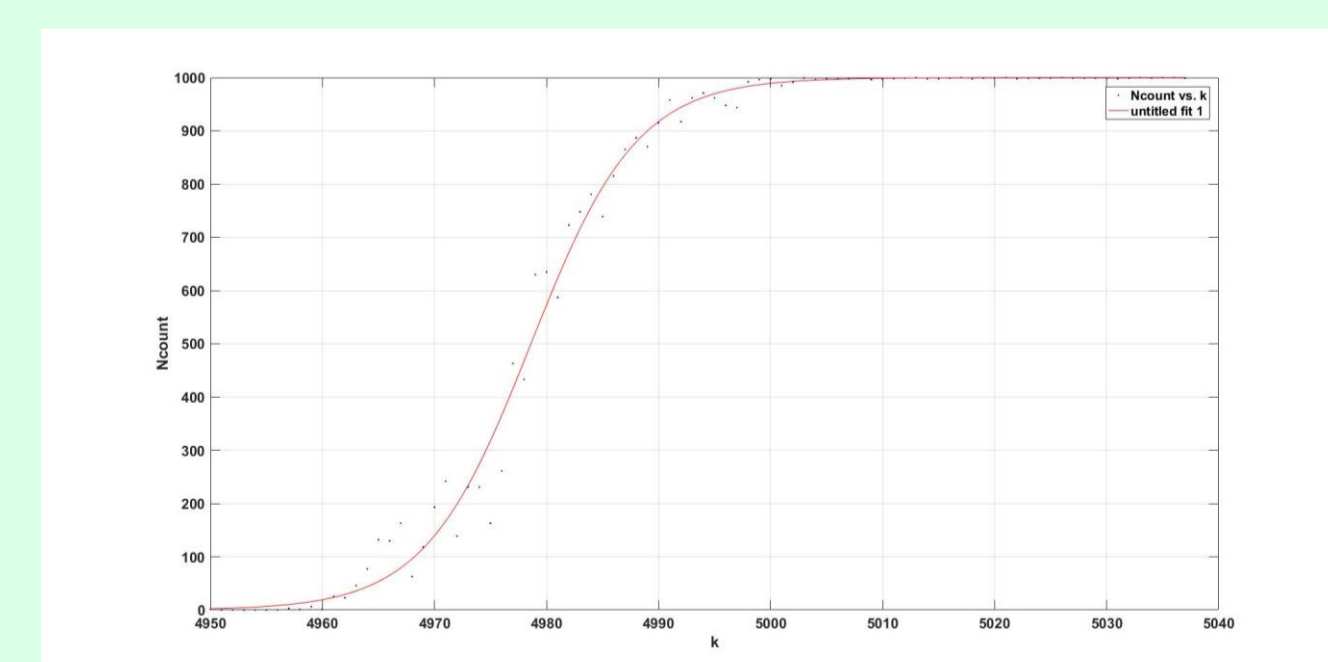


Experimental test setup

MEASUREMENTS RESULTS		
Parameter	Measured Value	Unit
Timing jitter	40	ps ( $1\sigma$ )
Gain	3	mV/pC
Non-Linearity Error	1.5	%
Noise	580	fC (FWHM)



a) Gain and Non-Linearity Error vs. input charge

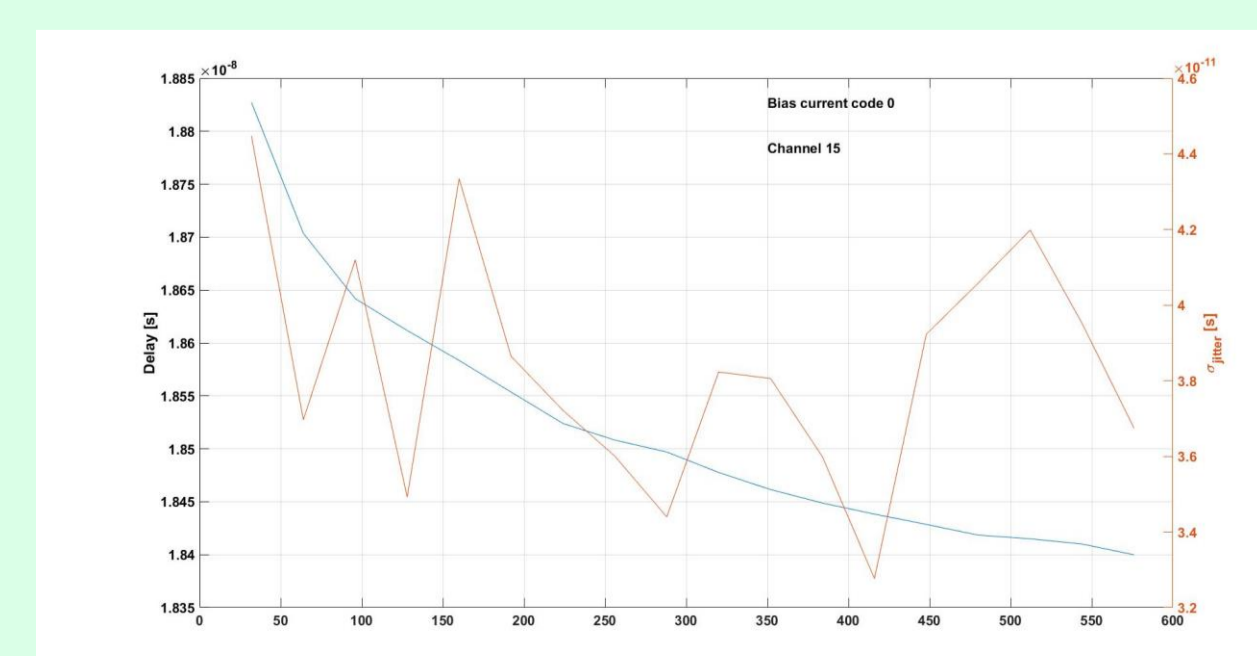


c) S-Shape curve vs. input charge @ fixed threshold

- a) Energy measurements: input signal has been swept to vary injected charge from 32 pC to 576 pC in 3.2 pC steps; the analog output voltage values has been acquired and processed.
- b) Timing measurements: the distribution of the time differences between the Pulser signal timestamp and the trigger out signal timestamp of the ASIC has been acquired by cycling with a fixed charge value at the input; the input signal has then been swept with a narrow span and measurements repeated.
- c) Noise measurements: keeping constant the timing discriminator threshold, the input signal has been swept and 1000 samples collected for each step, counting as ones only the valid events (chip triggering).

## Conclusions and perspectives

- The ASIC is suited for resolving the 511 keV peak in terms of timing accuracy and gain linearity.
- Further measurements with a SiPM detector coupled to the ASIC would allow fully characterization of the system's application.
- Extensive characterization of all the ASIC channels with more prototypes involved is needed to prove the robustness and repeatability of the circuit performance at large scale.



b) Jitter and Delay vs. input charge