The Phase-I Trigger Readout Electronics Upgrade of the ATLAS Liquid Argon Calorimeters

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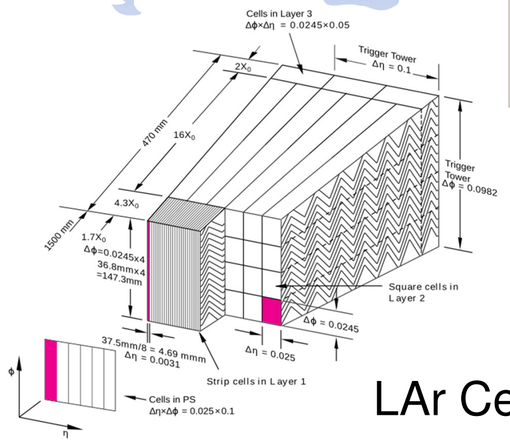
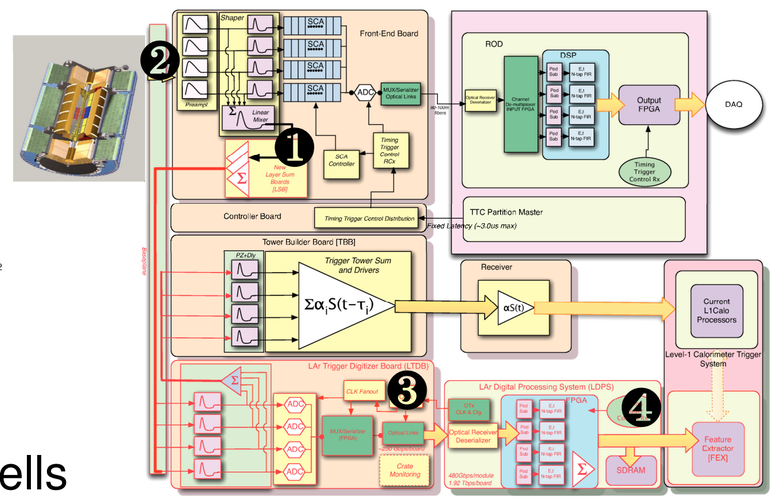
On the behalf of ATLAS LAr group

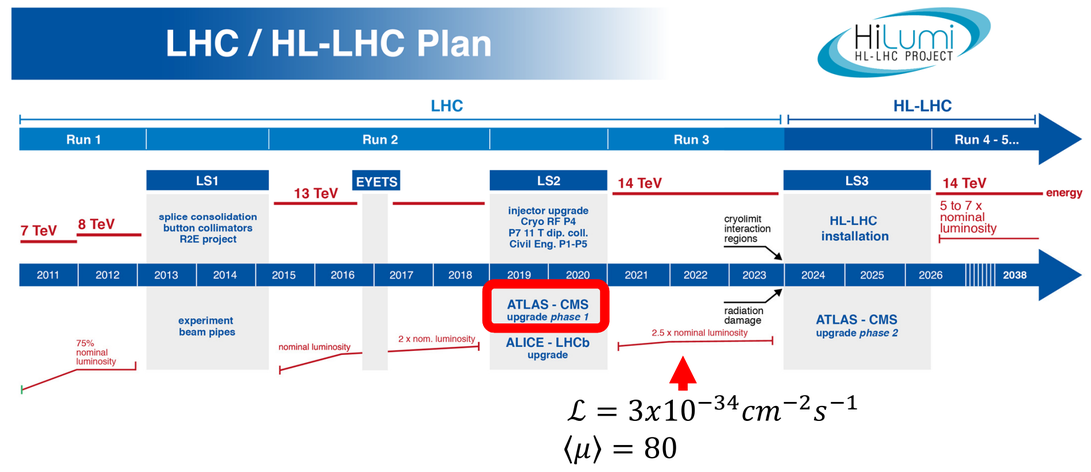
LAr Phase-I Upgrade



LAr Cells

Front-End(FE) Back-End(BE)

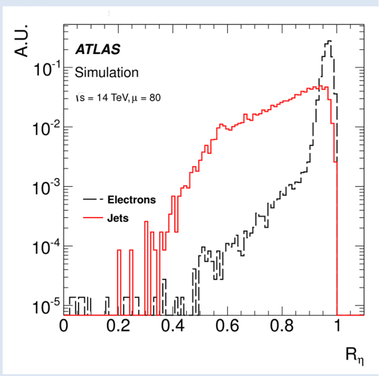




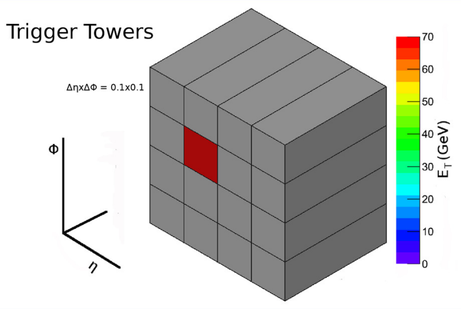
$\mathcal{L} = 3x10^{-34} cm^{-2} s^{-1}$
$\langle \mu \rangle = 80$

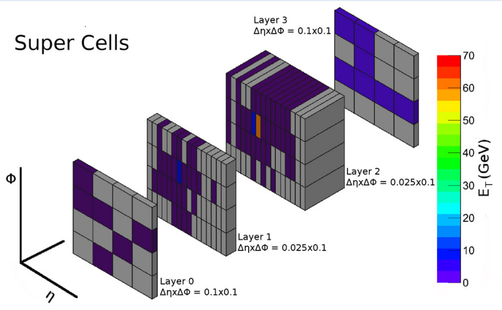
Super Cell

- *New LAr trigger system for high pile-up environment*
  Improved trigger selectivity to maintain present trigger thresholds in high pile-up conditions
- *Add longitudinal shower information and finer granularity* : trigger sums per detector layer, with four times improved granularity in eta direction for middle and front layers *(0.025), instead of present analog sum (Trigger Towers, 0.1 by 0.1) over all detector layers.*
- *On-detector digitization*
- *Total 34048 super cells*



Improvement on the separation between electrons and jets. This will going to be implemented in level 1 trigger





Back End – LDPS ❹

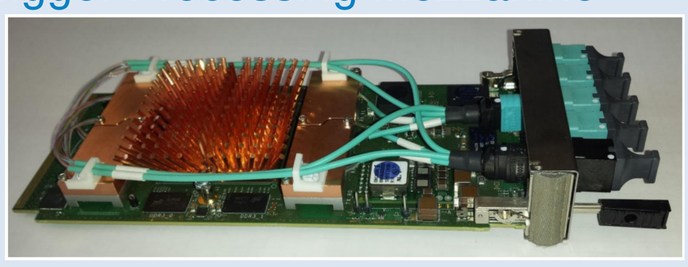
*LDPS(LAr Digital Processing System) receives digitized data(ADC), send E_T to FEX(Feature Extractors) and monitoring. Build on **ATCA** architecture*

◆LAr Carrier

Provides data transmitting, monitoring and control signal

◆LATOME - LAr Trigger Processing Mezzanine

- INTEL™ Arria™ 10 FPGA
- 2 GB DDR3
- 48 input fibers 5.12 Gb/s per fiber
- 48 output fibers 11.2Gb/s per fiber



- Capable up to 320 channels

◆Energy Reconstruction in LATOME

- FIR Filter

$$E = \sum_{i=1}^{N} a_i (S_i - P)$$

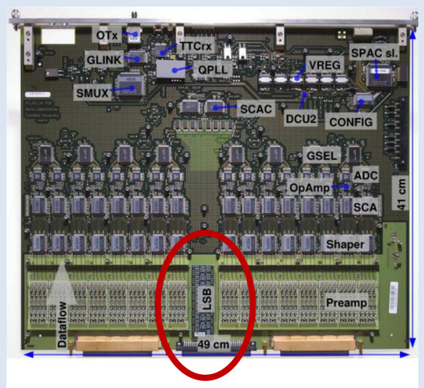
a_i : coefficient P : pedestal
S_i : ADC data N : N. of samples

- Framework
  - Serialized 6 channels with 240MHz
  - 62 parallel processing
- Features
  - Coefficients & pedestals stored in circular buffer
  - Cascaded DSP blocks
    - ✓ Minimized wiring delay
    - ✓ All calculation done in DSP blocks

Front End (On Detector)

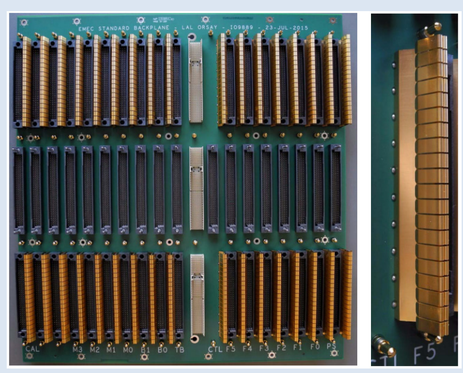
❶ LSB-Layer Sum Board

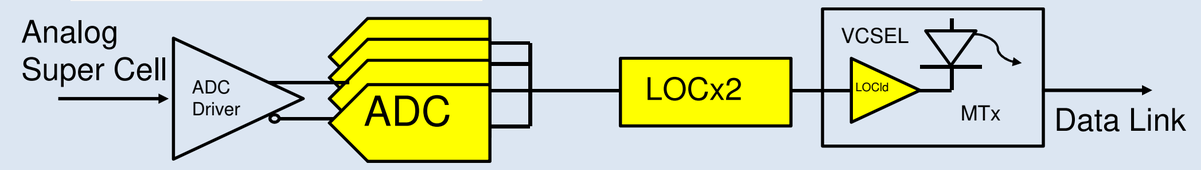
Sums the LAr cell signal into SuperCell signal.



❷ Baseplane

Distributes the signals among LTDB, FEB and TBB

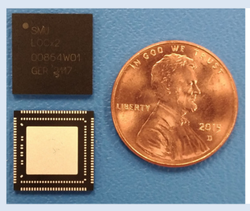




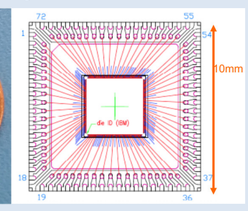
◆ASIC

Radiation qualified up to 3000 fb^{-1} integrated luminosity

- Nevis15 (ADC)
  4 channels 12 bit
  TSMC 130 nm technology
- LOCx2 (Serializer)
  dual-channel input (each for 2 ADCs)
  250 nm SOS technology
- LOCld- dual channel laser driver



LOCx2

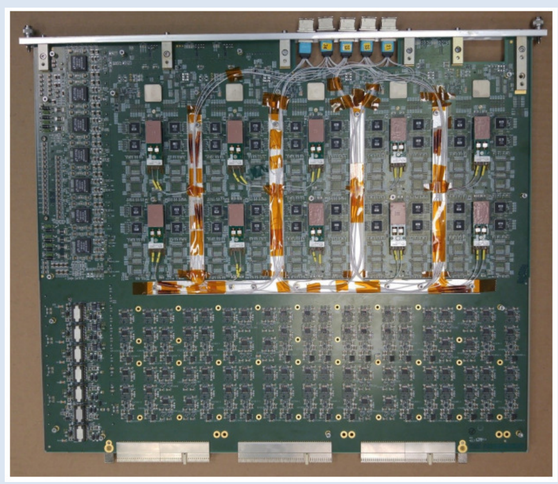


Nevis 15

❸ LTDB

-LAr Trigger Digitizer Board

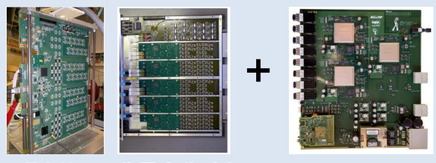
- 80 Nevis15 ADC
- 20 LOCx2
- 20 MTx and 5 MTRx
- Analog socket
- PDB-LTM power mezzanine
- Capable up to 320 channels



Demonstrator Results in 2017

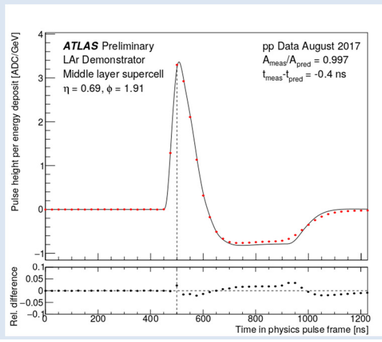
Installed in 2014, decommissioned in 2018

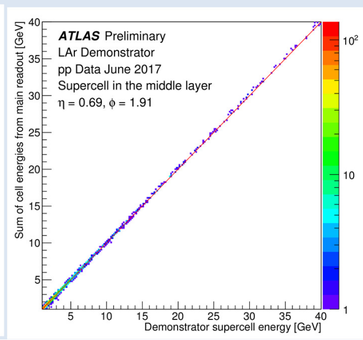
Front End Back End



BNL CEA/LAL ABBA

The results show good consistency with main readout





New demonstrator in 2018

- Pre-production LTDB
- LArC+LATOME

ATLAS Collaboration, ATLAS Liquid Argon Calorimeter Phase-I Upgrade Technical Design Report, CERN-LHCC-2013-017 (2013)

ATLAS EXPERIMENT