Towards the large area HVCMOS demonstrator for ATLAS ITk

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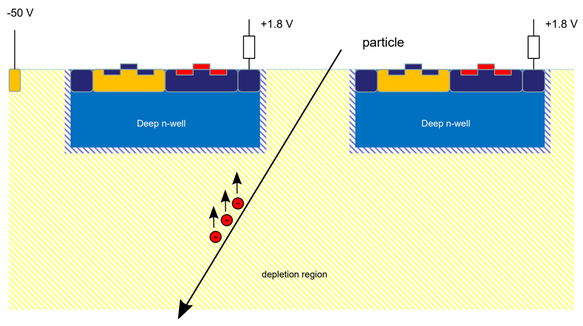
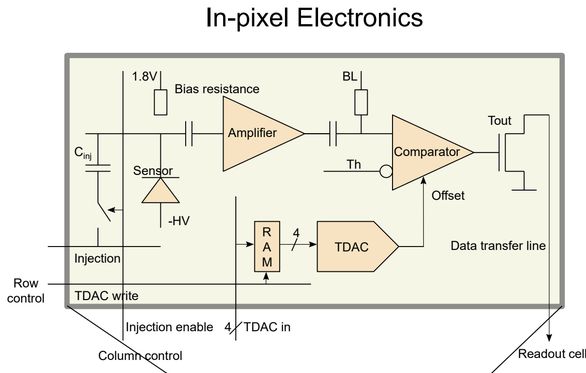
High Voltage CMOS (HVCMOS) sensors

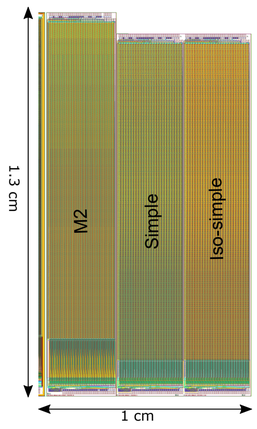
- Monolithic pixel sensors implemented in commercial CMOS process
- High efficiency in detection of ionizing particles
- Proposed cost-effective alternative to hybrid sensors in ATLAS inner tracker



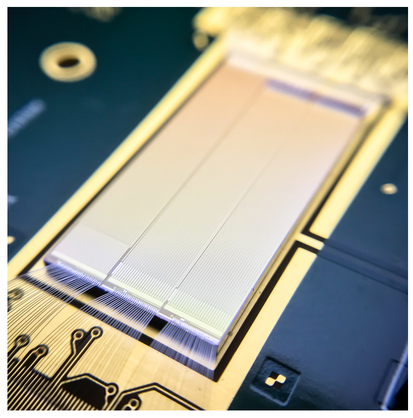
ATLASpix: Large fill-factor design



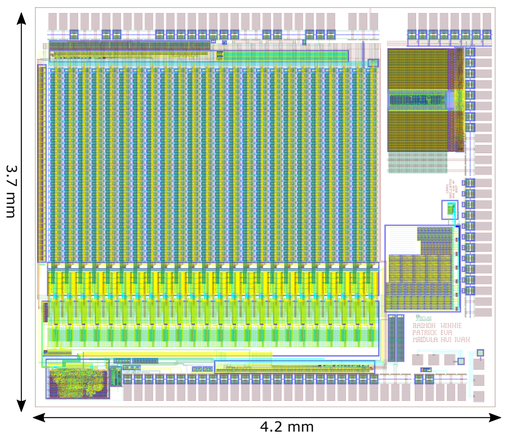
ATLASpix design roadmap



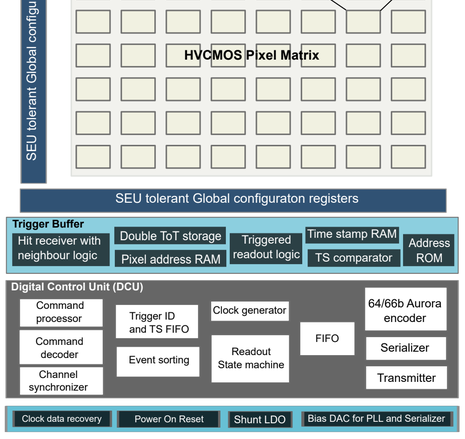
ATLASpix1 layout



ATLASpix1 post-silicon



ATLASpix2 layout

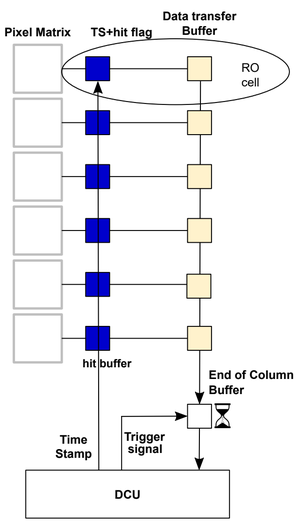


ATLASpix3 design at block level

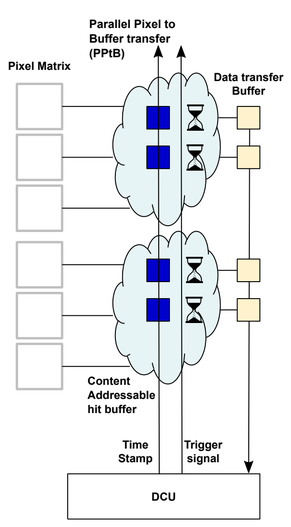
2016 Nov Dec 2017 Jan Feb Mar April May June July Aug Sep Oct Nov Dec 2018 Jan Feb Mar April May Time

ATLASpix1: First engineering run in 0.18µm

ATLASpix1 contains 3 design flavors namely Simple, M2 and IsoSimple based on the comparator type and readout type. Fabricated in AMS ah18 high voltage process, ATLASpix1 is the first large area HVCMOS prototype in 180nm gate length. ATLASpix1_M2 Introduces a novel triggered readout scheme called "Content Adressable hit Buffer (CAB) readout" which is aimed to cope with high particle hit rates. The hit signals are transferred in parallel from the pixels to the hit buffer (PPtB). The hit buffers store the hit information until the trigger latency elapses. Only the hits whose time stamps match the trigger signal marked for readout (content addressing). When compared to the traditional column drain readout scheme, CAB readout scheme helps to lower the traffic in data transfer bus.



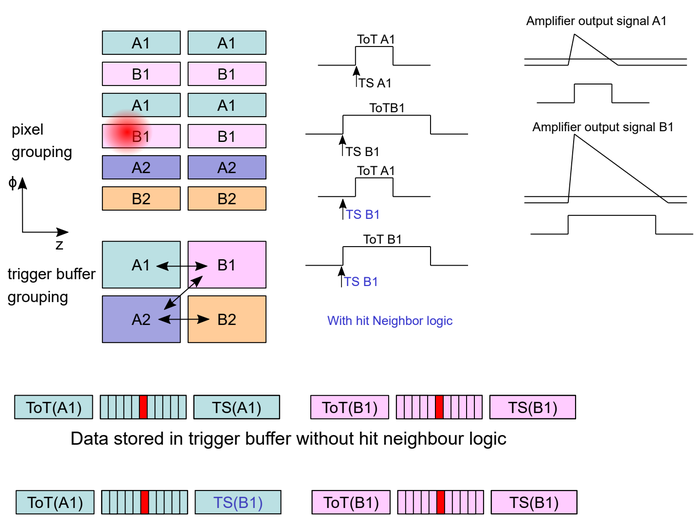
Column drain readout (FE-I3 like)



Content Addressable hit Buffer readout (CAB)

ATLASpix2: New features

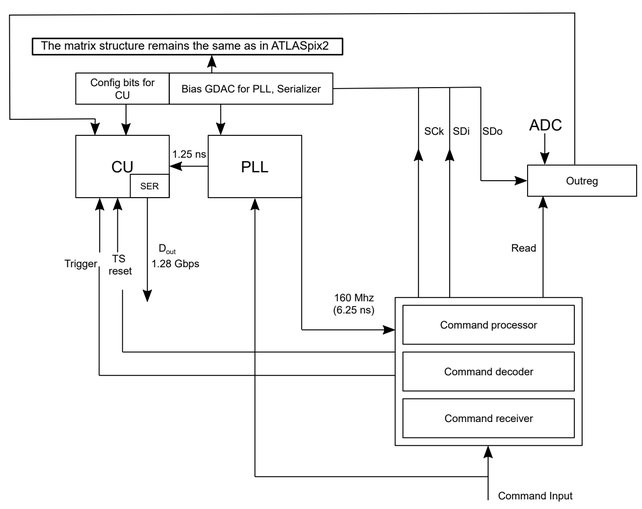
While pixel grouping has its merits, the Time-over-Threshold (ToT) implementation can be challenging because we can store only one ToT per pixel group due to memory constraints. The pixel grouping needs to be done in a smart way in order to have good spatial resolution. In ATLASPix2, the interleaved pixel grouping helps to have two ToTs per cluster. On the other hand, two sets of hit data are stored for a single cluster. This leads to the double ToT storage per hit buffer in ATLASpix3. Hit neighbour logic in ATLASPix2 ensures that, when there is a cluster, the Time Stamp (TS) corresponding to the pixel that has larger charge sharing is recorded. ATLASpix2 is currently being fabricated using AMS ah18 process. Test beam and irradiation tests are planned.



ATLASpix3: Design improvements

Each ATLASPix prototype is engineered to meet the specifications of HL-LHC pixel barrel outer layers. ATLASPix3 is a large area HVCMOS sensor chip with all the desired features that can be used for module construction. It is the HVCMOS demonstrator chip. The functional blocks of ATLASpix3 are currently being integrated.

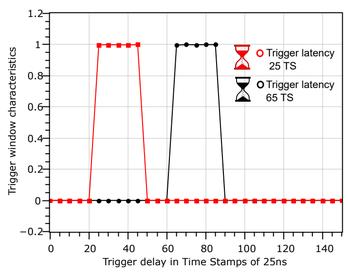
The highlights of ATLASpix3 design are event sorting according to trigger ID, double ToT storage per hit, command decoder and aurora 64/66b data encoder. The readout data format is made compatible with RD53a. ATLASpix3 submission is planned in November 2018 on TSI 180nm process using high-resistive wafer.



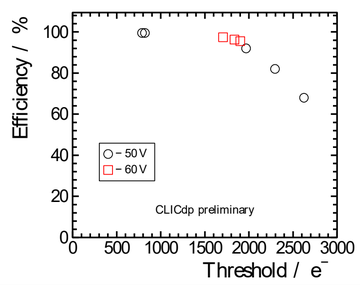
Parallel pixel to buffer readout (FEI4 like)

ATLASPix1 experimental study

Triggered readout



Detection efficiency vs global threshold



Conclusions

- ATLASpix1_Simple chip shows maximum detection efficiency of 99.5% in a test beam measurement at CERN
- CAB readout concept in ATLASpix_M2 chip is working

References

[1] I. Peric, et. all., HVCMOS Sensors - Progress towards final tracking sensor designs for Mu3e and ATLAS experiments, HSTD (2017) Status: Submitted (https://indico.cern.ch/event/577879/contributions/2740414/)

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