First-Level Muon Track Trigger for Future Hadron Collider Experiments

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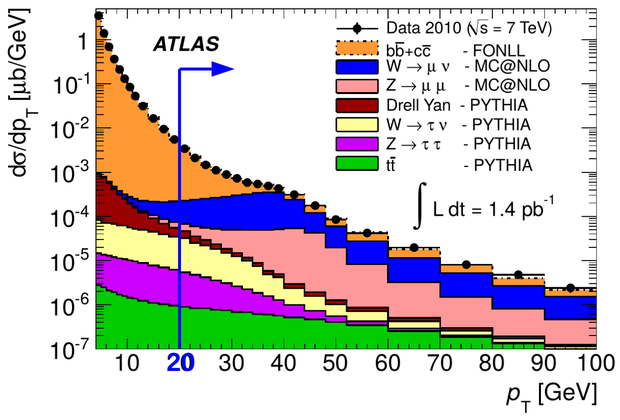
Motivation

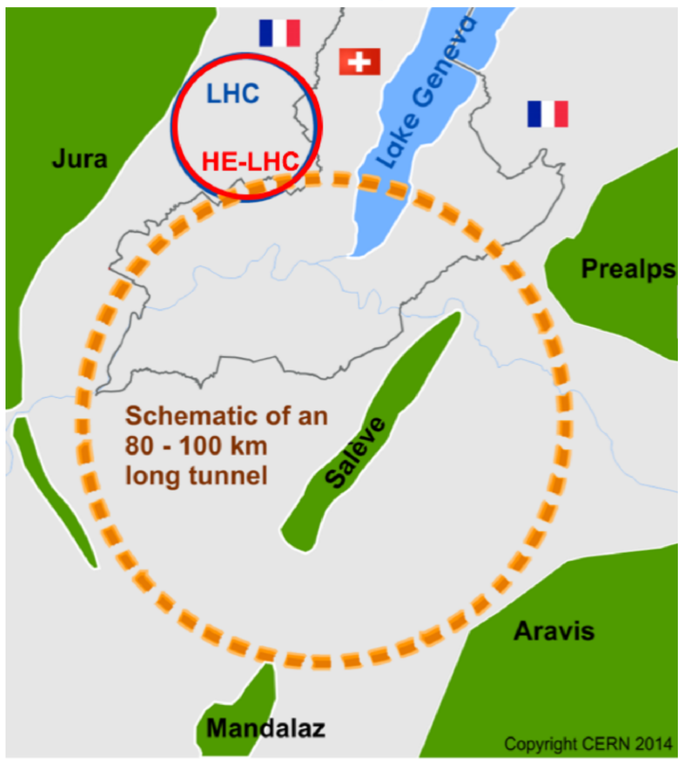
Importance of low p_T single-muon triggers at pp colliders

Inclusive muon spectrum



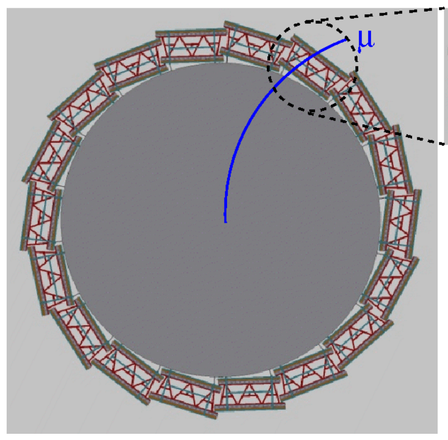
- The interesting electroweak physics is mainly at p_T>20 GeV.
- The inclusive muon cross section is very steeply rising with decreasing p_T.
- In order to limit the single muon rate at low transverse momenta, good momentum resolution at the trigger threshold is mandatory.

Future hadron collider projects



- High-luminosity LHC: √s= 14 TeV.
- High-energy LHC: √s= 28 TeV.
- Future circular collider: √s=100 TeV.
- Muon drift-tube (MDT) chambers with high spatial resolution will be used or are proposed for the muon systems of the experiments at these future colliders.

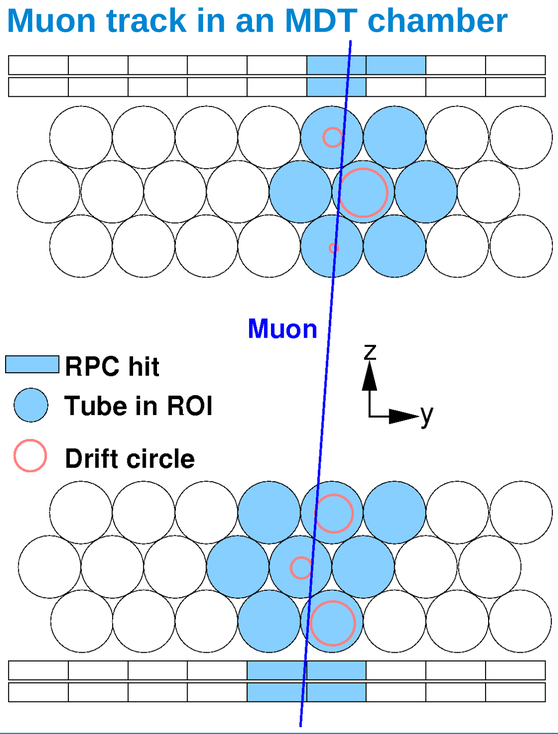
Example of the proposed FCC muon system



- RPC for precise timing → BCID.
- MDT for precise direction measurement.

Compact muon finder for fast muon track reconstruction at the first trigger level

Muon track in an MDT chamber



Compact muon finder algorithm

MDT hit preparation

- Use the MDT hits in the RPC to define a region of interest (ROI) and to determine the pp collision time (BCID).

MDT pattern recognition

- Determine a seed $\bar{m}$ for the muon track slope from the RPC hits.
- Consider only tubes in the ROI and use the BCID to convert hit times into drift times and drift radii.
- Solve the relationship for the distance of a straight line $y=\bar{m}z+b$ from an anode wire at (w_y, w_z) for b:

$$r = \frac{|\bar{m}w_z + b - w_y|}{\sqrt{1+\bar{m}^2}} \Rightarrow b_\pm = \pm r\sqrt{1+\bar{m}^2} - (\bar{m}w_z - w_y)$$

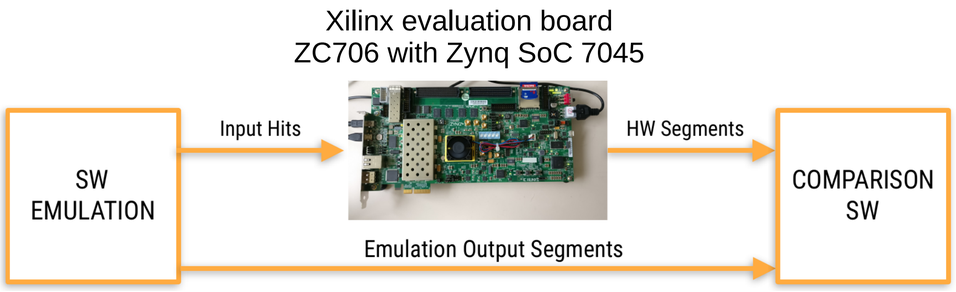
- Fill two histograms, one for each multilayer, with the corresponding values of $b_\pm$ for each MDT hit in the ROI.
- The histograms will have maxima at the right values of b.

MDT track fit

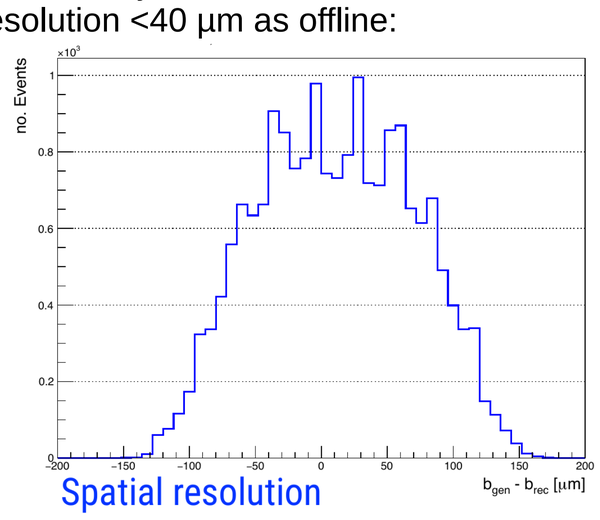
- Fit a straight line through the MDT hits belonging to the maxima to determine the track slope and track position precisely.
- Convert the track angle into a muon momentum.

Hardware implementation and test of the compact muon finder

Firmware implementation test-set-up



- Compact muon finder implemented in C++ and VHDL.
- Implementations tested with simulated and muon test-beam data.
- Firmware implementation tested against the C++ version on a Zynq SoC 7045 FPGA on a Xilinx evaluation board.
- Algorithm efficiency >99%.
- Spatial resolution <40 μm as offline:



Spatial resolution

Firmware implementation and FPGA resource usage

- 3 compact muon finders could be implemented on the FPGA.
  - Pipelined design (receives one hit/clock).
  - Light resource usage (LUT 70k, FF 52k, BRAM 12, DSP 770)
  - Low latency: 250 ns @ 240 Mhz.
- Firmware version delivers the same track parameters as the C++ emulation of the compact muon finder.