

FATALIC: a fully integrated electronics readout for the ATLAS tile calorimeter at the HL-LHC

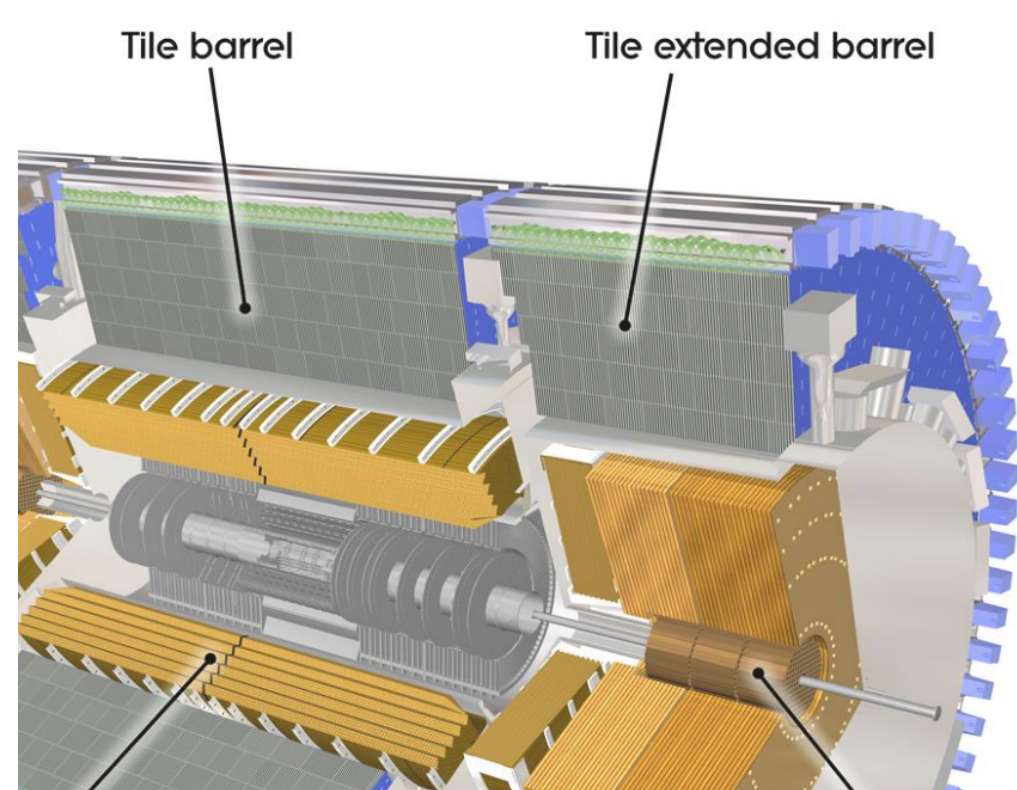
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ATLAS Tile Calorimeter

Sampling calorimeter with scintillating tiles.

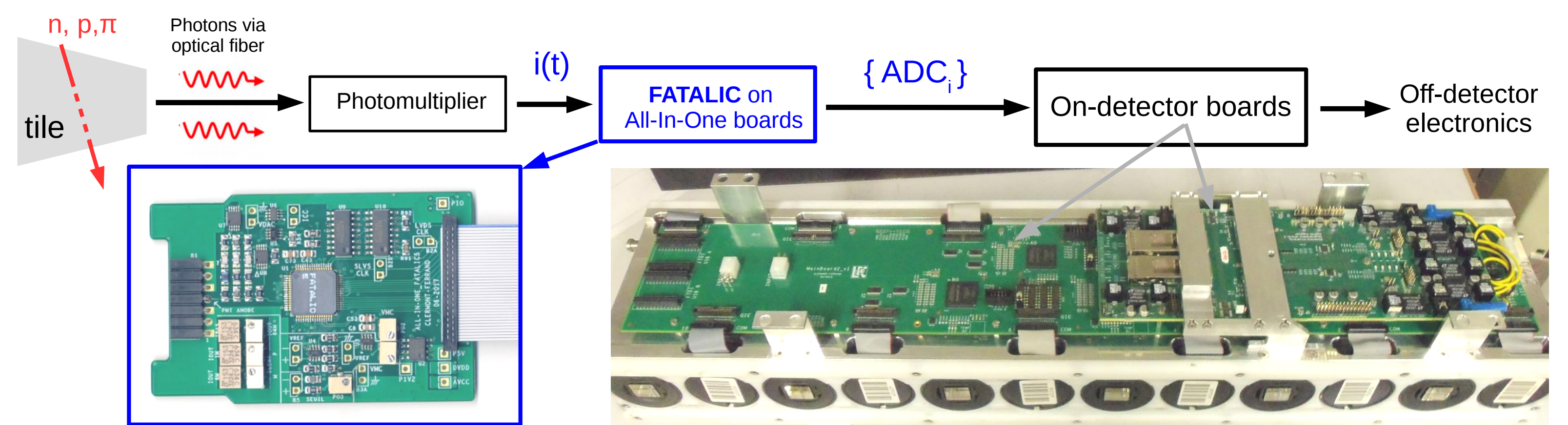


What?
Measuring energies from 0.1 to 1000 GeV

Why?
Jets leave up to 40% of their energy in this calorimeter

500 000 tiles • $\approx 5\,500$ cells • 2 PMs/cell

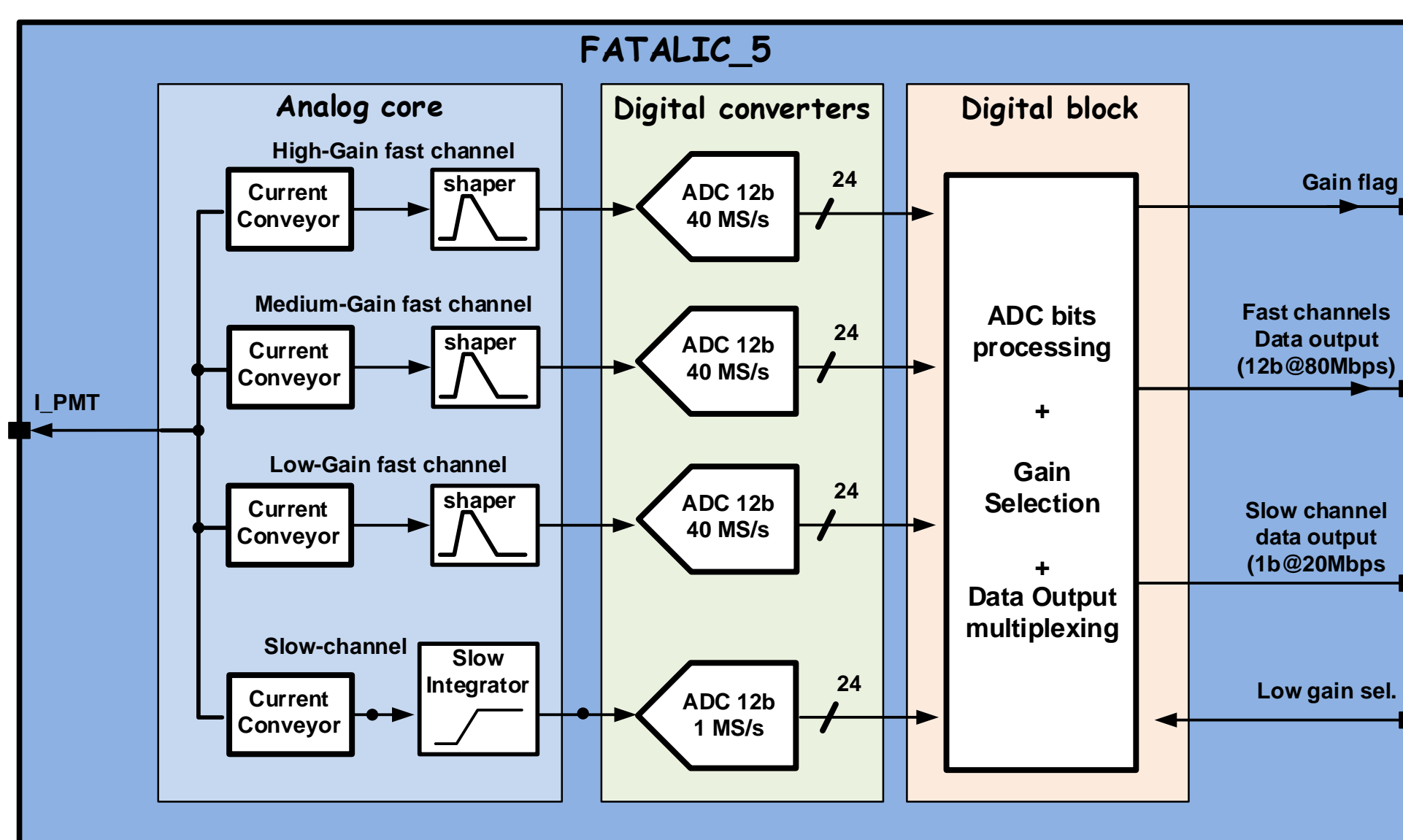
Schematic view of the detection chain



The light produced by tiles is converted by a photo-multiplier (PM) into electric current $i(t)$, which is processed by the *readout electronics* sending ADC counts to the rest of the chain.

Overview of FATALIC readout

ASIC CMOS 130 nm • shaping • digitisation • 3 gains • 12-bits ADC • integrator



ASIC specifications

Physics (*fast channel*)

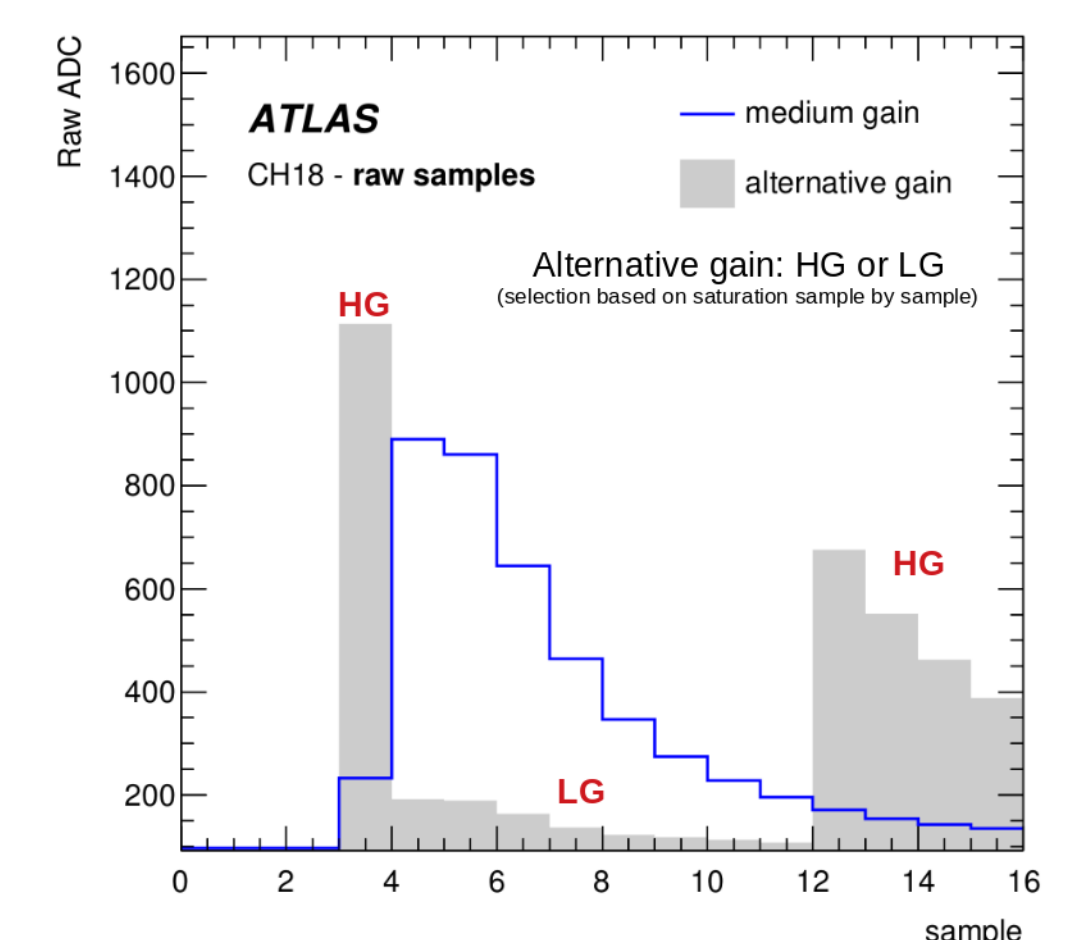
$Q = 25 \text{ fC} - 1.2 \text{ nC}$
 $\sigma_Q \leq 12 \text{ fC}$
Linear at 1% up to 0.8 nC
25 bits at 40 MHz

Calibration (*slow channel*)

$I = 0.5 \text{ nA} - 11 \text{ }\mu\text{A}$
 $\sigma_I \leq 0.25 \text{ nA}$
 $t_{\text{meas}} = 10 \text{ ms}$

Dynamic gain switch

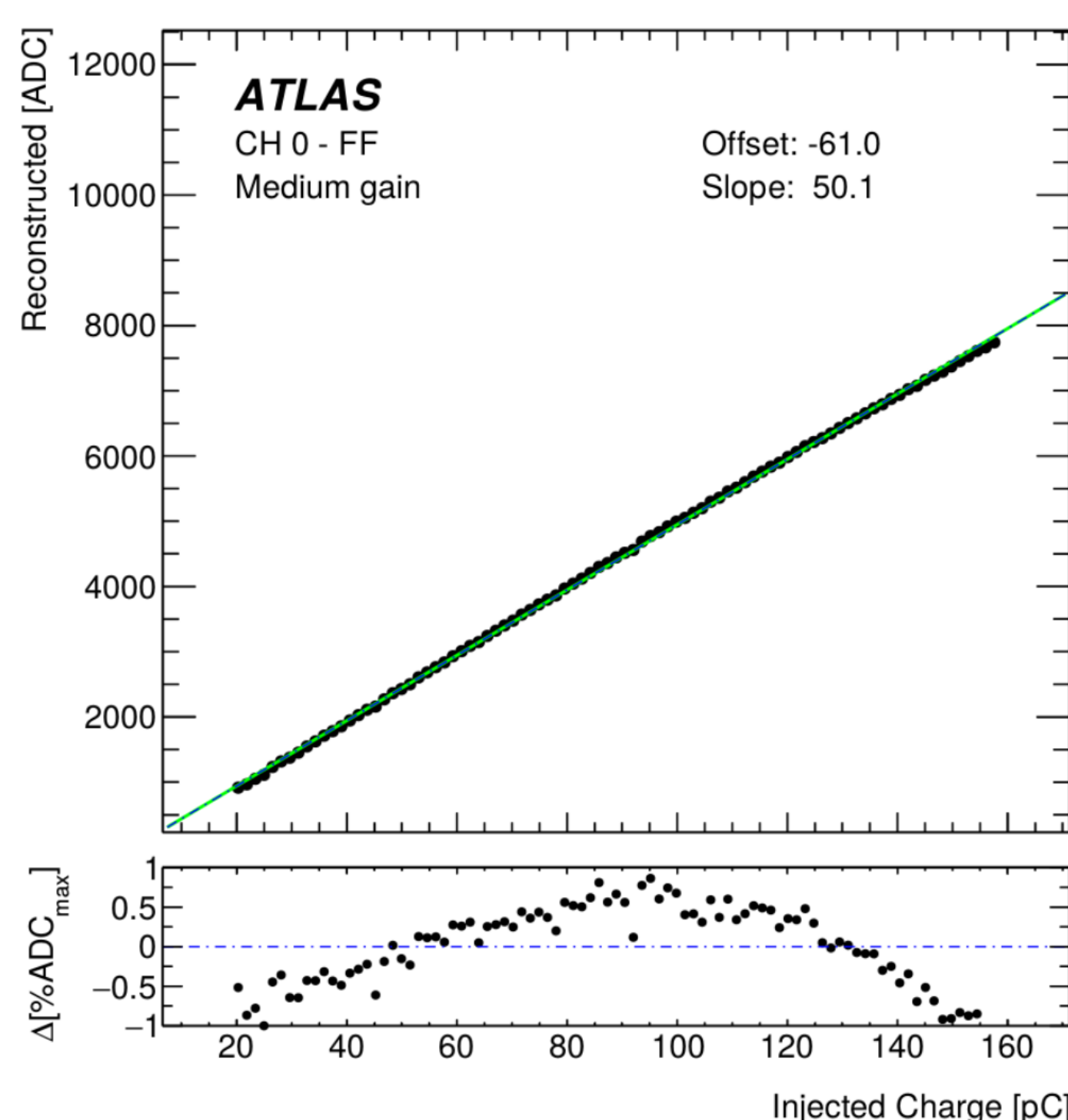
How to fit the bandwidth limitations (25 bits) with the precision of 3 gains (12-bits)?



Sample-by-sample gain selection allows to output only the 2 gains which are relevant

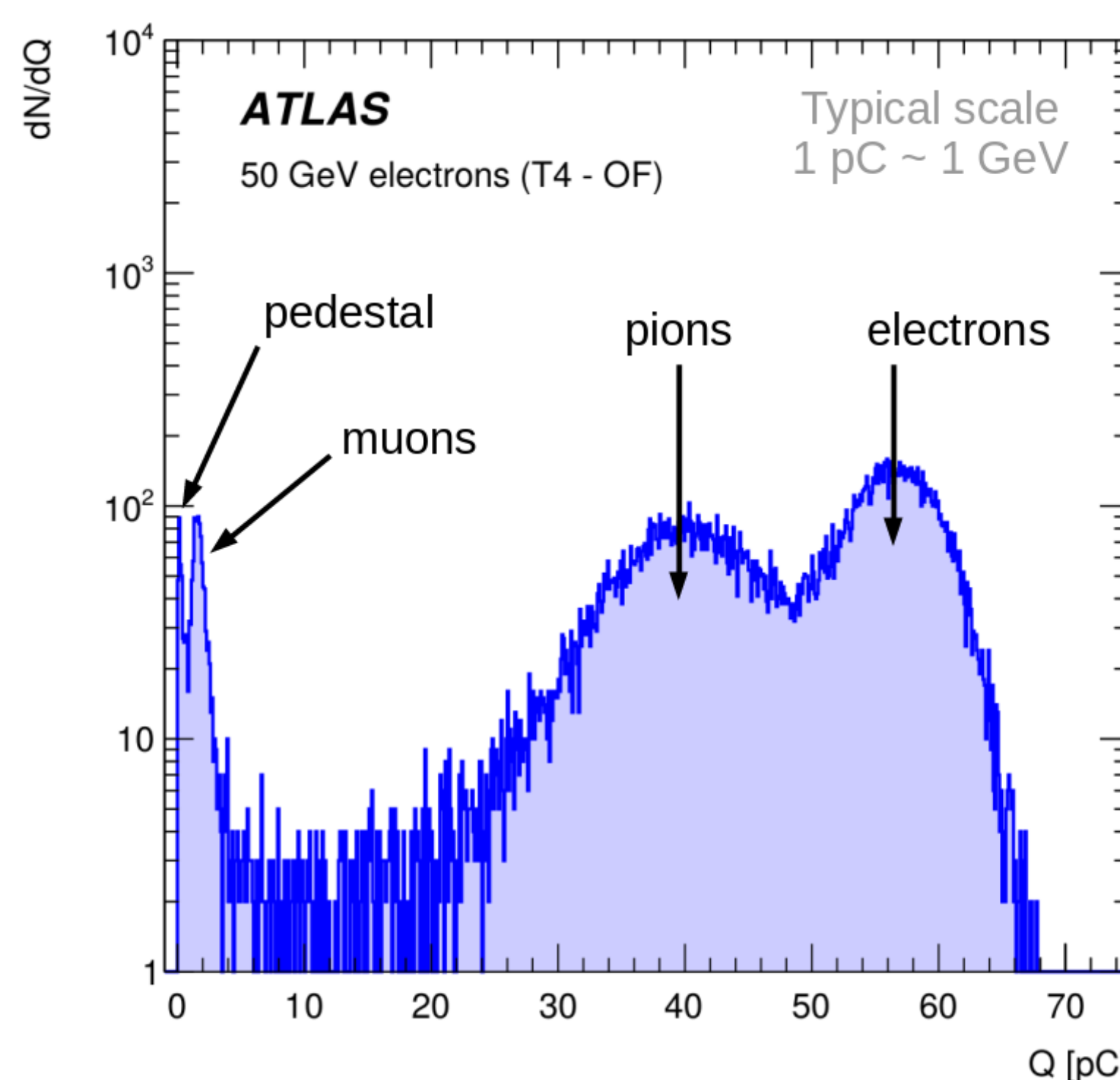
Intrinsic performances

Noise: $\sigma_Q = 6.2 \pm 0.2 \text{ fC}$
Non-linearity: $-0.03 \pm 0.02\%$ at 0.8 nC
Integrator noise: $\sigma_I \approx 6.5 \text{ nA}$ (limited by CMOS technology with $1/f$ noise)



Test beam results

FATALIC tested at CERN using beam of π , e and μ . Energy reconstructed from ADC counts using *optimal filtering* (OF)



High pile-up simulation

Simulation of resolution after adding signal from previous collisions (pile-up).

How? By adding delayed secondary pulses, with amplitudes given by simulation.

