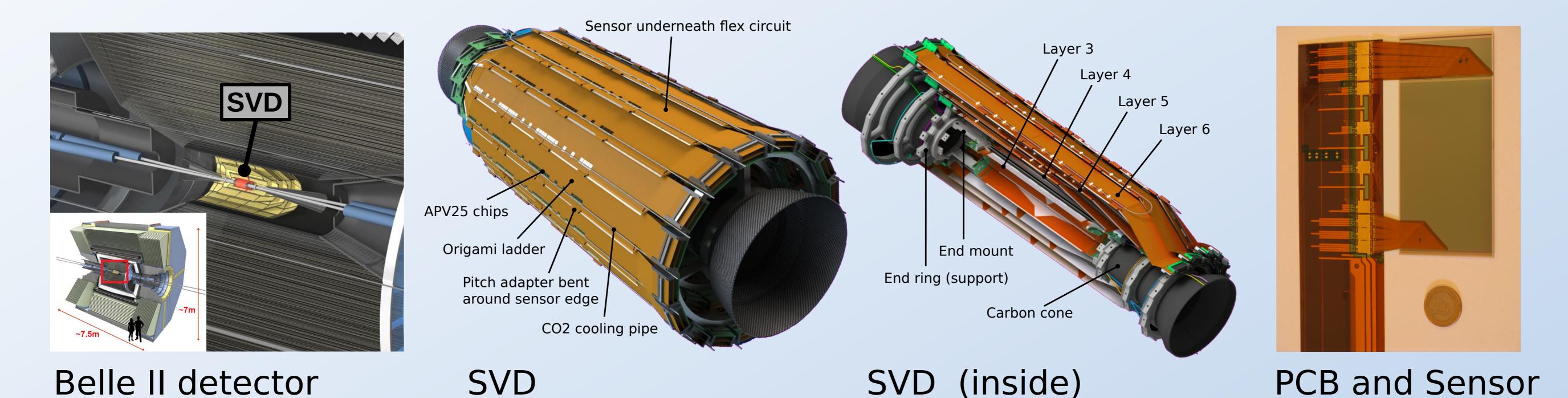
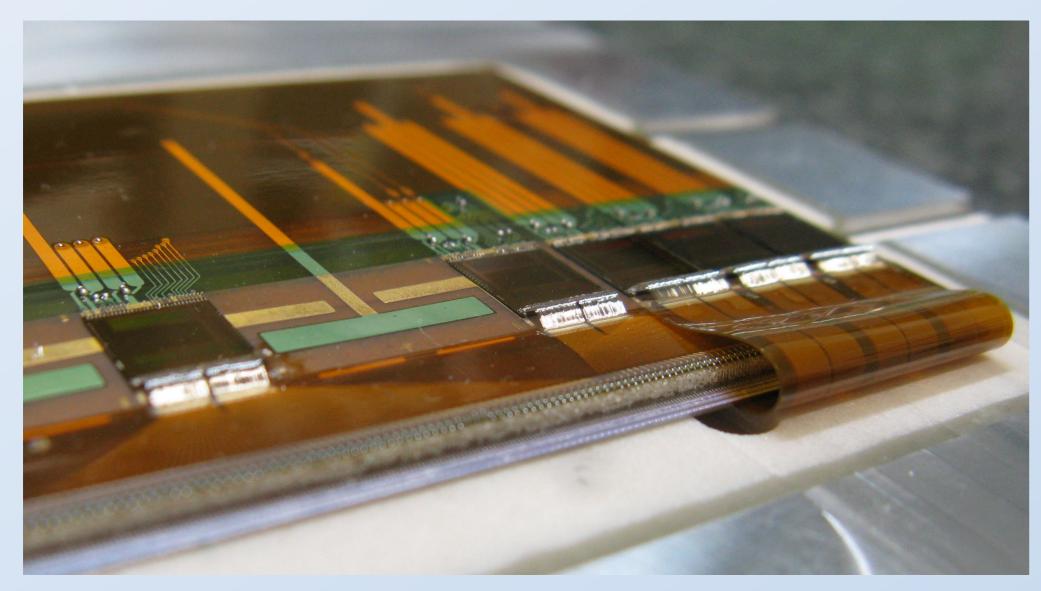
14th Pisa Meeting on Advanced Detectors, from 2018-05-27 to 2018-06-02 Richard Thalmeier (HEPHY Vienna) for the Belle II SVD Group

The Belle II Silicon Vertex Detector



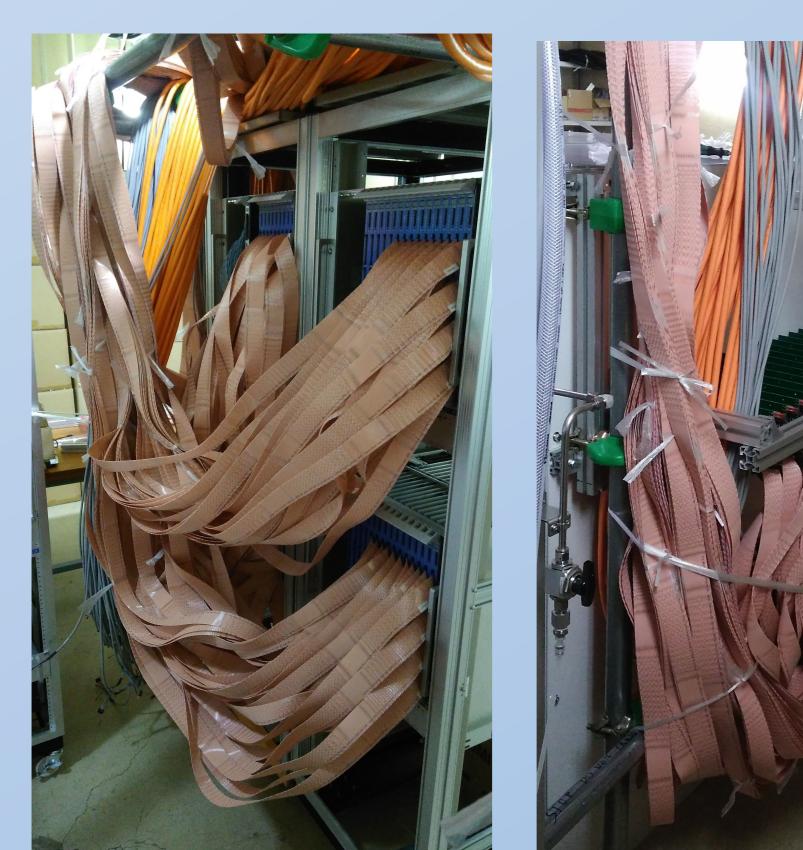


Chip-on-sensor (completed)



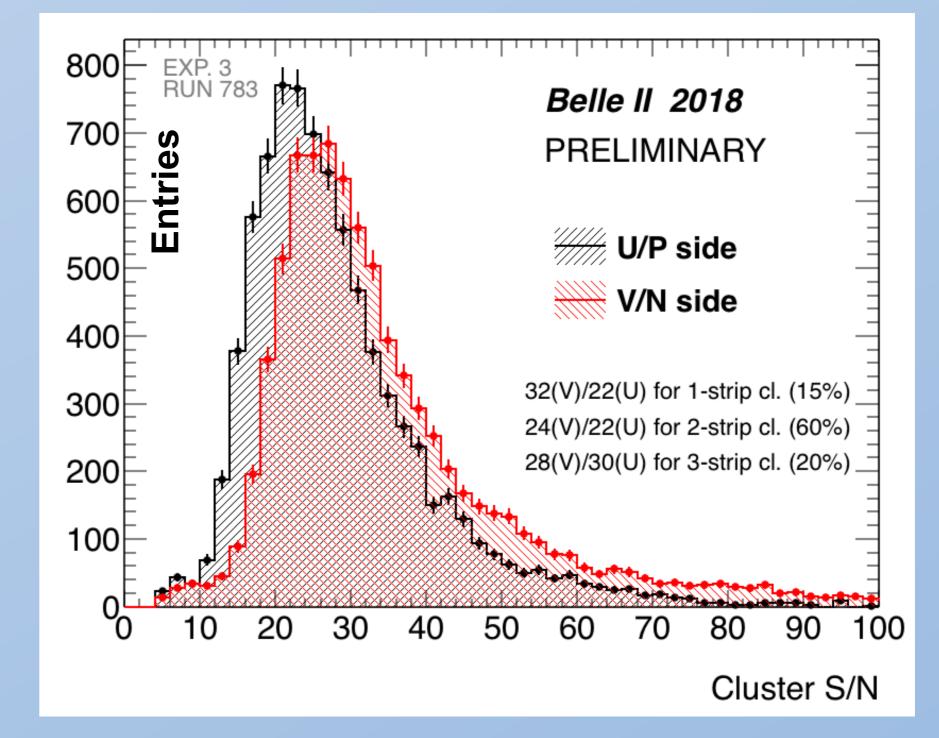
The silicon vertex detector (SVD) is one of the main detectors in the Belle II experiment (KEK, Japan) and plays a crucial role for precise decay-vertex determination and low-momentum-track reconstruction in combination with the pixel detector (PXD). It consists of four-layers of double-sided silicon strip detectors (DSSDs) arranged cylindrically around the Belle II interaction point. Each layer is composed of several DSSD ladders. To operate in the high rate and harsh background environment of Belle II, we employ the APV25 readout ASIC chip characterized by its short shaping time (~50 ns) and high irradiation tolerance (over 1MGy). The most notable feature of the SVD modules is the "chip-on-sensor" concept, which minimizes the distance of the signal propagation from the DSSD strips to the APVs and thus reduces noises from strip capacitance to an acceptable level. Current construction status of SVD: The first half is readily assembled; all components of the second half are finished and being assembled right now. The SVD is expected to be installed in Belle II in fall 2018. First results are obtained during the operation of a reducedscale SVD, installed in Belle II during the ongoing so-called phase 2 commissioning of the detector, the first commissioning of the SuperKEKB accelerator with the final focusing system and data from collisions.

Milestone: First half of SVD

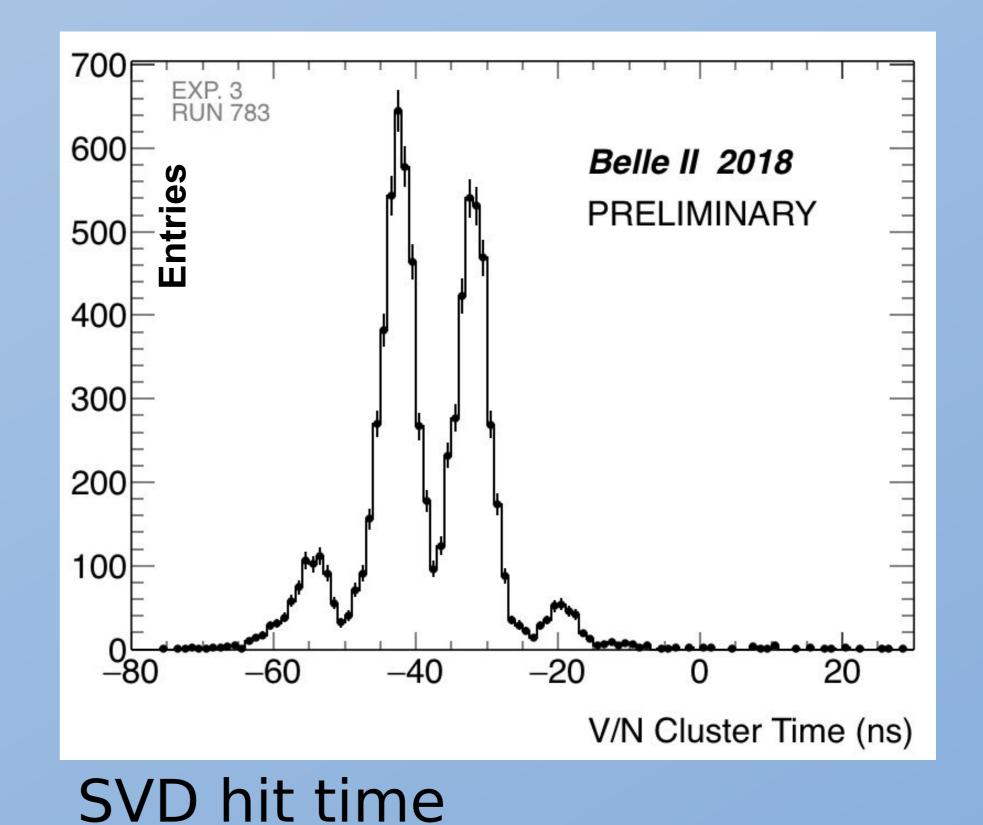


The measured signal-tonoise ratio (S/N) on the first data with tracks of different momentum and inclination matches expectations. design Different S/N for different cluster sizes is observed, most of the clusters are formed by two strips and have a S/N greater than 20, with the Ν side slightly performing better than the P side, as expected.

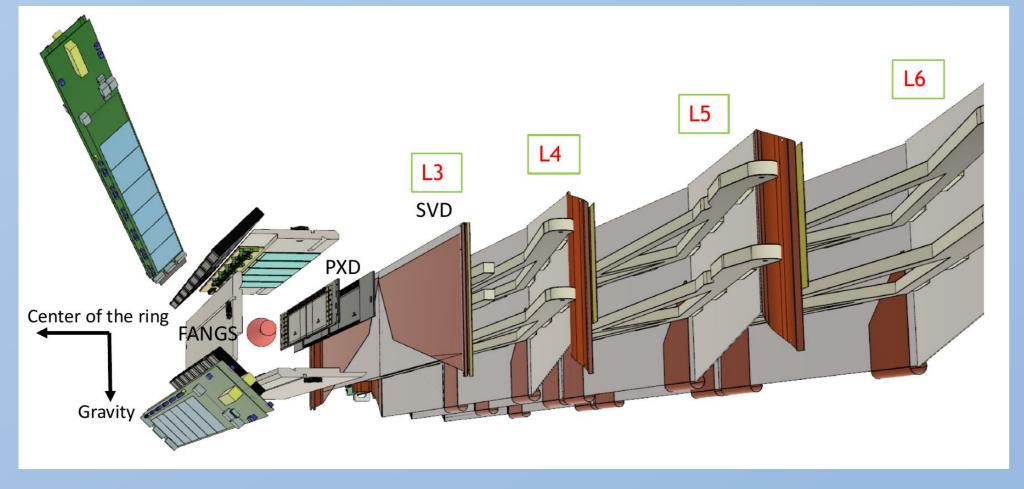
A precise hit time determination is crucial to remove off-time hits from beam background and improve tracking performances. With the first data we have



Signal to noise ratio



SVD readout electronics



Phase 2 setup

demonstrated that the SVD is clearly able to distinguish bunch crossings 16 ns apart. The RMS of cluster times corresponding to a bunch crossing is in the order of 3 ns, nicely matching the design.

