Radiation tolerance characterization of geiger-mode CMOS avalanche diodes for a dual-layer particle detector

M. Musacci [1,6], G. Bigongiari [2,6], P. Brogi [2,6], C. Checchia [3,6], G. Collazuol [3,6], G.-F. Dalla Betta [4,6], A. Ficorella [4,6], P.S. Marrocchesi [2,6], S. Mattiazzo [3,6], F.Morsani [6], S. Noli [1,6], L. Pancheri [4,6], A. Savoy Navarro [5,6], L. Silvestrin [3,6], F. Stolzi [2,6], A. Sulaj [2,6], J. Suh [2,6], L. Ratti [1,6], C. Vacchi [1,6], M. Zanoli [4,6], M. Zarghami [4,6]

marco.musacci01@universitadipavia.it

[1] Università di Pavia

[2] Università di Siena

[3] Università di Padova

[4] Università di Trento

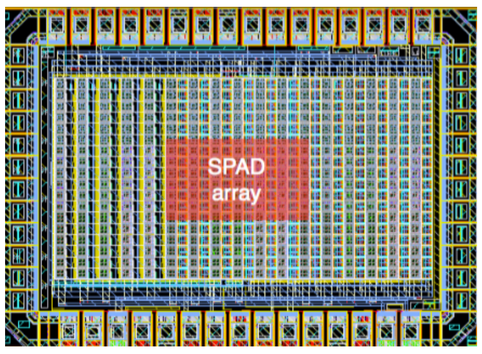
[5] Laboratoire APC, University Paris-Diderot/ CNRS

[6] INFN

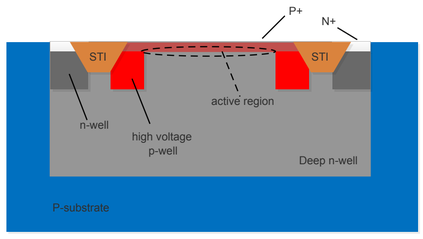
Abstract

A SPAD (Single Photon Avalanche Diode) array, fabricated in a 180 nm CMOS technology with high voltage (HV) option, has been investigated in terms of radiation tolerance in view of the fabrication of a dual-tier detector for charged particles based on the coincidence of signals coming from pairs of vertically aligned pixels. The DUTs (device under test) were irradiated with 10 keV X-rays up to a dose of 1 Mrad(SiO_2) and with neutrons up to 10^{11} cm^{-2}. Both the irradiation and measurement were performed at room temperature. Based on the results from this characterization, a new chip has been designed in a 150 nm CMOS technology in two mirrored versions ready for vertical integration.

Irradiated chip description



- Single layer designed in a 180 nm high voltage CMOS technology.
- 17 columns x 18 rows array.
- The array includes different SPADs with different size and technology layers.
- Different front-end electronics providing an output pulse with programmable duration.
- The pixel includes the readout electronics and the sensor in a monolithic structure.

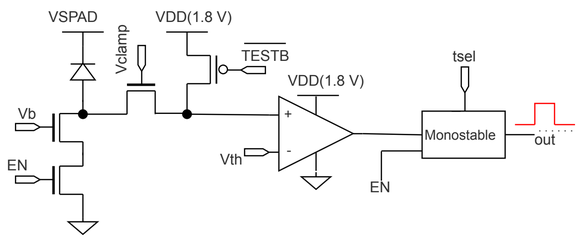


SPADs features

- Diode bias votage : $V_{SPAD} = V_{BD} + V_{EX}$
- Active area with different dimensions:
  - 20 µm x 20 µm,
  - 30 µm x 30 µm,
  - 36 µm x 40 µm.
- Two sensor topologies:
  - DPD (presented in this work),
  - DPH.

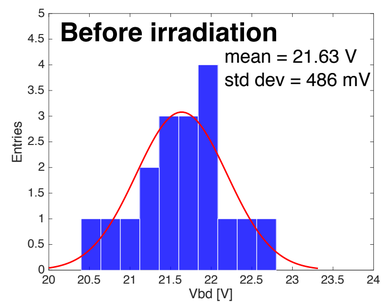
Front-end electronics

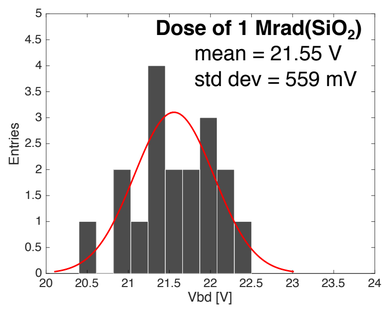
- Passive quenching,
- Active quenching.

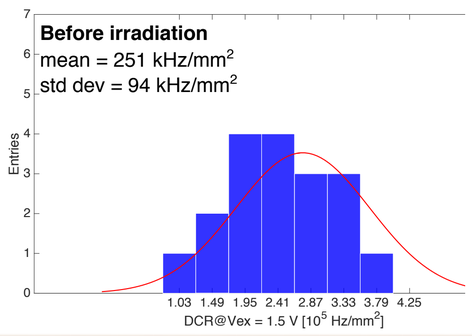


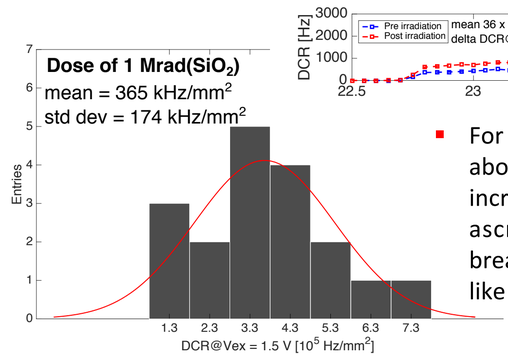
Total ionizing dose effects

- A set of DUTs were exposed to a total ionizing dose of 1 Mrad(SiO_2) using a 10 keV Semiconductor Irradiation System at the Physics and Astronomy Department of the University of Padova
- No significant variations have been measured considering the mean breakdown voltage and standard variation.
- The average dark count rate (DCR) is found to increase by 30%, from 251 kHz/mm² to 365 kHz/mm².

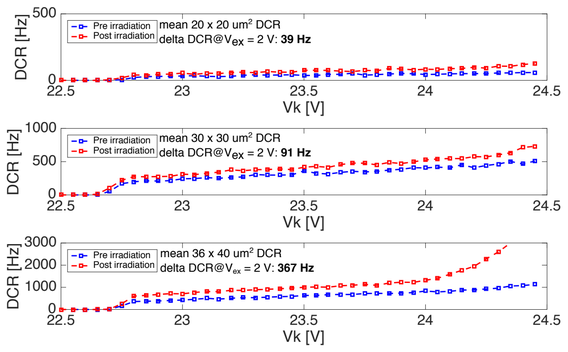








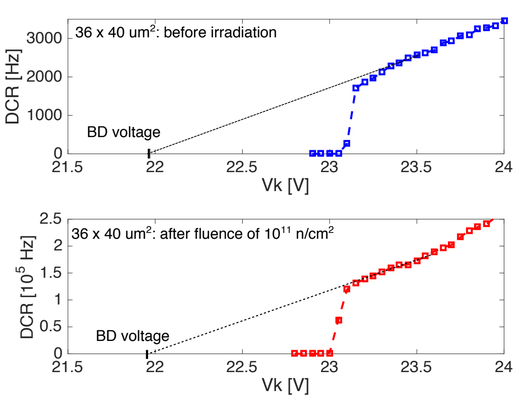
- The higher DCR may be due to a radiation-induced increase in the state density at the interface above the active region.

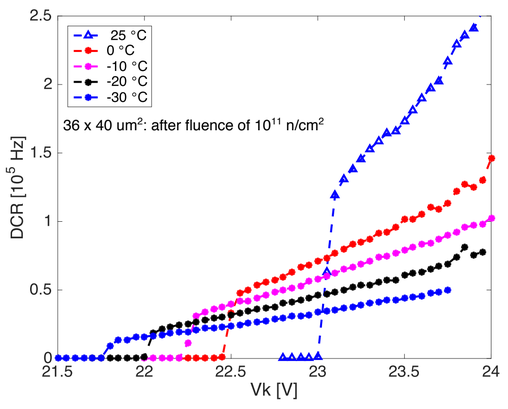


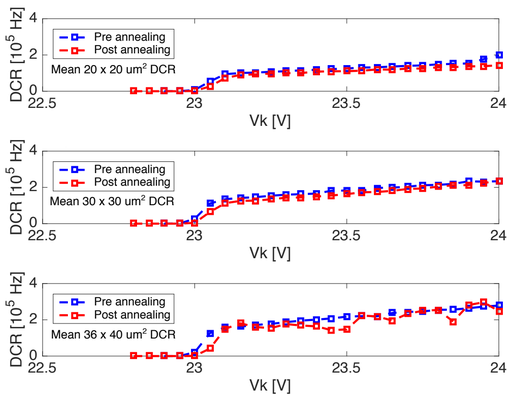
- For the three SPADs dimensions, above 24 V a much marked DCR increase is observed. It may be ascribed to a radiation-induced breakdown in a secondary junction, like the HV P-well/N-well.

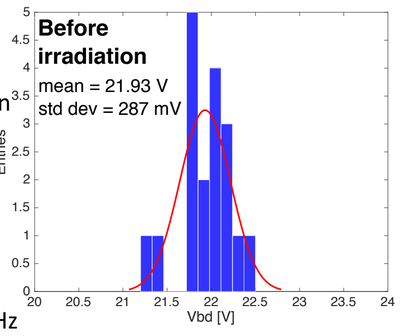
Neutron radiation effects

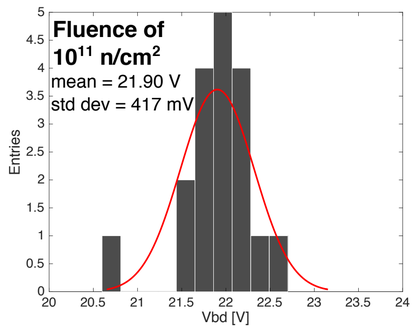
- The test vehicles were irradiated at the INFN Laboratori Nazionali di Legnaro with different fluences (10^{10} n/cm² and 10^{11} n/cm²).
- Both chips have been also measured after an annealing procedure at 60° for 80 minutes.
- Results relevant to irradiation with a fluence of 10^{11} n/cm² are presented.
- No front-end electronics degradation is expected since MOSFET transistors are virtually insensitive to bulk damage.
- No substantial change in the mean BD voltage is detected.
- An increase of a factor of a few hundreds is detected in the mean DCR due to the creation of deep level defects in the depleted region of the detector.
- After the annealing procedure, the mean DCR@V_{ex} = 2 V is found to decrease. In particular, considering the smallest SPAD a reduction by 17% is registered, while the biggest ones shows a reduction by 11%.
- Temperature tests show a reduction both in BD voltage and DCR, as the temperature is decreased, as expected. Mean BD voltage decreases from 22.1 V (at 25°C) to 20.8 V (at -30°C), while the DCR, at V_{EX} = 2 V, is reduced from 229 kHz (at 25°C) to 23.6 kHz (at -30 °C).

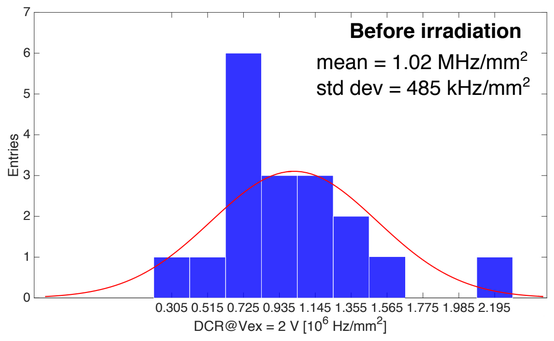


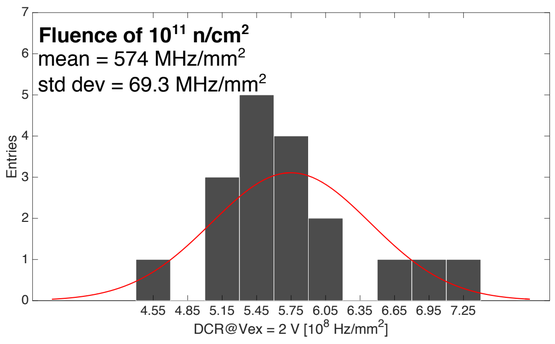




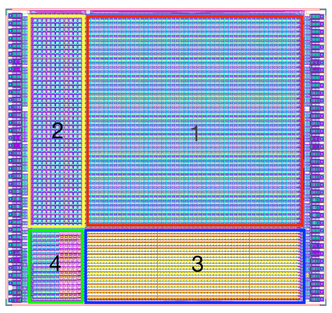


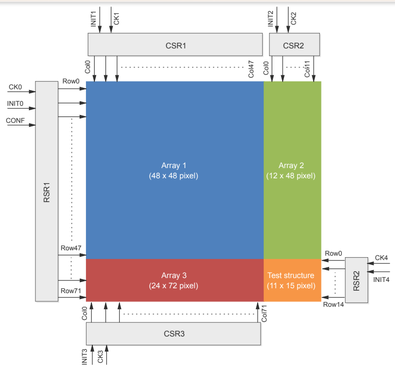




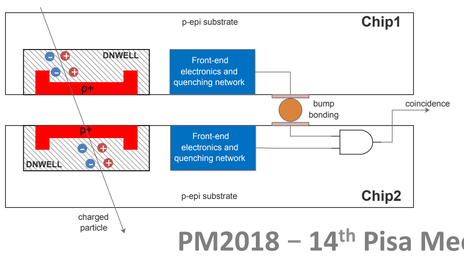


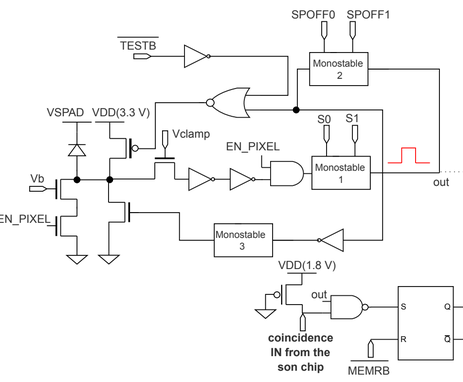
New designed chip features





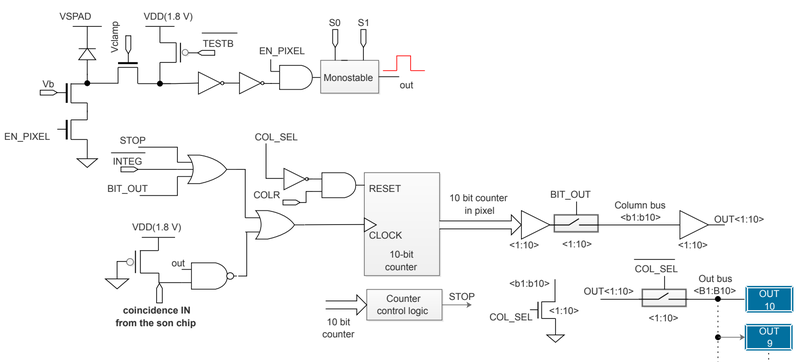
- Two mirrored chips (APiX2 Father and Son) were designed in a standard 150 nm CMOS technology in view of their vertical integration (bump bonding).
- 57 mm² total area (Father + Son) .
- Fill factor improvement, new features for the in-pixel electronics.





Active quenching readout

The sensor can be kept off for a pre-defined time interval by acting on the SPOFF0 and SPOFF1 control bits (from 70 to 130 ns).



- Dedicated shift register for pixel selection.
- **Array1**: 75 µm x 75 µm, 1-bit memory architecture, Fill Factor : 83% .
- **Array2**: 75 µm x 75 µm, 10-bit ripple counter architecture, Fill Factor: 45%.
- **Array3**: 50 µm x 50 µm, 1-bit memory architecture, Fill Factor: 43%.
- **Test structure**: 75 µm x 75 µm, active quenching and 1-bit memory with SPADs featuring different size and technology layers.

Passive quenching with 10-bit ripple counter readout

- Counter state control logic.
- Rolling shutter operation.
- Time window definition for coincidence detection.