Characterization of a depleted monolithic pixel sensor in 150 nm CMOS technology for the ATLAS Inner Tracker upgrade

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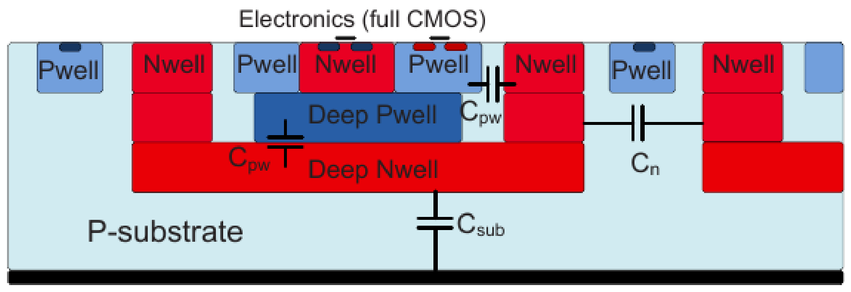
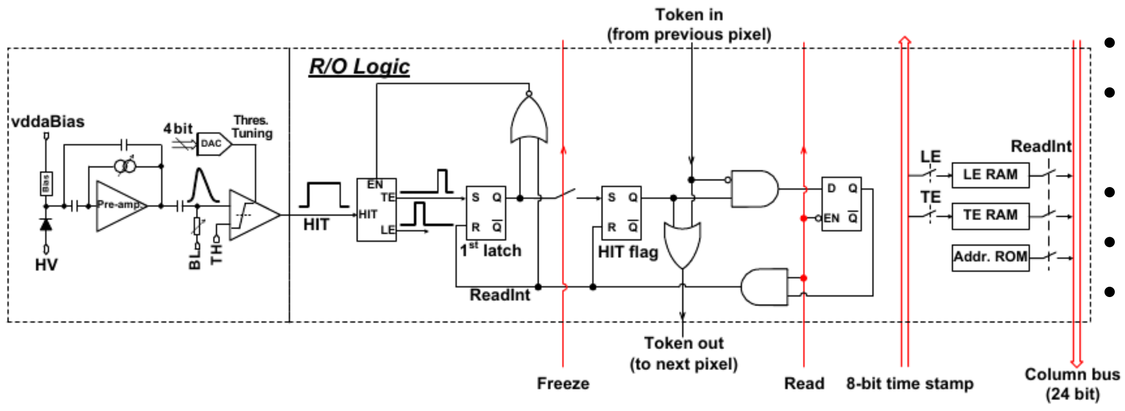
1.- LF-MONOPIX chip: design & pixel configuration



- ***Depleted Monolithic Active Pixel Sensor*** (DMAPS)
- Large collecting well containing all the electronics:
  - High field -> Less trapping -> Radiation hard
  - Large (~400 fF) sensor capacitance -> Noise & speed/power penalty & cross-talk
- ***LFoundry 150 nm HV-CMOS***
- Wafers can be thinned & backside processed
- **Chip size:** 10 mm x 10 mm
- **Pixel size:** 50 µm x 250 µm
- Pixels distributed in 36 columns x 129 rows
- 9 flavors (4 cols each) with different configurations



- Charge sensitive amplifier
- In-pixel 4-bit DAC for threshold trimming
- Hit register (1-bit counter)
- 8-bit timestamp @ 40 MHz
- Full-custom digital circuit (minimized area for less Cp & low noise design)

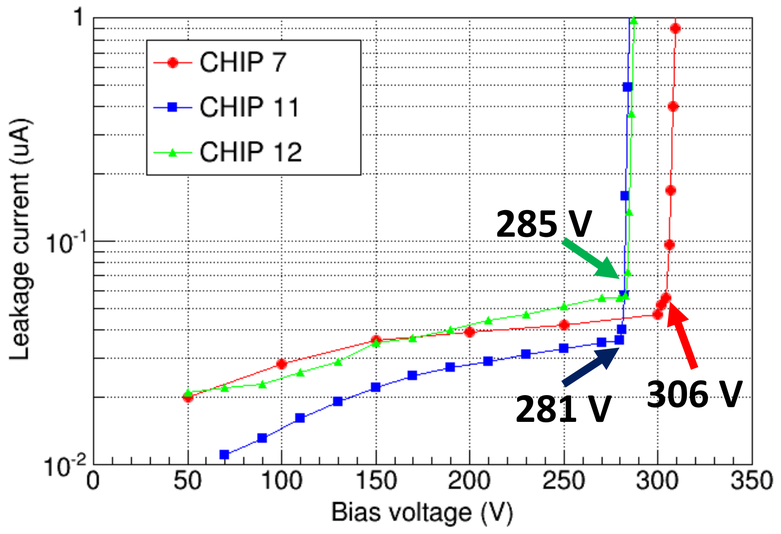
Sub-Array #	0	1	2	3	4	5	6	7	8
R/O Logic	Out	In-Pixel							
Amplifier (CSA)	CMOS							NMOS	
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	
Disc. Domain	Dig	A+D	Dig	A+D					
Token	CMOS		Current Steering						
Source Follower	P	N							

Preamplifiers: NMOS or CMOS-input

Discriminators:

- V1: two stage open-loop structure
- V2: self-biased differential amplifier

2.- Breakdown voltage



3.- Gain & input capacitance

A ^{55}Fe source (5.9 keV x-rays) is used to measure:

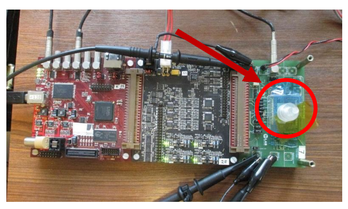
Gain (µV/e-)

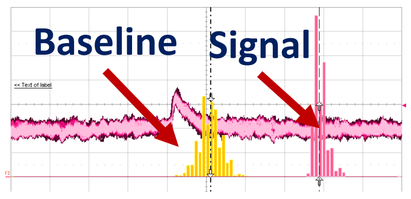
$$G = \frac{\Delta Vout}{1620\ e-}$$

Input capacitance (fF)

$$C_{inj}(F) = \frac{1620\ e-}{V_{inj}\ (V)}\ q_e(C)$$

	CMOS	NMOS	CMOS	NMOS
7	15.9 ± 0.1	12.0 ± 0.1	2.40 ± 0.05	2.82 ± 0.05
12	15.5 ± 0.1	13.0 ± 0.1	2.25 ± 0.06	2.47 ± 0.08



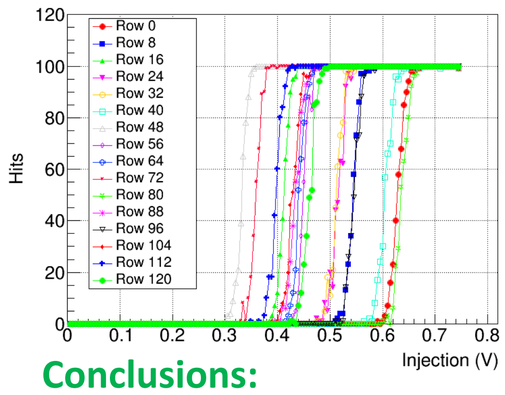


4.- Threshold & electronic noise

Methodology:

- External injection signal scan, recording the probability of pixel firing at V_{th} = 0.795 V.
- Error function fitted to S-curves -> Threshold & noise parameters.

Feature	Type	Untuned	Tuned
Threshold (e-)	V1 discri	2960 ± 150	-
	V2 discri	4290 ± 230	-
Thr. Disp. (e-)	V1 discri	533 ± 45	104 ± 14
	V2 discri	926 ± 89	153 ± 21
Noise (e-)	CMOS	230 ± 17	238 ± 17
	NMOS	193 ± 10	195 ± 13

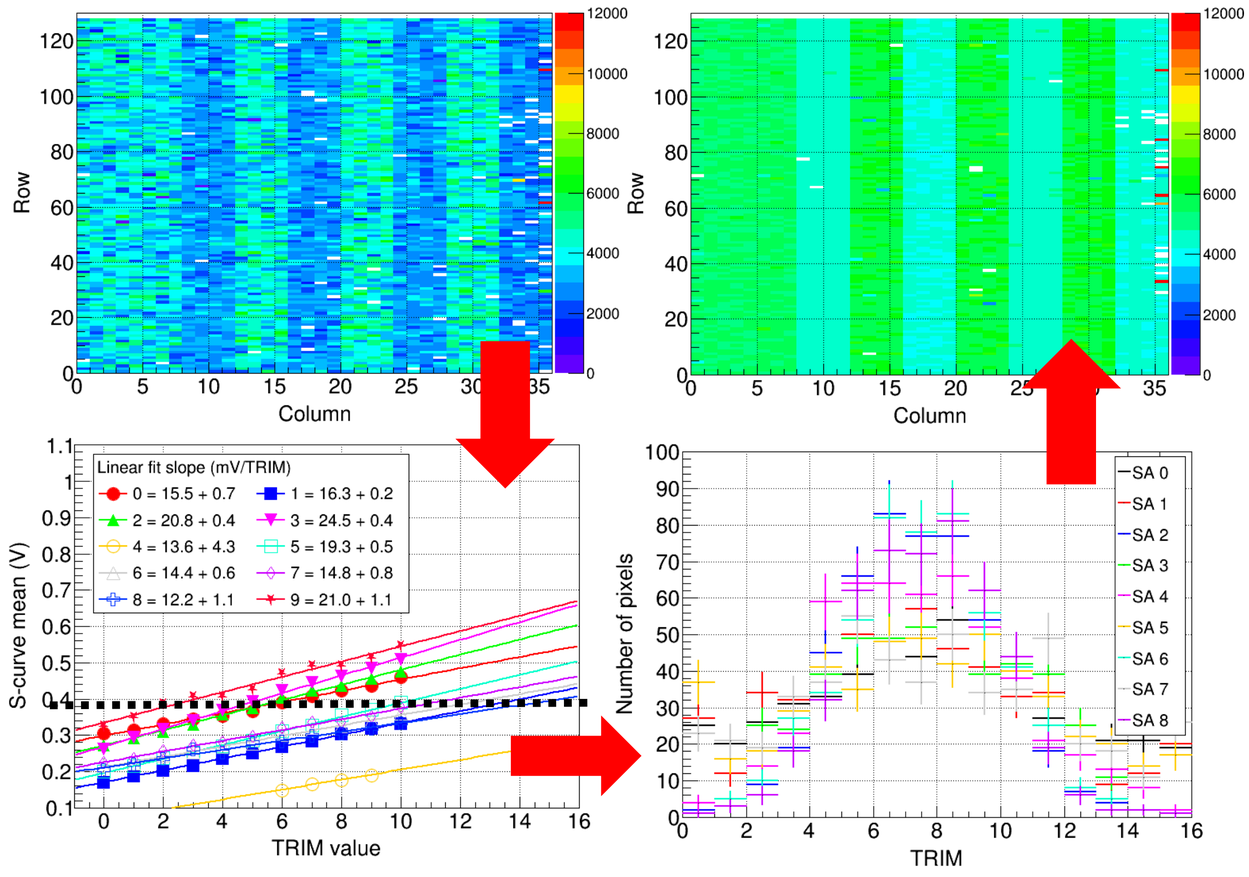


Conclusions:

- Lower threshold & dispersion for V1 discri.
- Less noise for NMOS preamplifier.

5.- Chip threshold tuning

1. Each chip has been scanned for TRIM values between 0 & 11.
2. For each pixel:
   a) Linear function fitted to the dependence of threshold with TRIM.
   b) Linear fit used to get the TRIM value for a common threshold.
3. Chip scan repeated for the tunned TRIM values.



6.- LF-CPIX collaboration

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7.- References

- T. Wang *et al.*, *Development of a Depleted Monolithic CMOS sensor in 150 nm CMOS Technology for the ATLAS Inner Tracker Upgrade*, *JINST* **12** (2017) C01039.
- T. Hirono *et al.*, *CMOS pixel sensors on high resistive substrate for high-rate, high-radiation environements*, *NIM* **A831** (2016) 94-98.