Single Event Upsets in the ATLAS IBL Front End ASICs

- IBL pixel front end chip FE-I4-B in 130 nm technology was designed with Single Event Upset (SEU) hard configuration memory. It is exposed to 92.5 $10^{11}$ cm$^{-2}$/fb$^{-1}$ hadrons with E>20 MeV according to PYTHIA/FLUKA simulations in the LHC 13 TeV pp collision fills with peak luminosities up to $2.1 \times 10^{34}$cm$^{-2}$s$^{-1}$.
- Inside the pixels Dual Interlocked Cell (DICE) latches were used with SEU cross-section measured for FE-I4-A in the 24 GeV proton test beam is $1.1 \times 10^{-15}$ cm$^{-2}$.
- SEU upsets in the global and local pixel configuration memory were observed during LHC fills: module desynchronization, dead modules, quiet pixels, noisy pixels.
- ATLAS Pixel detector with IBL at R=3.3 cm efficiently operates at high luminosity with expected SEUs.
- Global configuration SEUs mitigated by refreshing the memory during ECR every 5 seconds without dead time.
- Plans to introduce the gradual refreshing of Local pixel configuration during ECR in 2018.
- Local pixel memory SEUs in the enable bit and 1->0 transitions in TDAC and FDAC are consistent with test beam results.
- SEUs with 0->1 transitions in local TDAC and FDAC are five times higher than test beam results. Probably due to Single Event Transients (SET) glitches.

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