Active-edge FBK-INFN-LPNHE thin n-on-p pixel sensors for the upgrade of the ATLAS Inner Tracker

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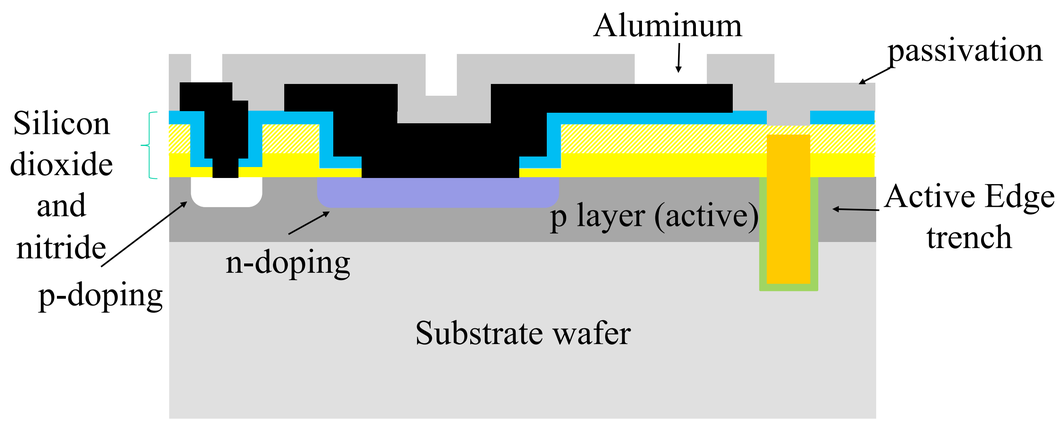
Abstract - In view of the LHC upgrade for the High Luminosity (HL-LHC), the ATLAS experiment plans to replace the Inner Detector with an all-silicon system. The n-on-p silicon technology is a promising candidate to achieve a large area instrumented with pixel sensors, since it is radiation hard and cost effective. The paper reports on the performance of 100 and 130 um thick n-in-p planar pixel sensors produced by FBK-CMM. After discussing the sensor technology, an overview of 2017 and 2018 beam-test results of the produced devices will be given, before and after irradiation, including new results for hit and charge collection efficiency and space resolution. Preliminary beam-test results for the new 2017 thin edgeless productions at FBK-CMM will be also presented, with a special focus on the hit efficiency at the detector edge and a new feature in the design consisting in staggered deep trenches.

The Device

PLANAR ACTIVE EDGE SENSORS

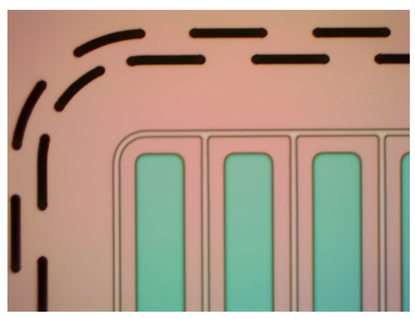


Schematic cross-section of planar active-edge sensor using Si-Si Direct Wafer Bonded substrate.

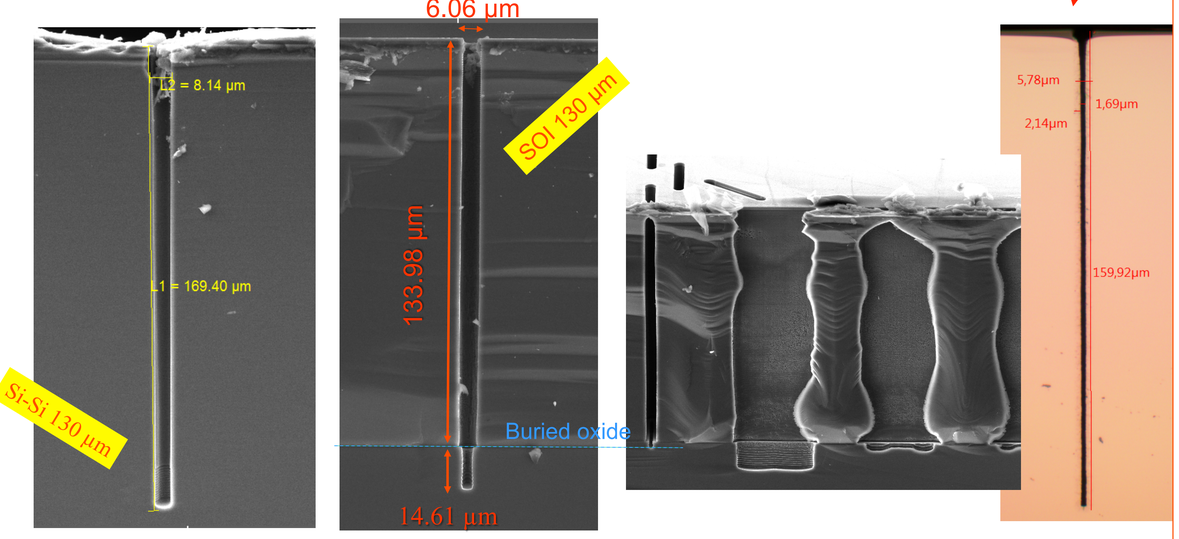
"STANDARD" planar n-on-p process + TRENCH

- Isolation by p-spray
- 3 different substrates:
  - Si-Si 130µm active thickness depth
  - Si-Si 100µm active thickness depth
  - SOI 130µm active thickness depth

TRENCHES OPTIMIZATION

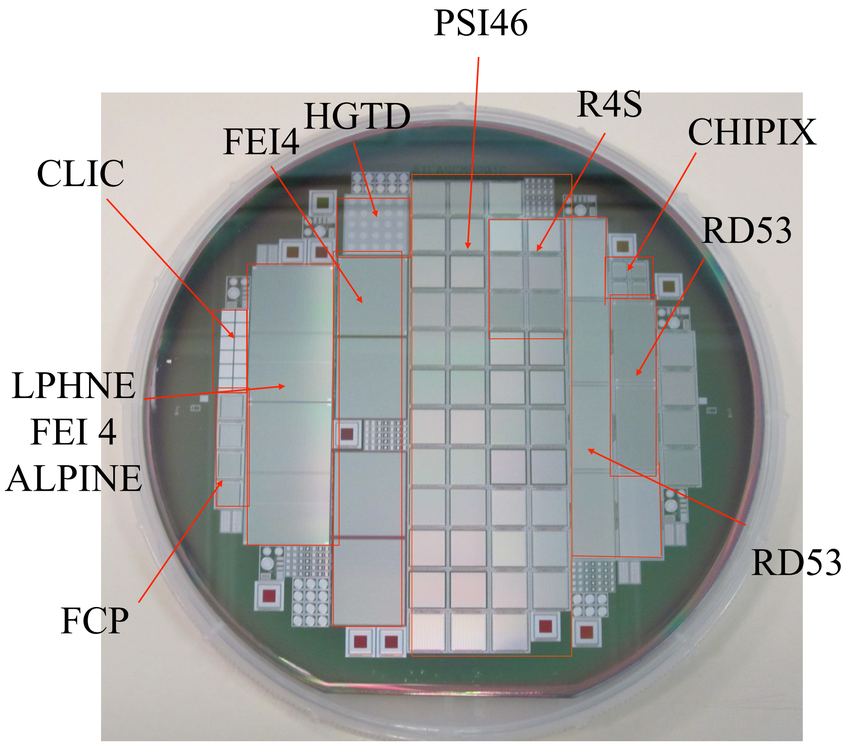


- Layout based on "staggered" trench
- A series of 5µm wide and 40µm long "small" trenches
- Trench depth 10µm deeper than Active Thickness
- Trench partially filled with undoped poly
- Trench doped via BBr_3 gas source



ActiveEdge batch pictures

THE WHOLE WAFER



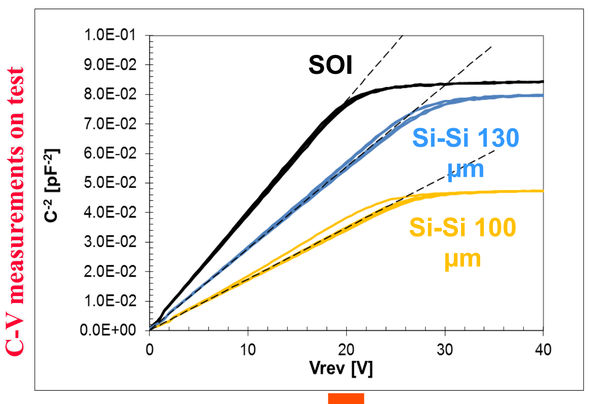
WAFER LAYOUT

- FE-I4
- Alpine
- PSI
- R4S
- RD53
- CLIC
- CHIPIX
- FCP
- MGS
- HGTD

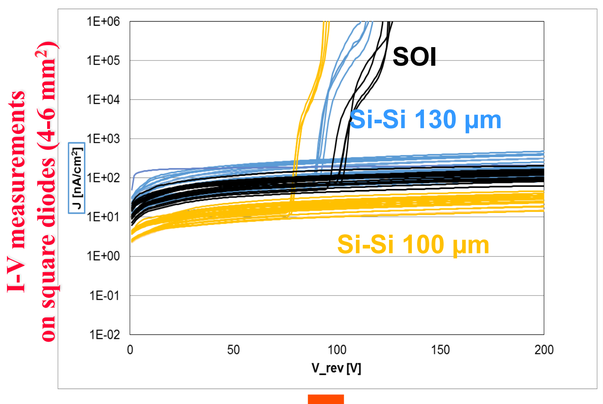
Many design variations

- FE chips
- Guard ring
- Distance between trenches and pixels\guard ring

FIRST ELECTRICAL CHARACTERIZATION



Depletion voltages:
- V_{depl} ~ 30V for 130 µm thick
- V_{depl} ~ 26V for 130 µm thick
- V_{depl} ~ 21V for 130 µm thick SOI



Breakdown voltage typically larger than 200V
Very aggressive design:
0-1-2 guard rings (0-1 for active edge)
Distance from the pixel to the trench of 60 to 80 µm

Electrical results

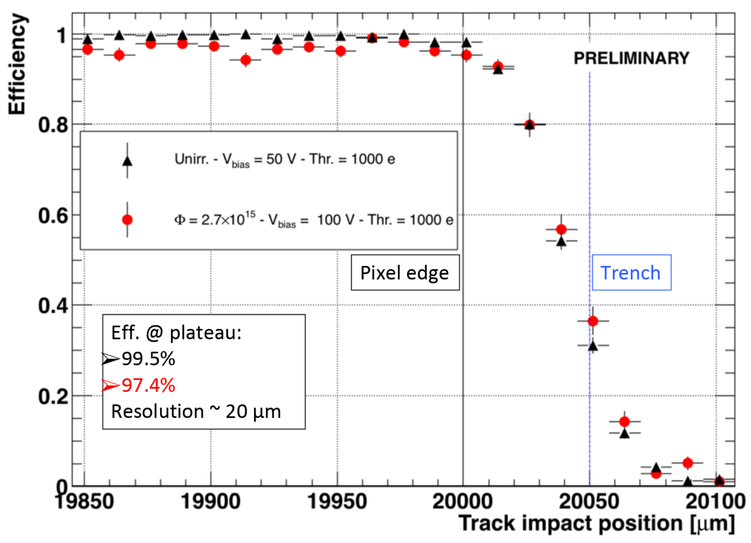
Performance and beam test analysis

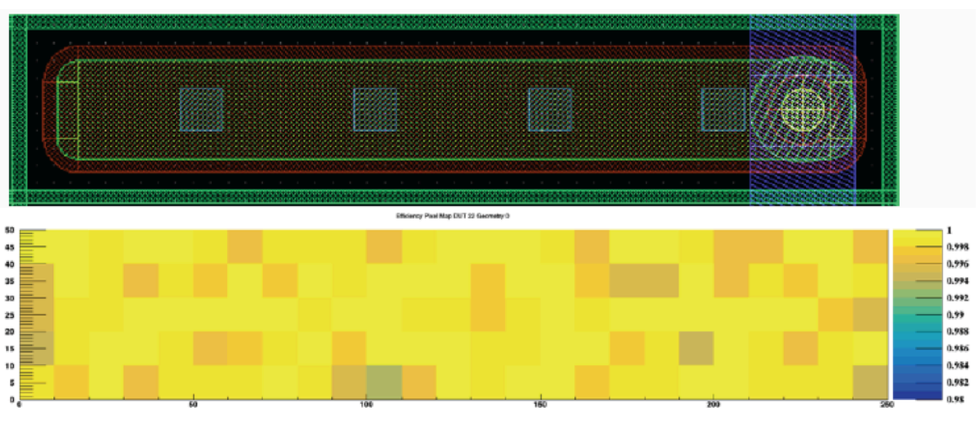
EFFICIENCY BENCHMARKS

Hit efficiency measured as function of the position with beam test at DESY before and after irradiation with protons at 2.7 x 10^{15} n_{eq} / cm^2

Still significant hit efficiency even in the region between the last row of pixels and the trench

Above the pixel implant, the hit efficiency decreases from 99% to O(97%) after irradiation (measured at 100V bias voltage)



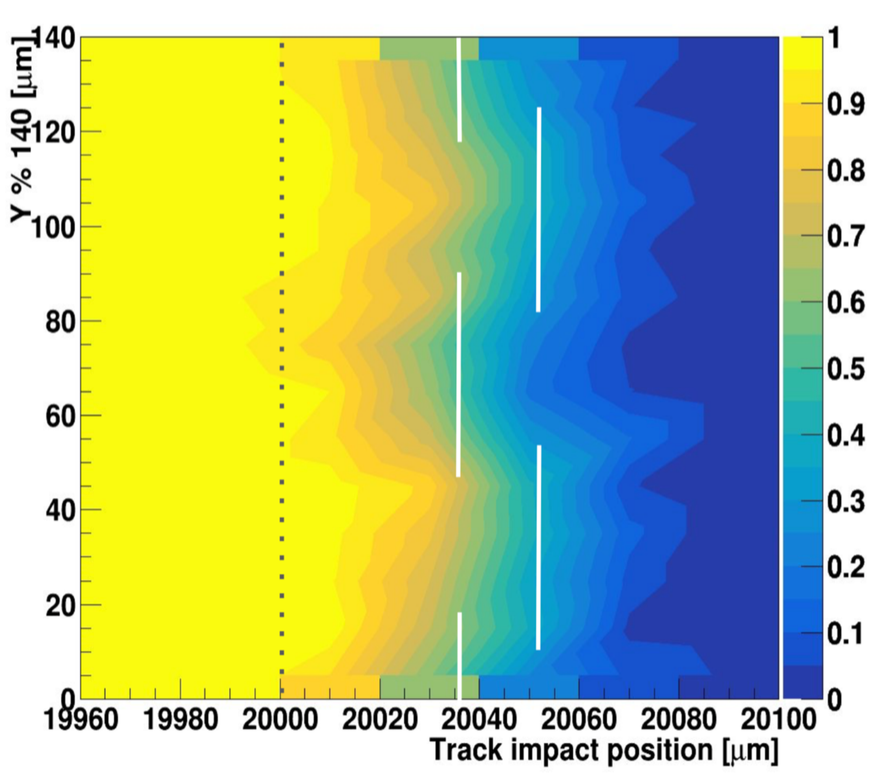


Very uniform in-pixel efficiency

No special effect at the borders of the pixel or in the region of the bump pad

FBK temporary metal technology used

BEHAVIOR OF STAGGERED TRENCH



Hit efficiency in the region of the trench.

The efficiency follows the profile of the staggered trench