Development of the radiation hard high-speed monolithic "MALTA" CMOS sensor for the ATLAS ITk outer pixel layer

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ATLAS ITk Pixel Detector

- All silicon design to replace present ATLAS Inner Detector for HL-LHC
- η coverage increased from 2.5 to 4
- 1M Pixel: 5 pixel barrel layers and 5 pixel rings
- 10,000 modules with 12-14 m² of pixel detectors
- Design of the pixel part is being finalized: inclined layout optimization

TowerJazz 180nm Investigator

First Irradiation tests for HL-LHC

TowerJazz 180nm Investigator sensor with small electrodes
Neutron irradiated at Triga reactor Slovenia
Measure charge collection before and after irradiation

Investigator Efficiency after irradiation

- 50x60μm pixel pitch, 3μm electrode 40μm opening
- Efficiency after neutron irradiation to 10¹⁴ n/cm²

Radiation hard CMOS sensors

Advantages over "classic" n-in-n/p-in-p sensors or traditional Monolithic Active Pixel Sensors (MAPS)
- Full CMOS allows complex electronics in active area of pixel matrix
- Thin and high-resolution trackers
- Large depleted volume increases sensitivity and provides efficient detection after irradiation

ATLAS CMOS Development Collaboration

- 25 institutes – RD on radiation hard CMOS sensors since 4 years
- Monolithic CMOS sensors are developed as option for the outermost ITk Pixel Barrel layer

- CMOS is much higher volume and lower price than our present silicon sensors due to high volume and larger wafers
- CMOS Modules costs = factor ~3 less than hybrid (no bumpbonding, no extra FE-chip)

TJ180nm CMOS Process Modification

- Novel modified process developed in collaboration of CERN with TJ foundry, originally developed in context of ALICE ITS
- We carried out initial charge collection studies at HL-LHC radiation levels (×10¹⁴ n/cm²) to study a possible application towards ATLAS ITk

TJ MALTA for ATLAS

Lead design: CERN
Received chip back in January 2018

- Monolithic pixel sensor for the outer layers of the ATLAS 1k Pixel outer layer
- Uses TJ180nm modified process
- Full-scale demonstrators with different readout architectures and optimized analog performance
  - MALTA: 512x512 pixel matrix 20x22 mm² (full size)
  - MonoPix : 20x10 mm² (half size) see presentation by K. Moustakas
- The ATLAS "MALTA" chip
  - Novel asynchronous readout architecture for high hit rate capability with 40bit parallel data bus for streaming
  - Features Sensor-to-Sensor high-speed signal transmission
  - Chip-to-Chip power distribution
  - Front-end output injected into double-column digital readout logic
  - Hits are stored using in-pixel flip-flops and transmitted asynchronously over high-speed buses to the end-of-column logic (digital periphery)
  - No clock distribution over the active matrix – reduces power consumption!
  - Double-column divided into groups of 2x8 pixels ("red" and "blue")
  - Buses shared by all groups of the same colour in the double-column
  - Group number encoded on 5-bit bus for streaming

- Charge collection electrode separated from circuitry to avoid additional noise from cross-talk
- Small diameter electrode (3μm diameters) to achieve minimal capacitance (<5fF)
- Analog power: bias current 500nA/pixel or <70nW/cm²

First measurements on TJ MALTA sensor

S-curve measurement shows expected low noise level (signal rise time 25ns)

Hitmap of the chip with a 90Sr source
Uniform response on all sectors

ΦFe source amplitude spectrum
Measured on analog monitoring pixels

Novel asynchronous readout architecture for high hit rate capability with 40bit parallel data bus for data streaming