Development of the radiation hard high-speed monolithic ``MALTA" CMOS sensor for the ATLAS ITK outer pixel layer

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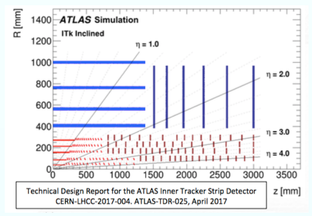
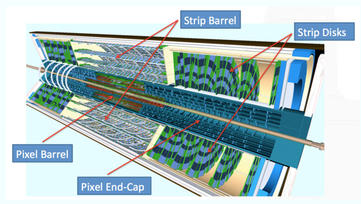
ATLAS ITk Pixel Detector



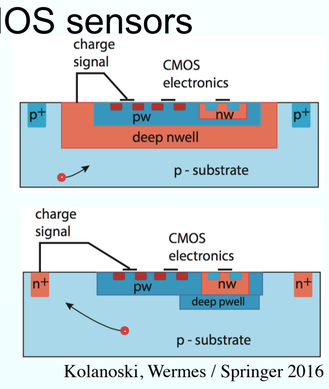


- All silicon design to replace present ATLAS Inner Detector for HL-LHC
- η coverage increased from 2.5 to 4
- Itk Pixel: 5 pixel barrel layers and 5 pixel rings
- 10,000 modules with 12 -14 m^2 of pixel detectors
- Design of the pixel part is being finalized: inclined layout optimization

Radiation hard CMOS sensors

Advantages over "classic" n-in-n/n-in-p sensors or traditional Monolithic Active Pixel Sensors (MAPS)

- Full CMOS allows complex electronics in active area of pixel matrix
- Thin and high-resolution trackers
- **Large depleted volume increases sensitivity and provides efficient detection after irradiation**



Kolanoski, Wermes / Springer 2016

ATLAS CMOS Development Collaboration

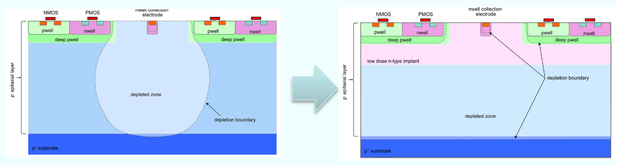
- 25 institutes – RD on radiation hard CMOS sensors since 4 years
- Monolithic CMOS sensors are developed as option for the **outermost ITK Pixel Barrel layer**

- CMOS is much higher volume and lower price than our present silicon sensors due to high volume and larger wafers
- CMOS Modules costs ~ factor ~3 less than hybrid (no bumpbonding, no extra FE-chip)

TJ180nm CMOS Process Modification

- Novel modified process developed in collaboration of CERN with TJ foundry, originally developed in context of ALICE ITS
- We carried out initial charge collection studies at HL-LHC radiation levels (~$10^{15} n_{eq}/cm^2$) to study a possible application towards ATLAS Itk

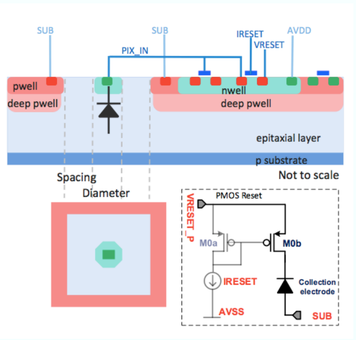
W. Snoeys et al. DOI 10.1016/j.nima.2017.07.046



Adding **a planar n-type layer** significantly improves depletion under deep PWELL

- Increased depletion volume → **fast charge collection by drift**
- Possibility to fully deplete sensing volume with no significant circuit or layout changes

TowerJazz 180nm Investigator



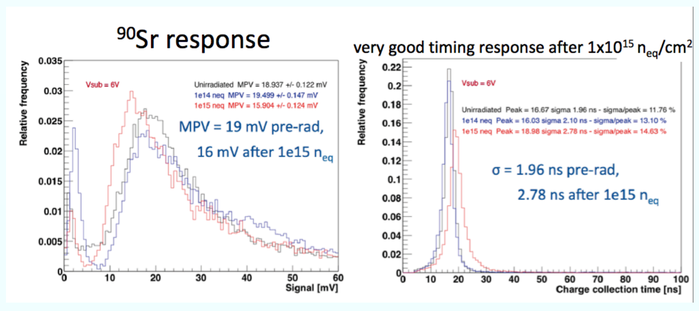
C. Gao et al., NIM A (2016) 831

- **Pixel dimensions for these measurements:**
- 20x20 to 50x50μm pixel size
- **3 um diameter electrodes** TJ180nm on >1kΩ 25μm EPI layer

Designed as part of the ALPIDE development for the ALICE ITS upgrade **Emphasis on small electrodes and small capacitance enables low analog power designs with low noise and fast response**

First Irradiation tests for HL-LHC

TowerJazz 180nm Investigator sensor with small electrodes
Neutron irradiated at Triga reactor Slovenia
Measure charge collection before and after irradiation



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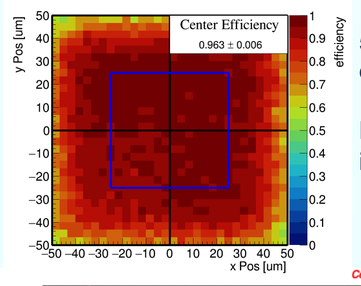
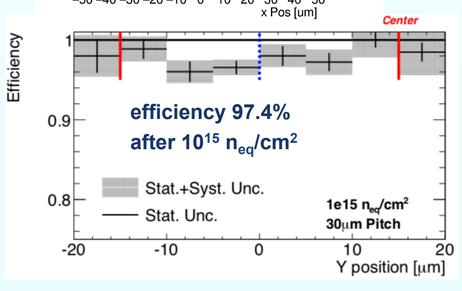
Investigator Efficiency after irradiation



50x50μm pixel pitch, 3μm electrode 40μm opening

Efficiency after neutron irradiation to **10^{15} n_{eq}/cm^2**

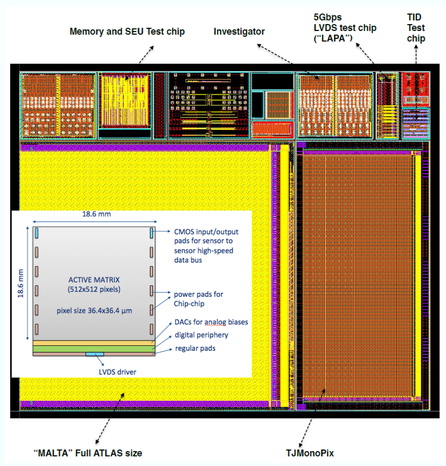


30x30μm pixel pitch, 3μm electrode 9μm opening

Good efficiency after irradiation
-> **crucial question**

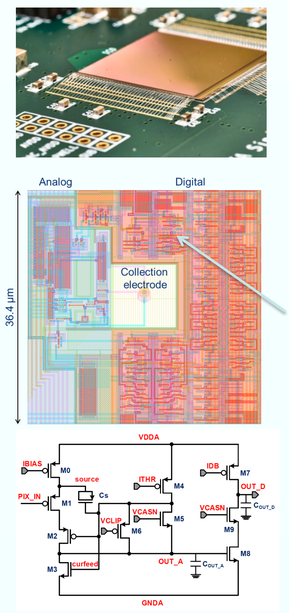
TJ MALTA for ATLAS

- **Monolithic pixel sensor for the outer layers of the ATLAS Itk Pixel outer layer**
- Uses TJ180nm modified process
- **Full-scale demonstrators** with different readout architectures and optimized analog performance
  - MALTA: 512x512 pixel matrix 20x22 mm^2 (full size)
  - MonoPix : 20x10 mm^2 (half size) see presentation by K. Moustakas
- **The ATLAS "MALTA" chip**
  - **Novel asynchronous readout** architecture for **high hit rate** capability with 40bit parallel data bus for streaming
  - Features Sensor-to-Sensor high-speed signal transmission
  - Chip-to-Chip power distribution



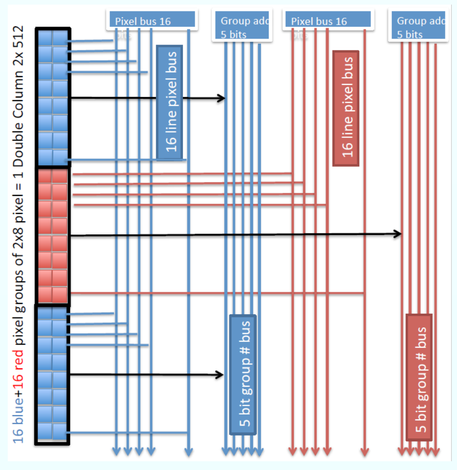
Lead design: CERN

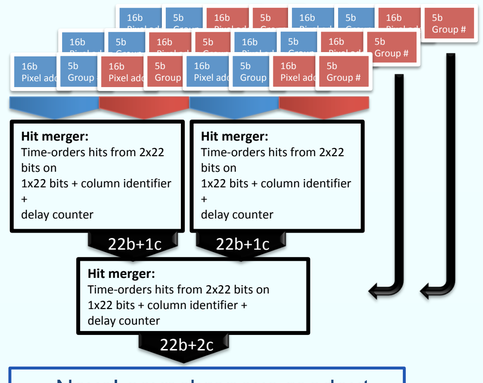
Received chip back in January 2018



- Charge collection electrode separated from circuitry to avoid additional noise from cross-talk
- Small diameter electrode (3μm diameters) to achieve minimal capacitance (<5fF)
- Analog power: bias current 500nA/pixel or <70mW/cm^2

- Front-end output injected into double-column digital readout logic
- Hits are stored using in-pixel flip-flops and **transmitted asynchronously over high-speed buses to the end-of-column logic** (digital periphery)
- **No clock distribution** over the active matrix **– reduces power consumption**!
- Double-column divided into groups of 2x8 pixels ("red" and "blue")
- Buses shared by all groups of the same colour in the double-column
- Group number encoded on 5-bit group address bus

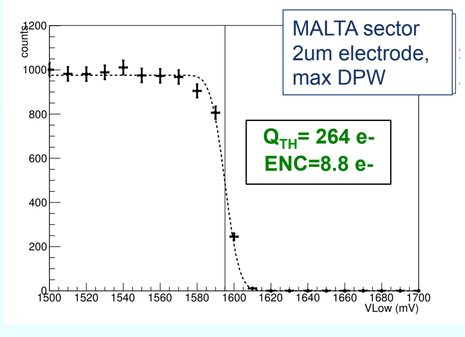




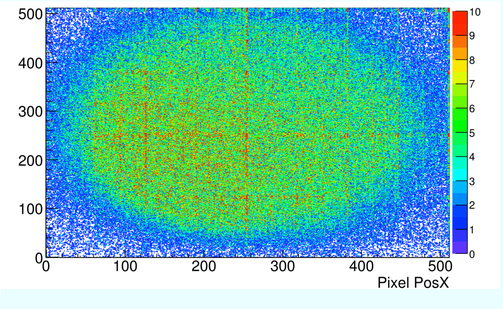
Novel asynchronous readout architecture for high hit rate capability with 40bit parallel data bus for data streaming

First measurements on TJ MALTA sensor

S-curve measurement shows expected low noise level (signal rise time 25ns)



Hitmap of the chip with a ^{90}Sr source
Uniform response on all sectors



^{55}Fe source amplitude spectrum
Measured on analog monitoring pixels