Silicon Photomultiplier Detector with Multipurpose In-Pixel Electronics in Standard CMOS Technology

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Introduction
An array of single photon avalanche diodes (SPADs) has been designed in a commercial 350 nm high-voltage CMOS (AMS 350nm) process. This monolithic detector includes active quenching and readout electronics. The SPAD consists of a p+ diffusion/n-well junction surrounded by a shallow p-well acting as guard ring to prevent breakdown. The electrical signal generated by the avalanche effect is directly DC coupled to a fast CMOS comparator. The active quenching has an inhibition and reset transistor. On this poster measurements of breakdown voltage, dark count rate, surface scan and efficiency measurement are presented.

H35-SiPM ASIC
- Geometry:
  - 15 x 20 Pixels
  - SPAD size: 38 x 92 μm²
  - Chip size: 2.8 x 2.6 mm²
  - 24.3 % geometric SPAD fill factor
- Main Features:
  - Vertical and horizontal control logic
  - Fast comparator
  - Active quenching circuit (reset and inhibition)
  - Edge detection
  - Monostable circuit
  - 1-bit hit flag
  - Analog time stamp memory
  - Hit-OR bus

Pixel Architecture
- Sensor Architecture
- Matrix Readout
- Front-End Electronics
- DC SPAD Signal

Measurement Setup
- Readout System
  - Different readout modes were developed: single pixel readout and full matrix readout. An FPGA is used to configure the ASIC and detect the hit pulses from the sensor. With a special application the chip can be configured and a readout mode is selectable. Dark count map and a hit map were implemented. The ASIC is mounted on a dedicated test board.

Breakdown Voltage Measurement
- Voltage Breakdown
  - The breakdown voltage values have been determined from the current-voltage (I-V) characteristics. Using a precision source/meter unit, f=20 Hz A. A breakdown voltage of 11.7 V was measured at 24.0 °C for a SPAD pixel size of 3496 μm².

Dark Count Rate Measurement
- Dark Count Rate
  - At 32.0 V (oversupply 0.40V) a dark count rate of 850 kHz per pixel was measured.
  - This rate corresponds to 174 Hz/μm². It was observed that the DCR is weakly dependent on temperature. The trap-assisted band-to-band tunneling is responsible for the generation of free charge carriers.

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