Advanced Through Silicon Vias for Hybrid Pixel Detector Modules

**Pixel Module Concept using TSV**
- More compact hybrid pixel detector modules with active area maximization, no wire-bonds, and 4-side attachable
- Deploy via-last TSVs into the readout chips IO Pads to bring all IOs (power, slow control, high speed readout) to the chip's backside
- Usage of the chip backside for wiring and absorb some functionality of the module flex PCB into the Redistribution Layer (RDL)
- Integrate the fine pitch bump bonding process on thin, large chips into post processing of the readout wafers

**Main goals**
- Establish high yield TSV + RDL process for hybrid pixel modules
- Straight side vias through ultra thinned readout wafers with 2x2 cm² chip size
- Target wafer thickness of 80 - 100 µm with via diameter of 60 µm

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**ATLAS FE-I4 TSV Run**

**Frontside processing**
- UBM deposition on the wafer front side with 25 µm bump pads on 50 µm pitch
- Bonding of the wafers onto carrier
- Thinning to 80 - 100 µm of the wafers

**TSV formation processing**
- Silicon etching of TSV until oxide between bulk and BEOL
- Oxide etching between Si bulk and poly-Si
- Poly silicon etching
- Insulation (PE-CVD)

**TSV filling and RDL formation processing**
- TSV filling with Cu liner filling process
- RDL formation on wafer backside
- Deposition of RDL and UBM pad metallization
- Processing of three ATLAS FE-I4 wafer
- Completing process with no problems and good visual inspection results
- Wafer backside with TSVs connected via the RDL side, photo taken from a previous production.

**Functional Testing of TSV Pixel Modules**
- Bare chips with TSVs and RDL are mounted on dedicated support cards allowing wire-bond connection from both chip sides
- Chips can be operated from the backside or via RDL
- Individual characterization of TSV properties possible for some un-used TSVs
- Chips are currently prepared for first electrical tests

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**TSV Processing Steps**

Process developed by Fraunhofer IZM
1. Underbump Metallization (UBM) on wafer front side
2. Wafer thinning: Bonding to carrier wafer and grinding and deep reactive ion etching (DRIE)
3. TSV Silicon Etching: DRIE-BOSCH Process
4. TSV Insulation: Plasma-enhanced chemical vapour deposition (PE-CVD)
5. Adhesion/Barrier + Seed-Layer: Ti and highly ionised physical vapour deposition (Hi-PVD) of Cu
6. TSV Filling: Electrochemical deposition (ECD) of Cu, liner filling
7. Redistribution Layer (RDL) and UBM pad metallization
8. Release of carrier wafer, cleaning of wafer frontside, dicing

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**Results of TSV test structures**

- Several TSV test structures for resistance, capacitance measurements and daisy chains with 168 TSVs implemented on setup wafers
- Single TSV resistance measured to be 14 - 15 mΩ
- Passivation breakdown measured to be >40 V for a varying passivation layer thickness of 1000 - 500 nm
- Daisy chain and capacitance measurements ongoing

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**References**

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