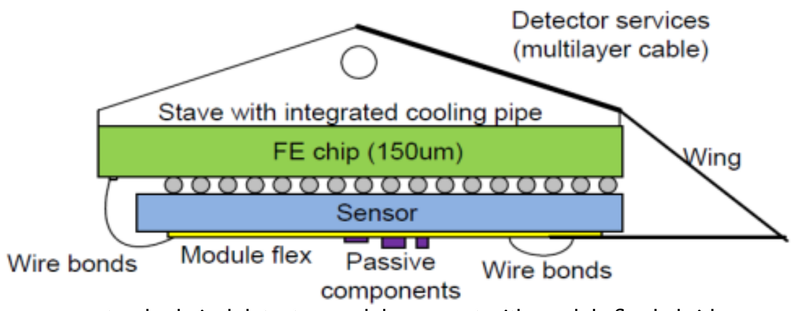
Advanced Through Silicon Vias for Hybrid Pixel Detector Modules

Pixel Module Concept using TSV

- More compact hybrid pixel detector modules with active area maximization, no wire-bonds, and 4-side abuttable
- Deploy via-last TSVs into the readout chip's IO Pads to bring all IOs (power, slow control, high speed readout) to the chip's backside
- Usage of the chip backside for wiring and absorb some functionality of the module flex PCB into the Redistribution Layer (RDL)
- Integrate the fine pitch bump bonding process on thin, large chips chip into post processing of the readout wafers

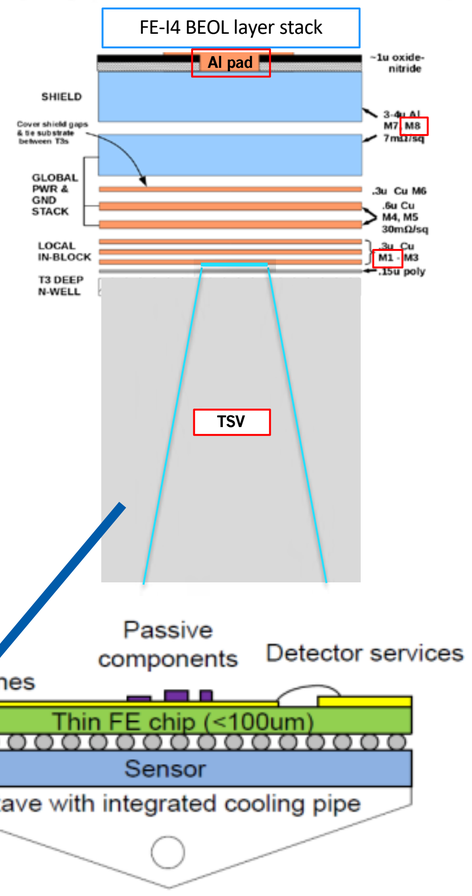
Main goals

- Establish high yield TSV + RDL process for hybrid pixel modules
- Straight side vias through ultra thinned readout wafers with 2x2 cm^2 chip size
- Target wafer thickness of 80 - 100 µm with via diameter of 60 µm



standard pixel detector module concept with module flex hybrid

post process via-last TSV on FE-I4 wire bond pad



pixel detector module concept with TSV

ATLAS FE-I4 TSV Run

Frontside processing

- UBM deposition on the wafer front side with 25 µm bump pads on 50 µm pitch
- bonding of the wafers onto carrier
- thinning to 80 - 100 µm of the wafers

TSV formation processing

- silicon etching of TSV until oxide between bulk and BEOL
- oxide etching between Si bulk and poly-Si
- poly silicon etching
- oxide etching between poly-Si and M1 BEOL Cu
- TSV insulation

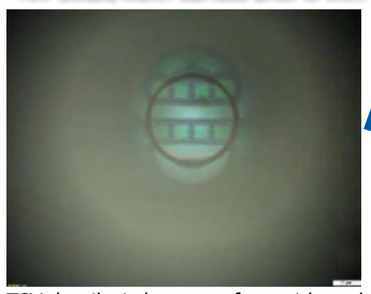
TSV filling and RDL formation processing

- TSV filling with Cu-liner filling process
- RDL formation on wafer backside
- passivation layer deposition and opening
- probe- and wire-bond pad formation with Ni/Au deposit

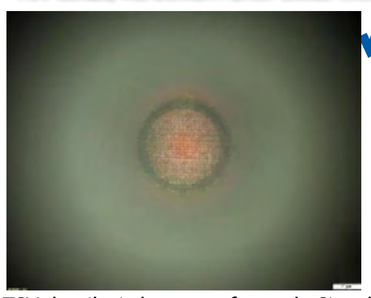
Processing of three ATLAS FE-I4 wafer

- Processing completely finished with no problems and good visual inspection results
- Wafers are cut and first chips are prepared for electrical testing and flip chipping with sensors

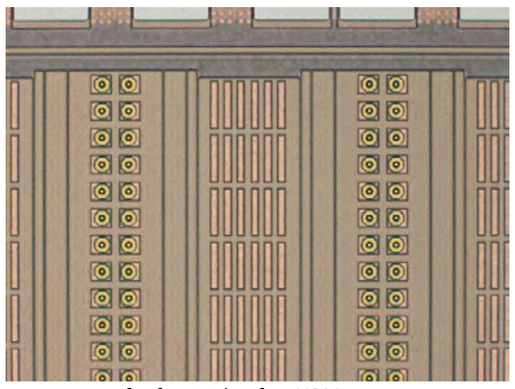
TSV detail, wafer surface after Si etch



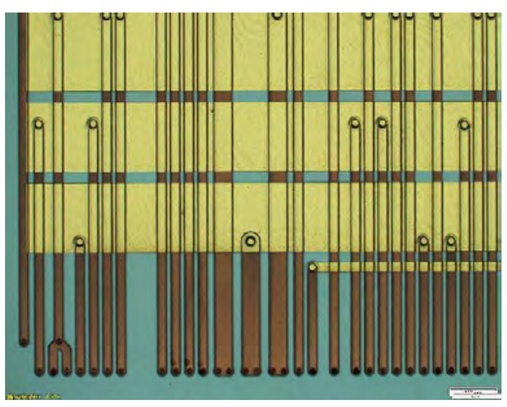
TSV detail, via bottom after oxide etch



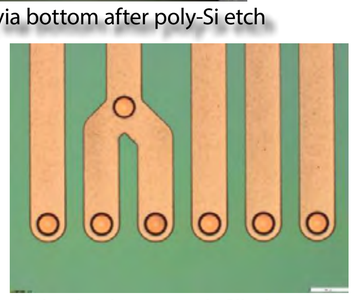
TSV detail, via bottom after poly-Si etch



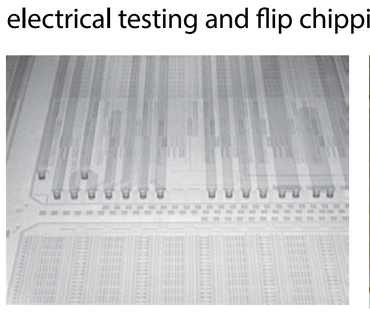
wafer frontside after UBM process



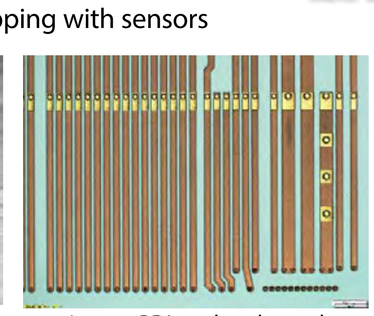
wafer backside after RDL + UBM pad process



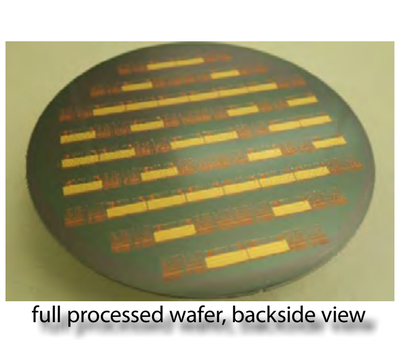
backside RDL with filled TSVs



Cu TSV filling X-ray check



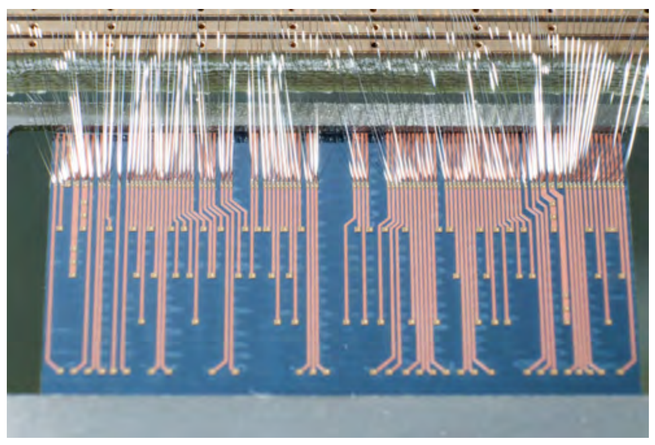
view on RDL and probe pads



full processed wafer, backside view

Functional Testing of TSV Pixel Modules

- bare chips with TSVs and RDL are mounted on dedicated support cards allowing wire-bond connection from both chip sides
- chips can be operated from frontside or via RDL and TSV from the backside
- individual characterization of TSV properties possible for some un-used TSVs
- chips are currently prepared for first electrical tests



ATLAS FE-I4 chip with TSVs connected via the RDL side, photograph taken from a previous prototype

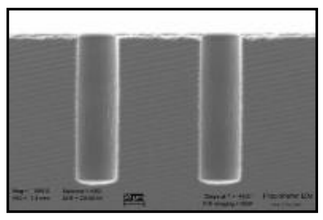
TSV Processing Steps

Process developed by Fraunhofer IZM

1. Underbump Metallization (UBM) on wafer front side
2. Wafer thinning: Bonding to carrier wafer and grinding and deep reactive ion etching (DRIE)
3. TSV Silicon Etching: DRIE-BOSCH Process
4. TSV Insulation: Plasma-enhanced chemical vapour deposition (PE-CVD)
5. Adhesion/Barrier + Seed-Layer: Ti and highly ionised physical vapour deposition (HI-PVD) of Cu
6. TSV Filling: Electrochemical deposition (ECD) of Cu, liner filling
7. Redistribution Layer (RDL) and UBM pad metallization
8. Release of carrier wafer, cleaning of wafer frontside, dicing

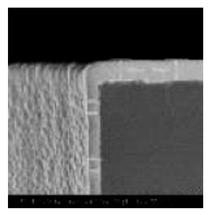
Thinning of wafers (step 2)

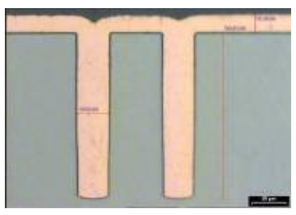
© DISCO

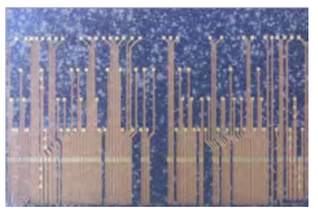


Etching of TSVs from wafer backside (step 3)

TSV insulation and via filling (steps 4, 5, 6)



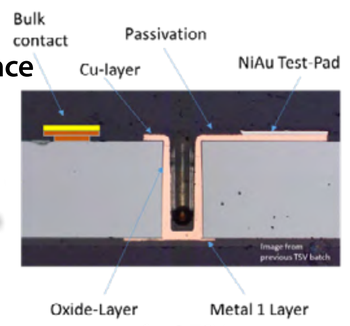




Deposition of RDL and pad metallization (step 7)

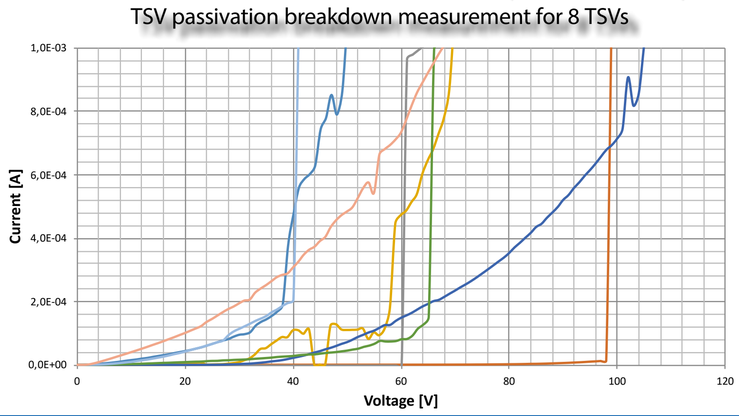
Results of TSV test structures

- several TSV test structures for resistance, capacitance measurements and daisy chains with 168 TSVs implemented on setup wafers
- Single TSV resistance measured to be 14 - 15 mΩ
- Passivation breakdown measured to be >40 V for a varying passivation layer thickness of 1000 - 500 nm (top to bottom)
- Daisy chain and capacitance measurements ongoing



TSV test structure for capacitance and insulation measurements integrated on setup wafers

TSV passivation breakdown measurement for 8 TSVs



Fabian Hügging, N. Owtscharenko, D.-L. Pohl, N. Wermes - Physikalisches Institut - University of Bonn
T. Fritzsch, O. Ehrmann, H. Oppermann, M. Rothermund, Piotr Mackowiak, Kai Zoschke - Fraunhofer IZM Berlin

UNIVERSITÄT BONN

Fraunhofer IZM

SI LAB Silizium Labor Bonn

AIDA 2020