Application of Silicon Photomultiplier Model to the Design of Front-End Electronics

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Introduction

Designer of the front-end electronics for the silicon photomultipliers (SiPM) should take into account unique characteristics of this photodetector. The performance of the front-end should not diminish or distort the qualities of photodetector such as e.g. its timing performance. That is why, there is the need to create an electrical model of SiPM, that in particular would emphasize on the equivalence capacitance of the detector and the shape of the output pulse produced in response to an incident photon. The paper presents a model of the SiPM that has been created based on the parameters of chosen photodetectors and its application in designing a specific integrated circuit (IC).

Front-end ASIC

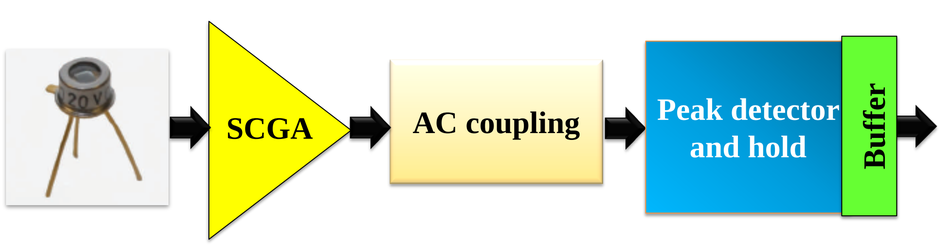

Figure 1. Flowchart of the designed front-end ASIC

The design precondition of the multi-channel prototype ASIC was a basic, space-saving architecture. Single channel of the integrated circuit consists of a super-common gate amplifier followed by AC coupling with a DC level shifter and a peak detector and hold (Figure 1). AC separation is a basic pulse shaping technique. It introduces the undershoot of the signal. Level shifter was required to match the output range of the amplifier to the peak detector's input range.

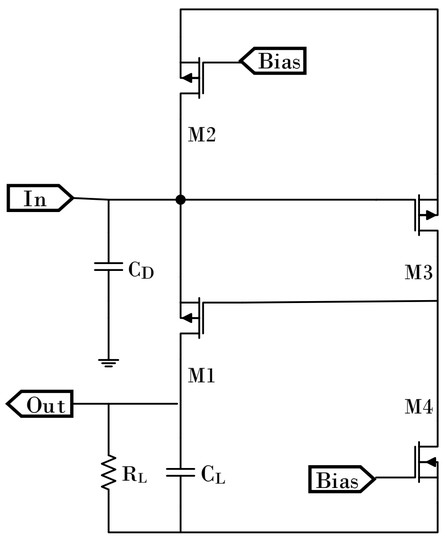

Figure 2. Schematic of a super common gate amplifier for the SiPM

An input stage of the ASIC is an active cascode (super common gate) with M1 as the input transistor and M3 placed in its feedback (Figure 2). This architecture is widely used especially in particle physics designs. The amplifier has small input impedance. Preamplifiers based on common gate configurations are adequate in measurement of high charge pulses (from hundreds of fC up to pC). Current mode provides higher speed of the amplifier however, it also introduces higher noise compared to the voltage mode. SiPM with its large internal charge multiplication proves to be suitable for this type of architecture.

Electrical model of a silicon photomultiplier

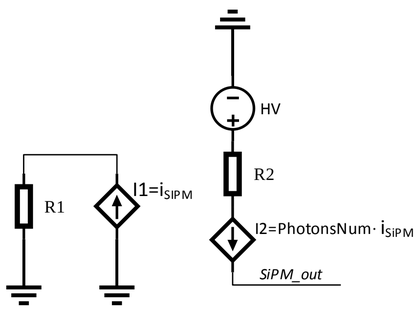

Figure 3. Model of a SiPM designed in PSpice environment. The current source I1 is an exponential current source. I2 is a current controlled current source

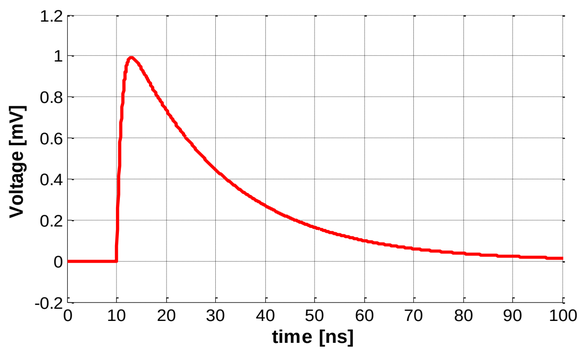

Figure 4. Voltage signal of the PSpice SiPM's model measured on 50 Ω resistor connected to ground

In the Pspice simulations the SiPM equivalent circuit consists of an exponential current source (Figure 3). The current source I1 generates the charge corresponding to a single photon. Then the current controlled current source I2 is used to generate the charge corresponding to any number of photons. Figure 4 presents the voltage output generated by the model on the 50 Ω resistor connected to ground. The amplitude corresponding to a single photon is equal to 1 mV. The pulse has a short rising time and a long, exponential decay. The design precondition for the model was a rising edge of several ns and a falling edge of about 50 ns (baseline restores after about 100ns). The rising edge for the PSpice model is equal to 1.57 ns and the falling edge 44 ns.

Simulation and measurement results

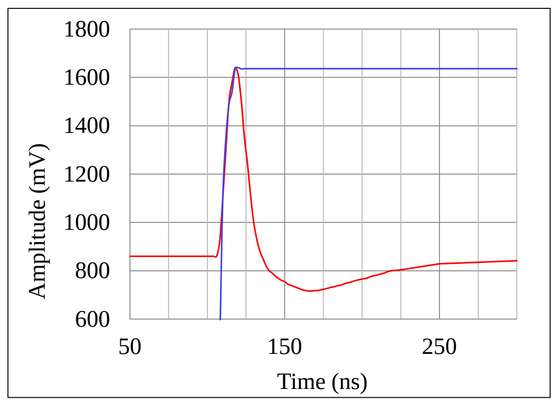

Figure 5. Output signals generated during Hspice simulation of the ASIC with SiPM's model connected to the input. Signal of the super-common gate amplifier (red) and peak detector and hold (blue) originated from the detection of 11 photons.

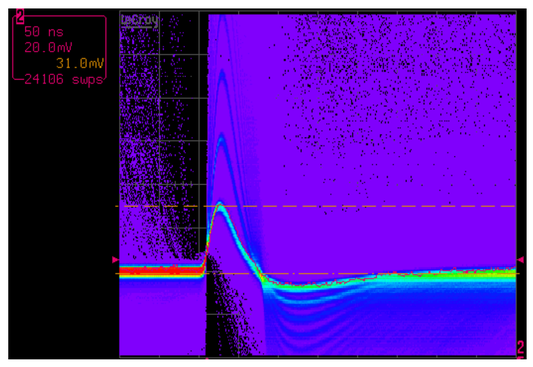

Figure 6. Output signal of the super-common gate amplifier measured on the oscilloscope. The SiPM used in the measurement is Hamamatsu S12571-100C

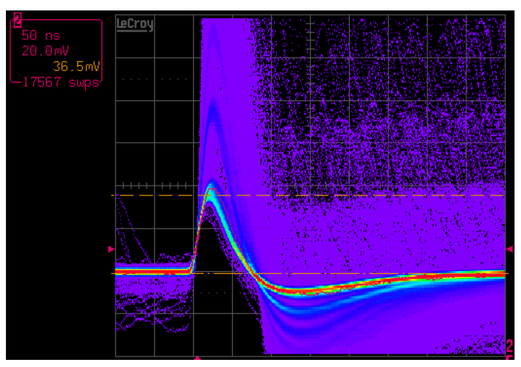

Figure 7. Output signal of the super-common gate amplifier measured on the oscilloscope. The SiPM used in the measurement is SensL 10035 Micro C series

Figure 5 presents the output signals from SCGA and PDH of the designed ASIC with the SiPM's equivalent circuit connected at the input. The reset of the PDH ends at 100 ns and peak detector immediately follows the pulse's amplitude. Amplitude of the signal acuiqred during a simulation of the schematic corresponds to 57 mV for a single photo-electron (output of the amplifier). Simulation of ASIC's layout with extracted parasitic elements returns 35 mV for a single photo-electron (1 p.e.).

The response of the amplifier was also measured with the use of SiPMs from two manufacturers (Figure 6 and 7). Both SiPMs have 100 µm pixel size. The amplitude of the output signal of amplifier measured with Hamamatsu detector is equal to 31 mV for 1 p.e. The same measurement with SensL returns 36.5 mV. Similar comparison between simulation and measurement was performed for the peaking time of the amplifier's response when a SiPM is connected to the input.

The peaking times (Tpeak) recorded in the successive steps of the design process are collected in Table 1. C_d represents the internal capacitance of the SiPM. The peaking time obtained during Hspice simulation with SiPM equivalent model and schematic of the ASIC is presented in "SiPM model – Schematic" column. Afterwards, the IC has been extracted and the simulation has been extended with the contribution of the parasitic capacitances (SiPM model - Extracted). The SiPMs used in measurements had following capacitances: 40 pF (Hamamatsu S12571-100C) and 100 pF (SensL 10035 Micro C).

C_d [pF]	T_{PEAK} (SiPM model - Schematic) [ns]	T_{PEAK} (SiPM model - Extracted) [ns]	T_{PEAK} (Measurement) [ns]
0	8.3	9.6	-
5	10	11.2	-
10	11.6	12.8	-
15	12.7	14.1	-
20	13.8	15.3	-
25	14.7	16.3	-
30	15.4	17.2	-
35	16	18	-
40	16.9	18.8	22
100	22	24.9	26

Table 1. Simulation and measurement values of the output signal's peaking time

Conclusions

- Equivalent electrical model of the silicon photomultiplier was succesully used in the design process of the ASIC. Based on the comparison between Hspice simulation and measurement it can be concluded that the SiPM's electrical model represents the physical device well. The comparison was conducted taking into account the amplitude and rising time of amplifier's output signal.
- Amplitudes obtained in response to single photo-electron: 57 mV (simulation of the schematic), 35 mV (simulation of the layout with parasitics), 36.5 mV and 31 mV (measurement of the SiPM attached to the input of the ASIC)
- The peaking time in response to a single photo-electron: 18.8 ns (simulation 40 pF) - 22 ns (measurement 40 pF) and 24.9 ns (simulation 100 pF) - 26 ns (measurement 100 pF).

Acknowledgment

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Reference

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