Development of a silicon drift detector system for the TRISTAN project - Future search for sterile neutrinos

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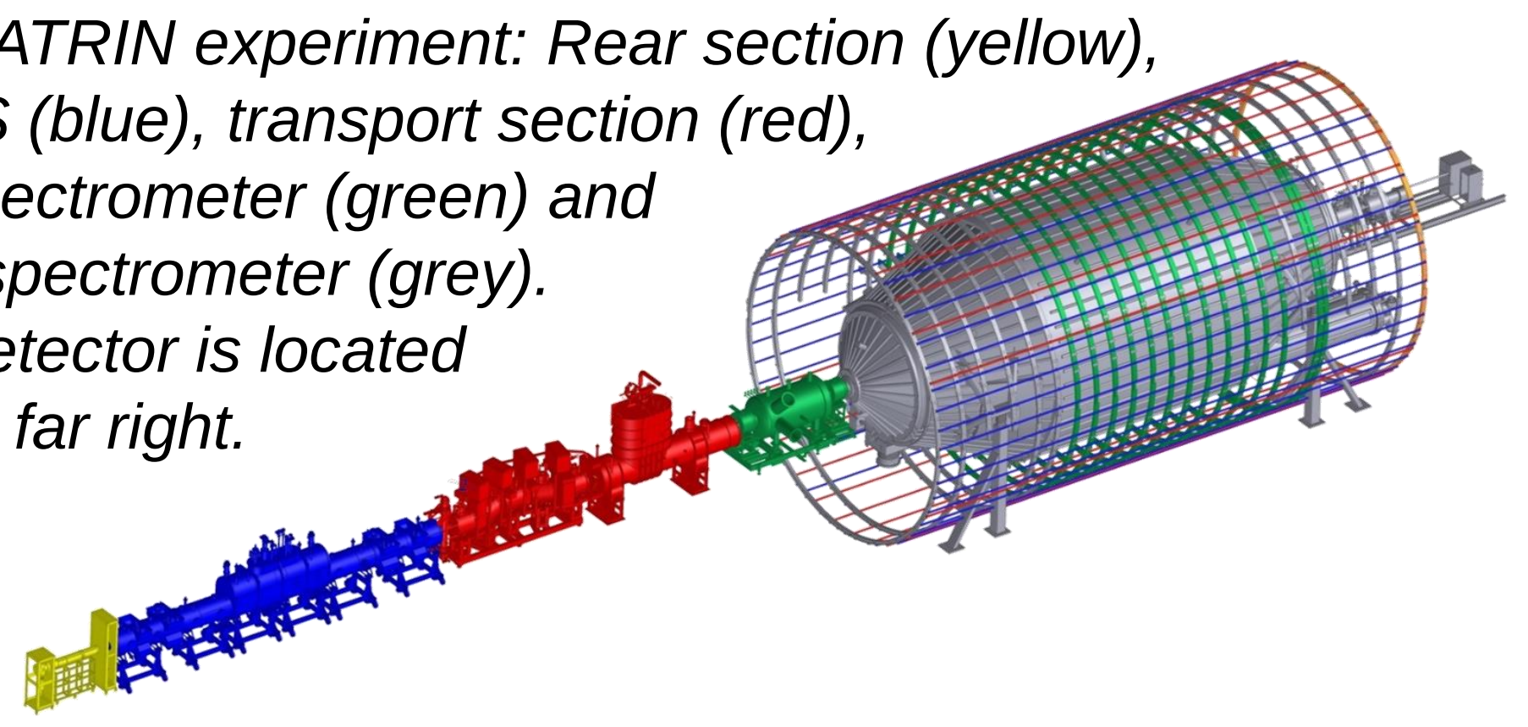
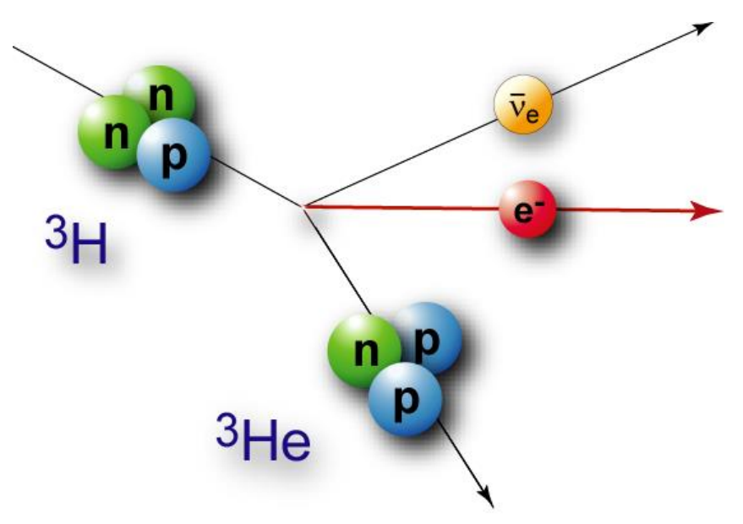
The experiment

Starting in June 2018 the **KA**rlsruhe **TRI**tium **N**eutrino (KATRIN) experiment will investigate the tritium beta decay spectrum endpoint region in order to determine the absolute neutrino mass scale. KATRIN combines an ultra-luminous and stable tritium source with a high-resolution electrostatic filter of the MAC-E-filter type. After three (effective) years of data taking, a sensitivity of $m_\beta = 200\ meV\ (90\%\ C.L.)$ will be reached.

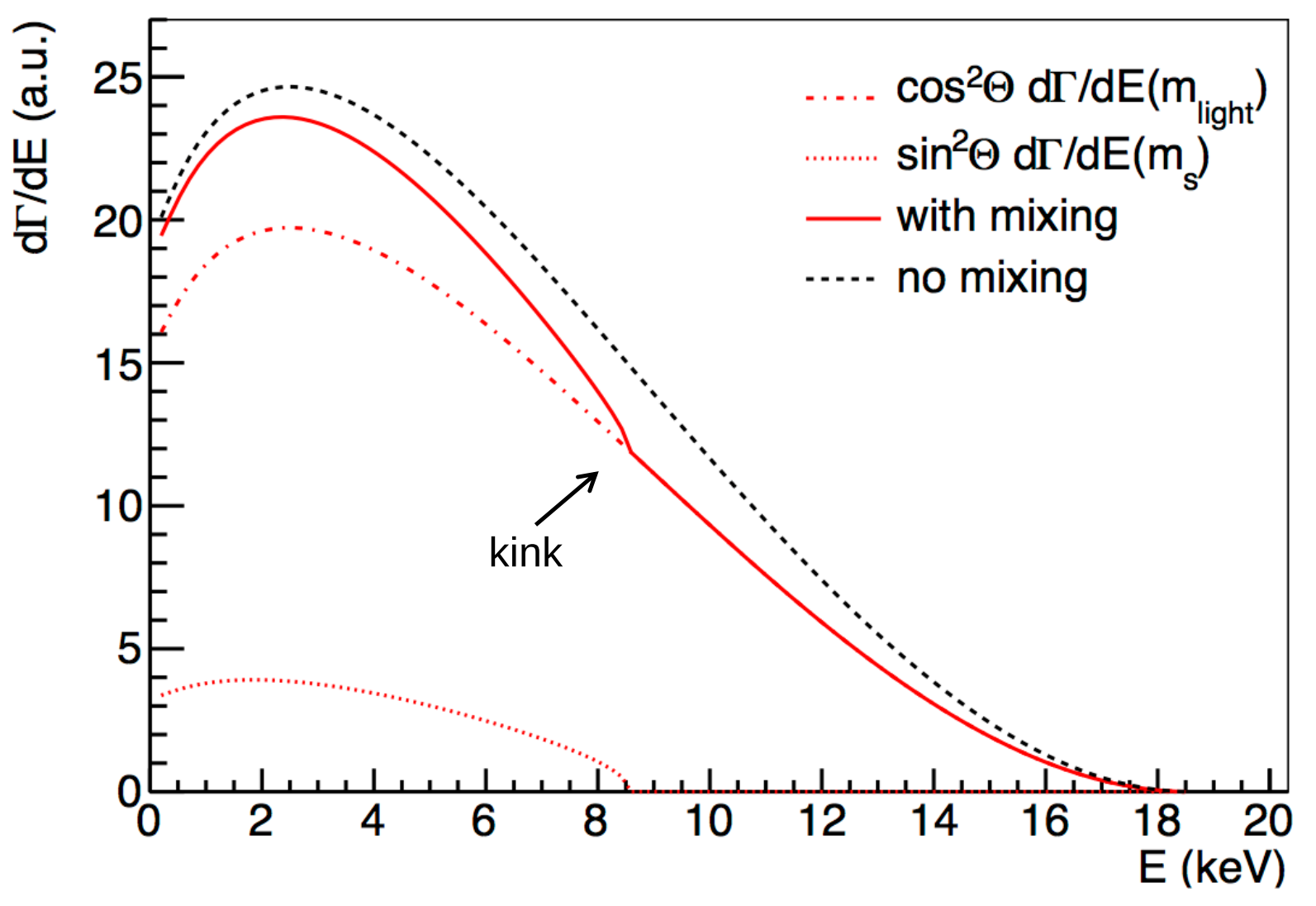


The KATRIN experiment: Rear section (yellow), WGTS (blue), transport section (red), pre-spectrometer (green) and main spectrometer (grey). The detector is located on the far right.

Tritium decays with a half-time of 12.3 years under emittance of an electron and an electron anti-neutrino into Helium-3.



TRISTAN uses the KATRIN setup to search for a sterile neutrino signature by exploring the spectrum further away from the endpoint. In this measurement mode, the count rate will be orders of magnitude larger than in the normal KATRIN operation. Hence, a novel detecor and read-out system has to be developed.



A sterile neutrino signature would manifest as a spectral distortion and a kink at $E = E_{Endpoint} - m_{sterile}$. The kink in the plot is exaggerated.

The tritium spectrum is a superposition of different spectra for each neutrino mass eigenstate, weighted by its mixing to the electron flavor.

$$\frac{d\Gamma}{dE} \propto \cos^2(\theta)\frac{d\Gamma}{dE}(m_{light}) + \sin^2(\theta)\frac{d\Gamma}{dE}(m_s)$$

A novel detector

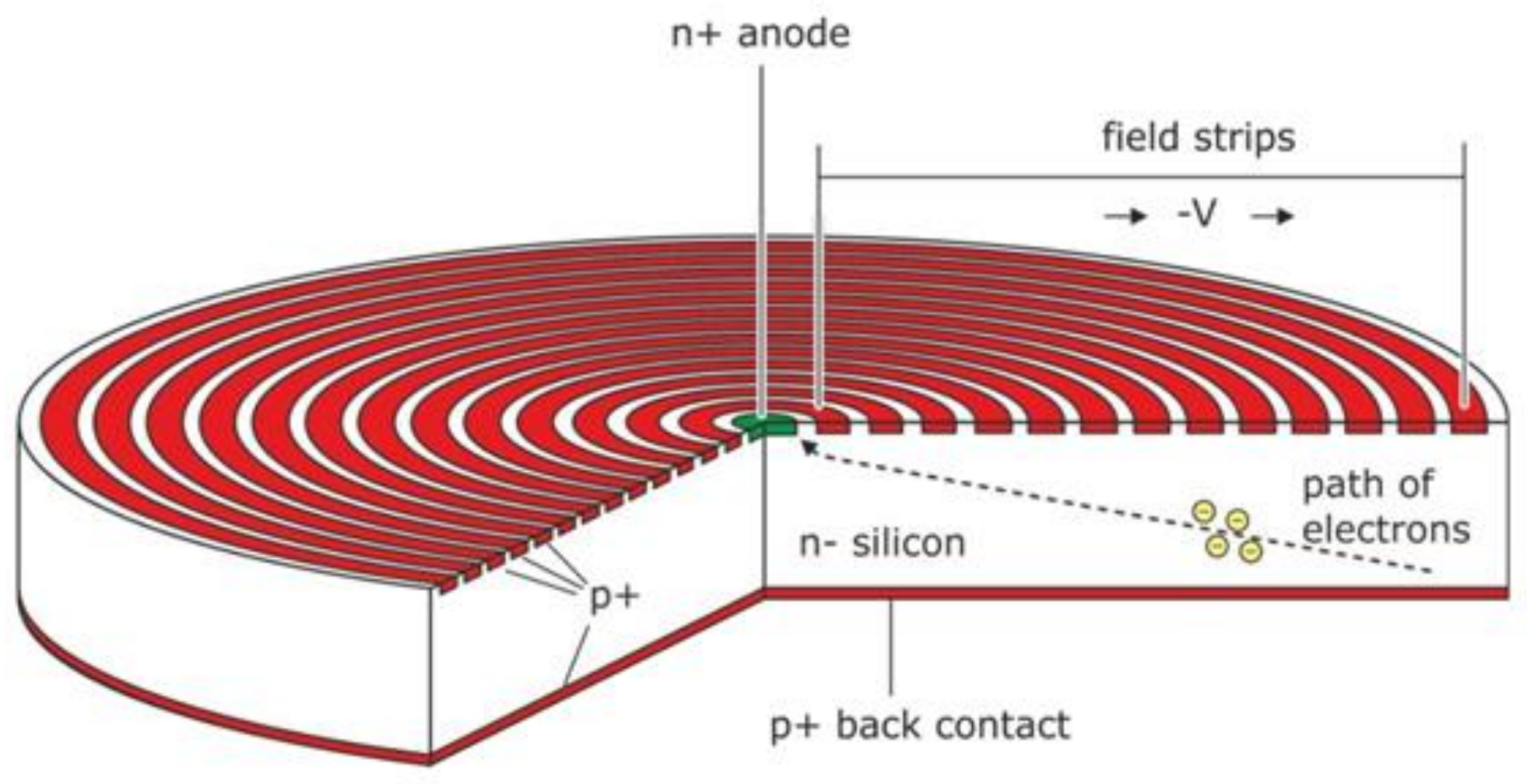
The novel silicon drift detector (SDD) array has to fulfil the following requirements:

Handling of high rates (>10^8 cps)
- ➢ ~ 3500 pixels

Large area coverage (20 cm diameter), small capacitance
- ➢ Silicon Drift Detector technology

Low systematics (ppm-level)
- ➢ Low ADC non-linearity read-out
  + waveform digitization

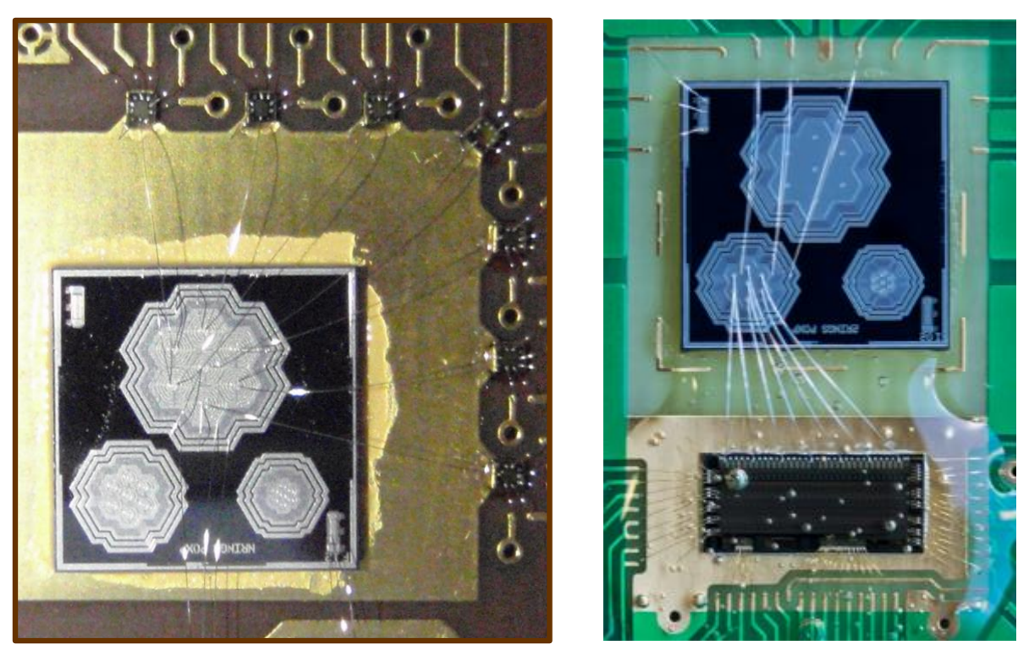
Good energy resolution (300 eV @ 20 keV), low threshold (1 keV)
- ➢ Thin dead layer (< 100 nm)



The silicon drift detector has a small anode to reduce the electrical capacity which gives a short signal rise time. The rings sit on different potentials to drift the charge cloud to the anode.

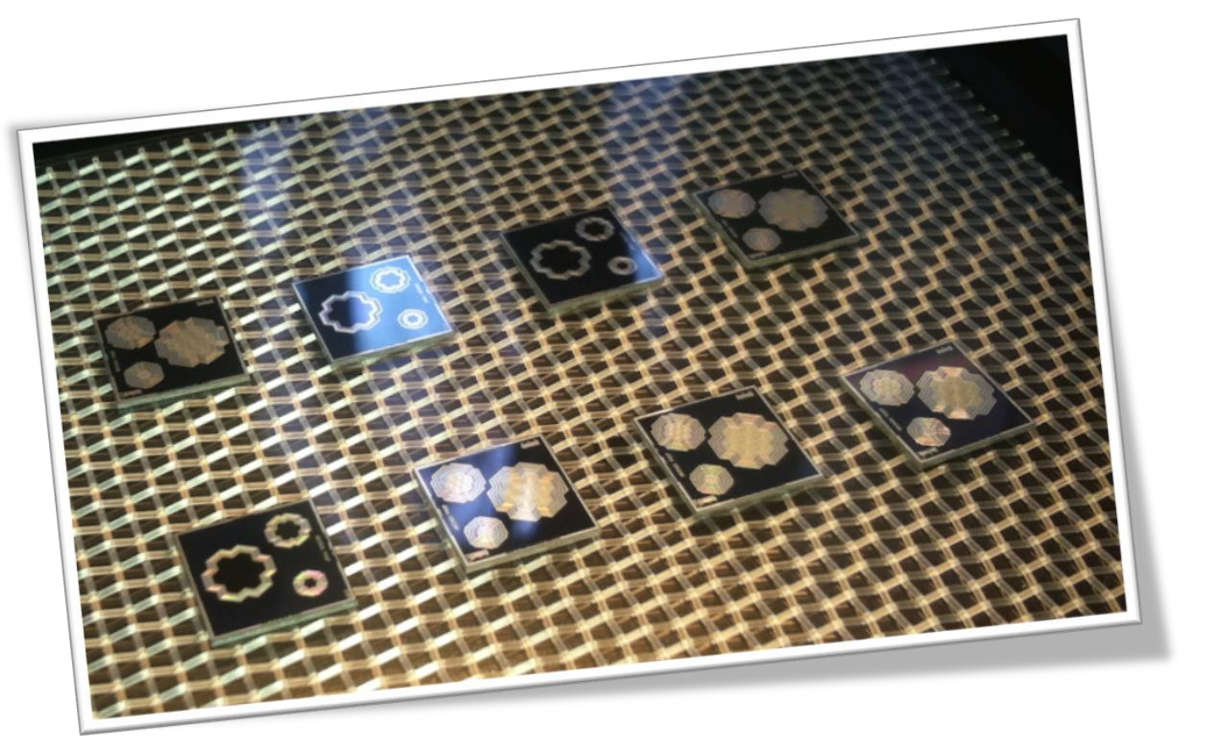
First prototypes

Several silicon drift detector prototypes with seven hexagonal pixels in different sizes (0.5, 1 and 2 mm in diameter) have been produced.



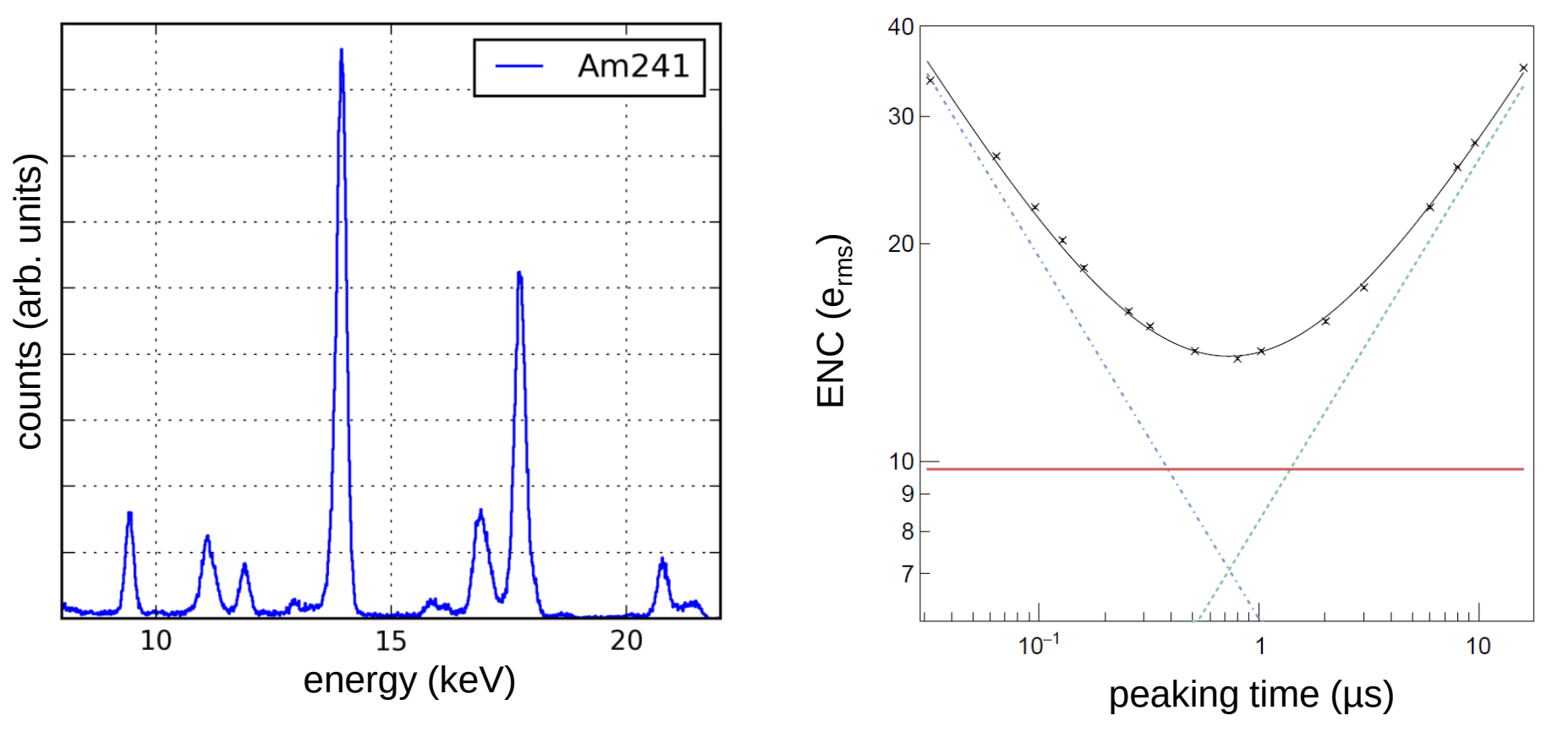
First prototypes have been produced at Halbleiterlabor der Max-Planck-Gesellschaft in Munich.

The chips have been equipped with CUBE ASICs by XG-Lab (left) and the IDefX BD ASIC by CEA/IRFU/SAp (right).

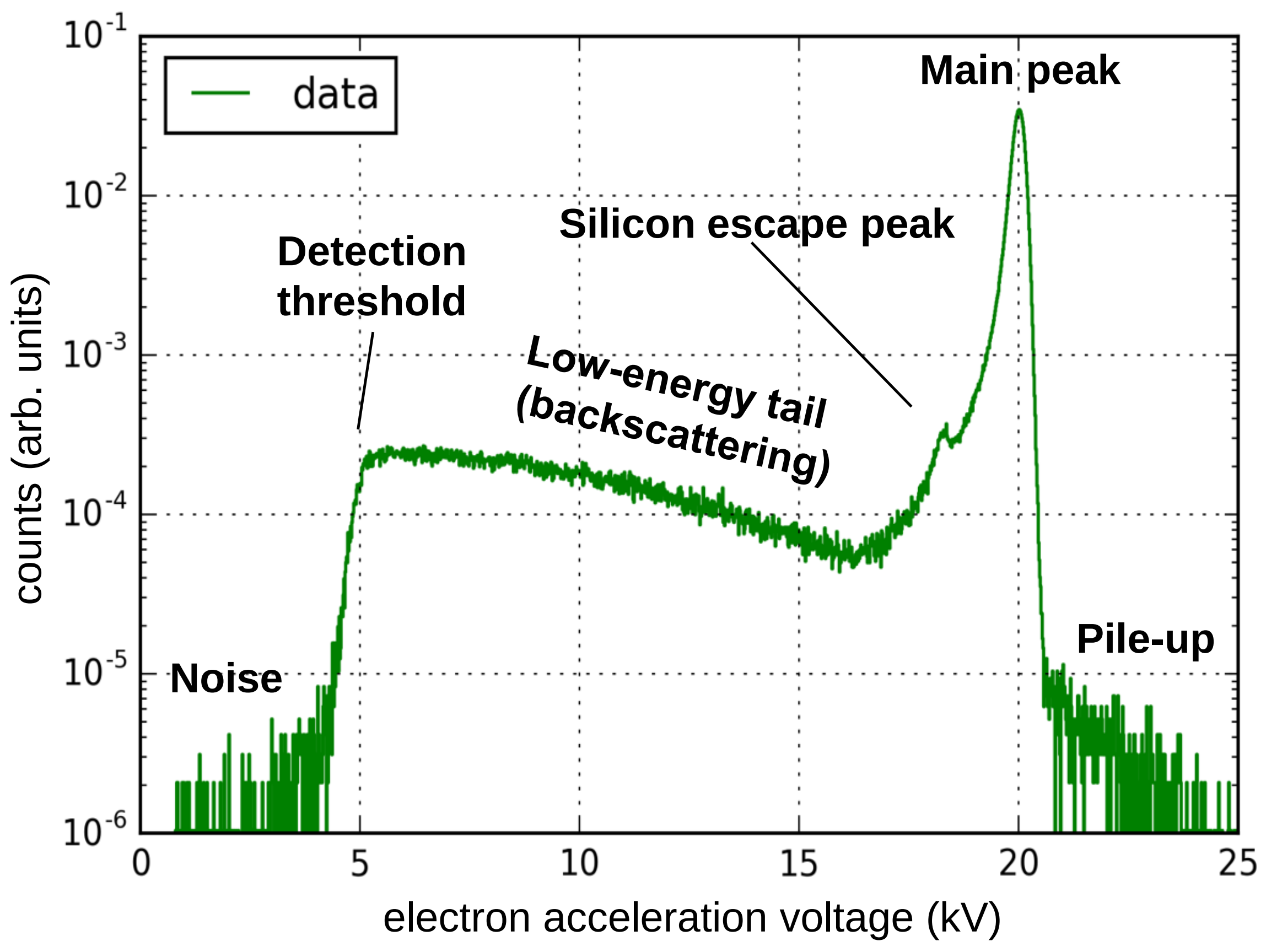


Studies of systematic effects such as dead layer thickness, backscattering, charge sharing, pile-up, ADC non-linearities and others are currently performed.

The detectors were characterized with X-rays from ^{55}Fe and ^{241}Am sources. A resolution of 150 eV_{FWHM} at 6.5 keV (ENC = 9.8) was reached with the XG-Lab system.

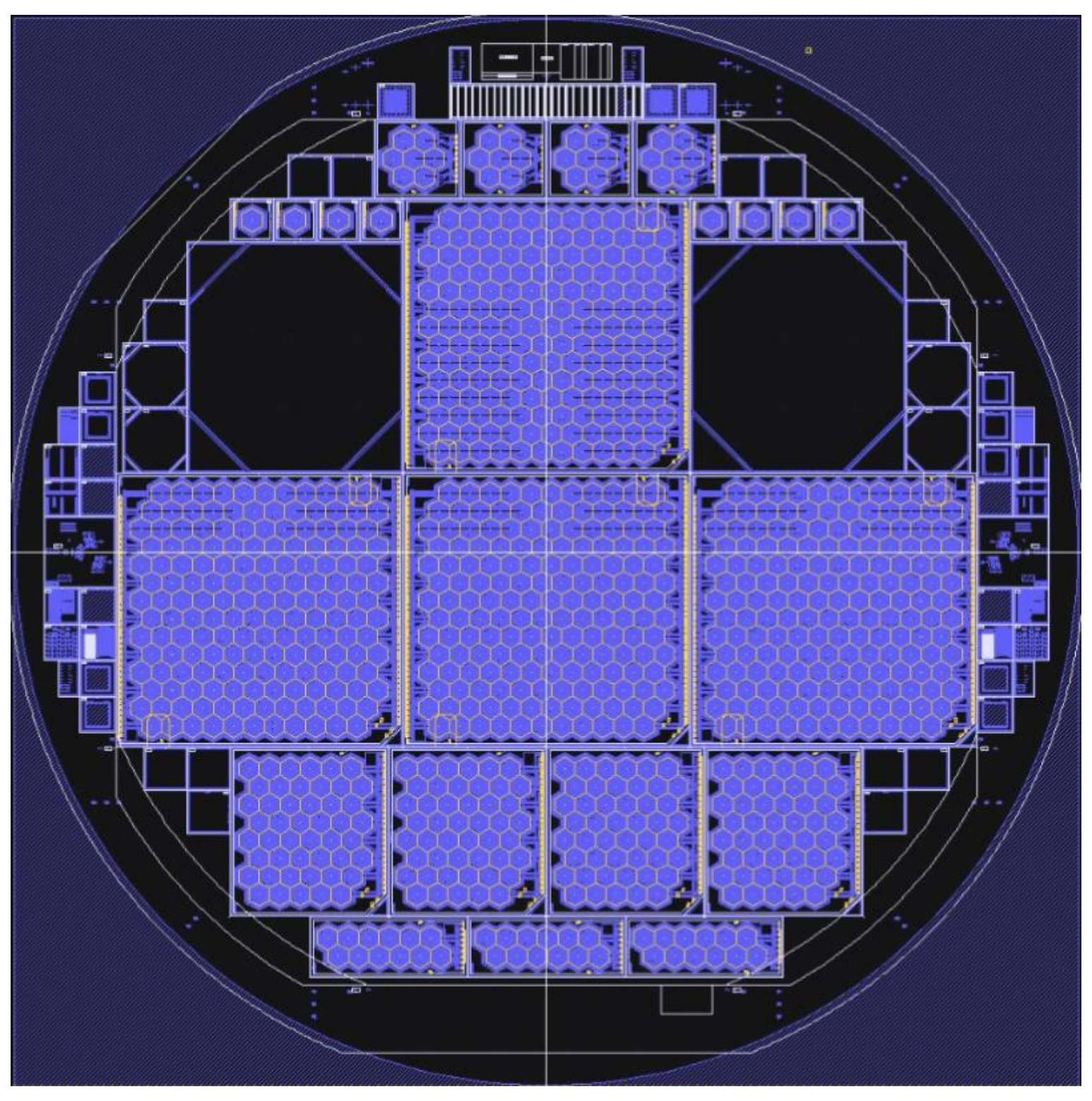


The spectrum of electrons measured with the electron microscope IT300 by JEOL at the Halbleiterlabor with 20 kV acceleration voltage shows the influence of several systematic effects.



The next generation

The next generation of prototype detector chips are currently produced at HLL and will be available end of 2018. They will feature an integrated field-effect transistor to further reduce parasitic capacitance. The pixel diameter was optimized to 3 mm and one wafer will carry chips with different numbers of pixels ranging between 1 and 166 in order to scale up test setups step by step.

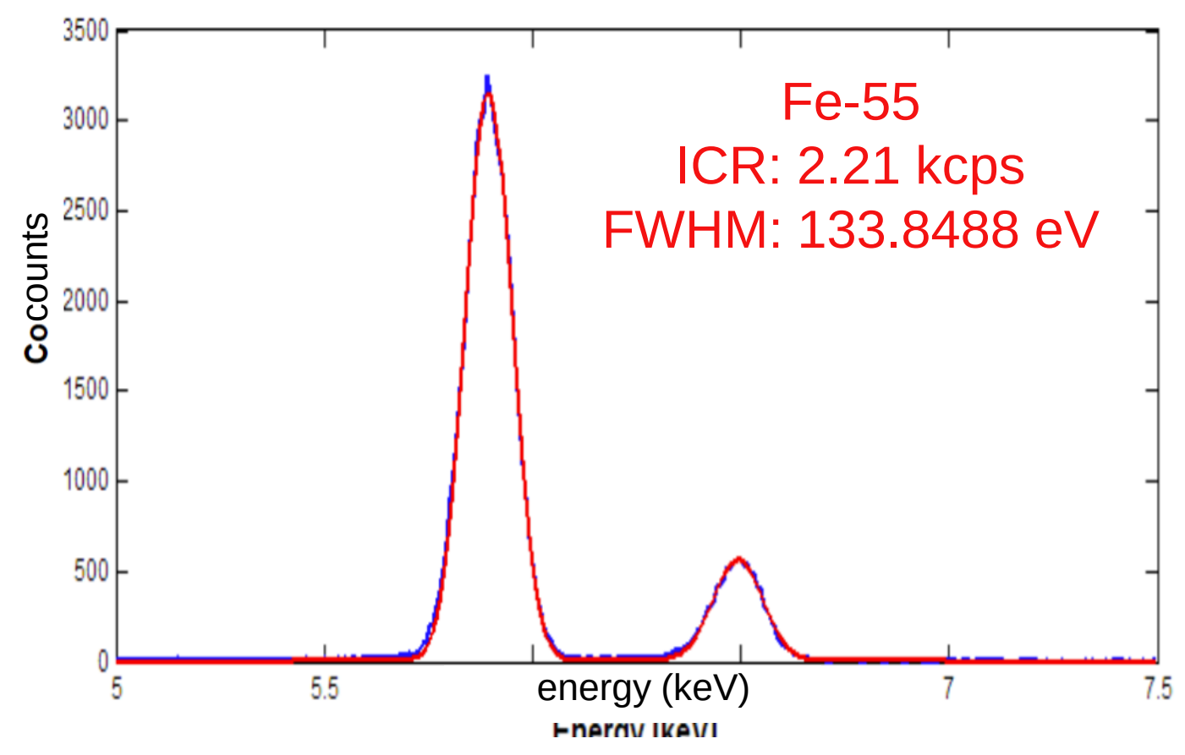


The wafer carries detector chips with 1, 7, 12, 48 and 166 pixels. Four of the 12-pixel units will form one submodule with 48 pixels. 14 of them will form one final detector module.

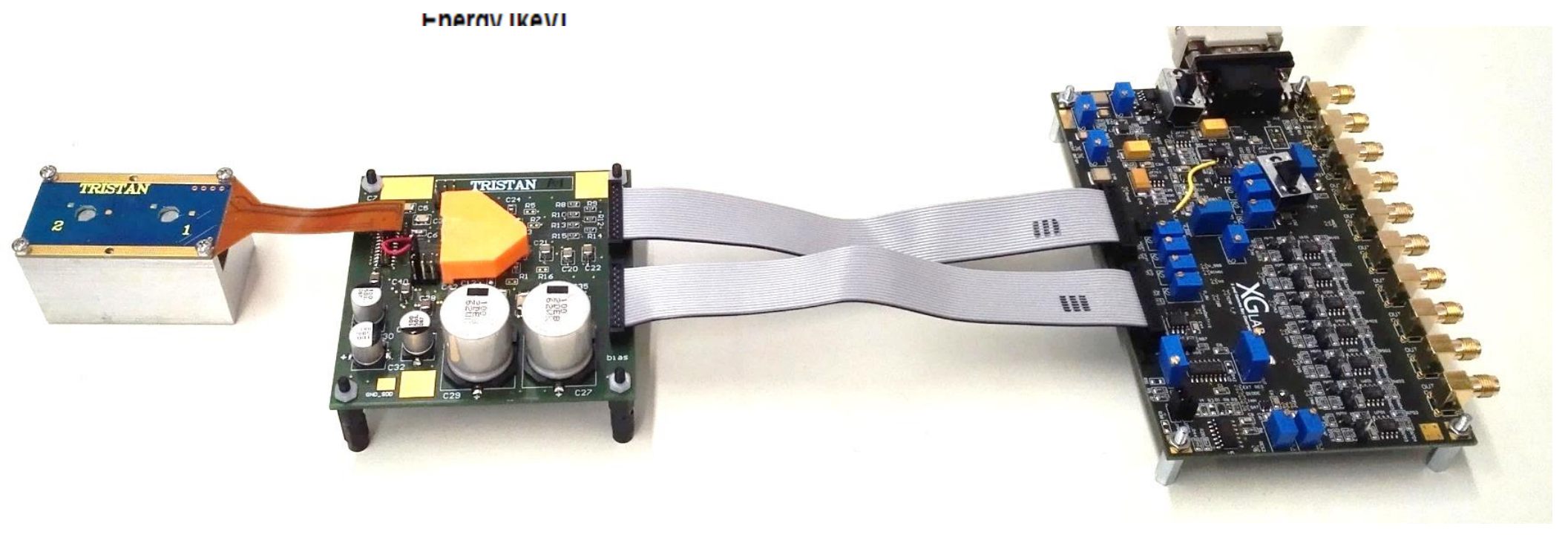
For read-out of the detector chip and amplification of the a special preamplifier ASIC (Ettore) was developed for TRISTAN by XGLab (https://www.xglab.it/). It provides

- 12 independent channels,
- operation in pulsed-reset mode and
- preamplifier and AC-coupled second stage.

The first prototypes have been produced and tested in Milan by XGLab and Politecnico.



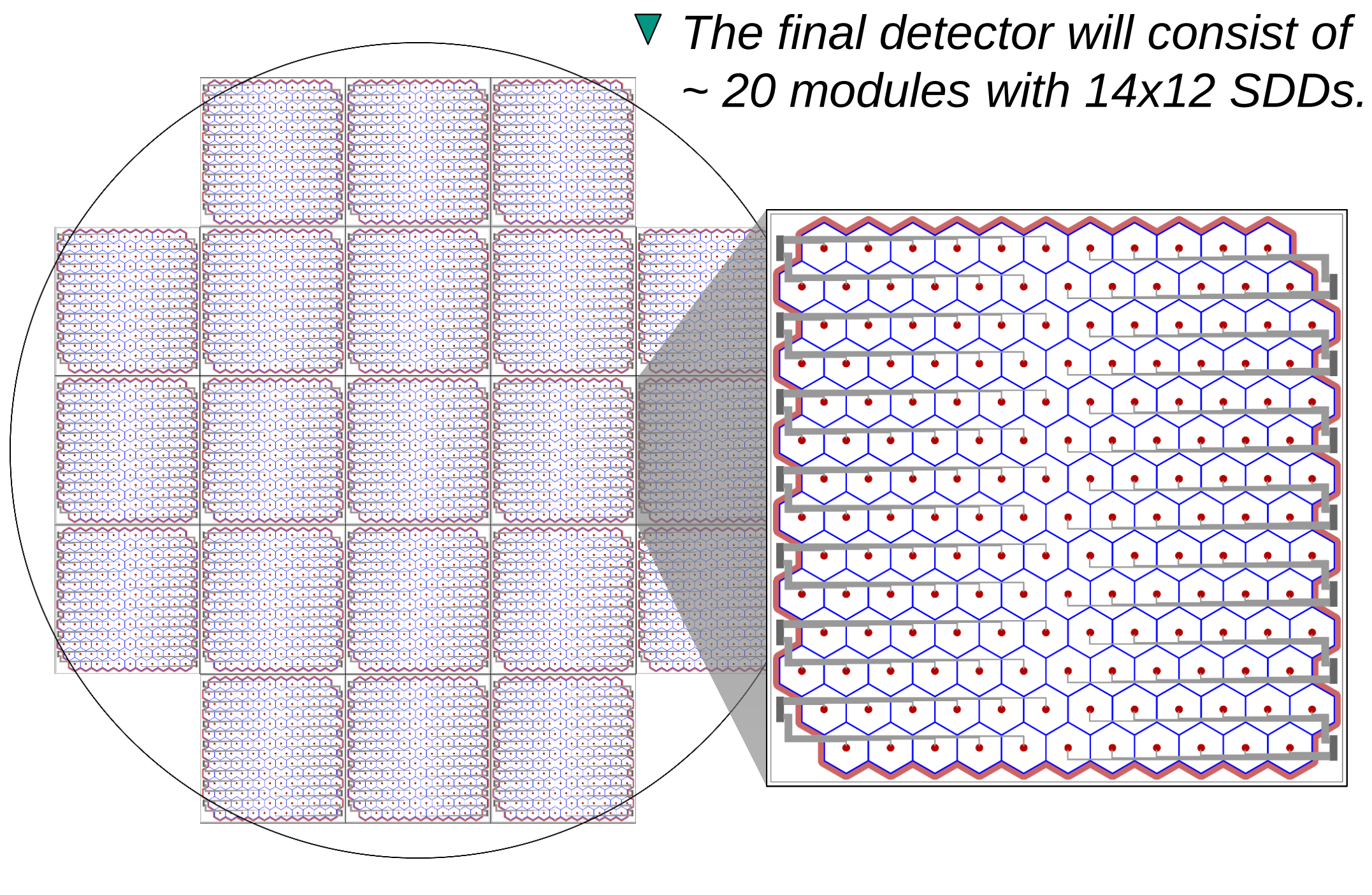
The signal rise time is 30 - 40 ns. A resolution of 134 eV_{FWHM} at 6 keV is reached with a peaking time of 1 µs at an input count rate of 2.2 kcps.



The ASIC test setup consists of a detector board for two single cell detectors, an ASIC board on which Ettore is mounted and a bias board that provides the voltages for the detector and the ASIC.

The final DAQ system has to provide a 14 to 16-bit ADC with small non-linearities and a sampling rate of about 100 MHz. Furthermore, it has to be able to read out all pixels with time synchronization to correct for backscattering and charge sharing among the pixels.

The final detector will consist of ~ 20 modules with 14x12 SDDs.



The final system will prospectively be completed in 2023 to be installed in the KATRIN setup after the neutrino mass measurement. For a statistical point of view, a sensitivity to the active-sterile mixing angle of < ppm can be reached after three years of data taking with the TRISTAN detector.

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