#### The CMS Phase II upgrade -Precision Clock Distribution Studies

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## Motivation



• The CMS detector is undergoing an extensive upgrade:

• Among other significant advancements (see more than twenty talks and posters in this conference), the new ECAL, HGCAL, Barrel and Endcap Timing detectors will be able to tag the events with high precision (~30 ps) timing information, which will help to mitigate an expected average of 200 pile-up events of the HL-LHC.



#### Motivation: need for low jitter clock distribution



- The clock distribution may significantly degrade the precise timing information obtained from the CMS Phase-II detectors.
- A 15 ps random jitter on the clock may have an impact of 3.5 ps (assuming 30 ps [Sensor+TDC] uncertainty).
  - The impact will be significantly larger for higher jitter values.
  - We need a low-jitter clock distribution not to jeopardise the timing performance.



## Motivation

- Distributing a low jitter clock (sub 20 ps RMS) to over 10000 clock distribution channels in a radiation environment with temperature variations is quite challenging. The limited material and cable budget in the detector makes the task even more ambitious.
  - It is important to keep track of the drifts and phase differences between all of the channels. Therefore, investigating feasibility of a jitter monitoring system is necessary.
- Starting from the RF clock, the components of the current clock distribution system is required to be extensively tested.
- The measurements will be used to evaluate the feasibility and/or redesign individual future components of the clock distribution path.
  - CERN, CMS and industry based solutions are being explored and considered.



#### What to expect?

- Introduction and basic concepts
- Back-end tests
- Front-end tests
- Full chain test
- Outlook and conclusion



#### Possible clock distribution schemes





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## Testing methodology

- Two independent test-benches have been used to perform the tests presented in this talk:
  - CEA PCD test stand (Lecroy SDA 820Zi-B scope 20 GHz),
  - CERN HPTD test stand (Keysight DSA91204 scope -12 GHz, Keysight SSA-E5052B spectrum analyzer).
- In order to evaluate each component on the path, we increase the testsetup complexity starting from the clock generator.
- Jitter is evaluated using a very high-speed oscilloscope, IM samples are collected to obtain Time Interval Error (TIE) jitter.
  - The channel to channel jitter is evaluated using a secondary channel as the reference clock input to the scope.
- Our analysis software:
  - <u>https://github.com/osahin/jitter-analyzer</u>



#### Total jitter: dual-dirac-delta method



Total jitter has two different types of components:

- Random Jitter (RJ) can be modelled by a Gaussian,
- Deterministic jitter (DJ) bounded over time.
- A naive but useful model can be obtained by convoluting a Gaussian and two diracdelta functions (Dual-dirac-delta model).
- We quote the RMS of this naive model as figure of merit to have a simple understanding of the overall jitter.



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## µTCA clock distribution

Our test setup is similar to the current  $\mu$ TCA clock distribution system of the CMS detector:

- One of two central boards (AMCI3-XG) is distributing the LHC clock through backplane of the µTCA crate (The Phase II systems will use ATCA crates).
  - The input clock is 2xLHC clock freq, the distributed clock is 40.078 MHz.
  - Dual star clock distribution topology of CMS µTCA is similar to the future ATCA clock distribution network.
- In our tests, we used a custom AMC (FC7) board to emulate the back-end clock distribution node. This board
   encodes the clock and through thevadatech PSU optical links distribute it to front-end.



In the CMS topology one of the MCH slots are occupied by the AMCI3(XG) board.

NAT MCH

AMC13



Crate



#### µTCA clock distribution



- An 80 MHz (2xLHC clock) clean clock (decoded as Trigger-Timing (TTC) optical signal) is used as an input to the μTCA crate (RJ 3.6 ps, DJ 7.9).
- The backplane signals are probed using FC7 front-panel connector which includes a jitter cleaner, CDCE62005 (PLL), in the clock distribution network.
- The 40.078 MHz clock is used as a reference clock ( $\sim$ 2.5 ps RJ).



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## Result: µTCA clock distribution



FC7 (output clk) wrt Si5344 (input clk)
RJ 5.6 ps
DJ 28.2 ps
RMS 15.1 ps

A non negligible DJ component is observed in the  $\mu TCA$  clock distribution network even after the FC7's PLL.



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#### GBTx tests: single channel single BE



The GBTx chip (a rad-hard high-speed communication ASIC widely used in LHC experiments) is tested using dedicated VLDB test board.

For the front-end tests we did not use any crate and only employ a test-bench evaluation board (Xilinx KCU105) which send a clean encoded clock signal to front-end modules.

• The KCU105 boards sending encoded frames to the VLDB board. The clock source is CG635 (at 120.234 MHz).



#### GBTx tests: single channel



- The spectrum plot shows the noise in frequency
- Over I Hz to I0 MHz spectrum, **9 ps random jitter** is observed,
  - between 100 Hz to 10 MHz 5.2 ps.



#### GBTx tests: single channel





#### GBTx tests: two channels two BEs



In order to understand the effect of two independent back-end boards, two Xilinx KCU105 boards sending GBT frames to the VLDB board are employed. The 40.078 MHz CG635 clock source is fed to the Si5344 eval board.



#### Result: GBTx tests

Measurement	RJ [ps]	$\sigma \; [\mathrm{ps}]$	DJ [ps]	$\sigma \; [\mathrm{ps}]$
Single channel - two e-links	7.8	$\pm 0.1$	5.6	$\pm 4.3$
Two channels - single BE	8.7	$\pm 0.1$	24.2	$\pm 2.1$
Two channels - two BEs	13.7	$\pm 0.1$	12.7	$\pm 1.4$
Two channels - two BEs - Si5344 PLL	8.2	$\pm 0.1$	18.6	$\pm 2.3$

- The measurements are obtained using the DSA91204 oscilloscope. For the given measurements, the modules are evaluated on the bench, without any back-end crate (eg  $\mu$ TCA).
- The RMS of the two channel measurement (assuming dual-dirac-model) 12.4 ps indicating that with a low jitter input clock, GBTx is capable of delivering low jitter clock to on detector modules.
- The measurements (particularly DJ) are extremely sensitive to passive components (eg connectors and cables) and installation of these components.
  - A monitoring system is necessary to ensure proper installation of 10000 channels and maintenance over more than a few years of operation.

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#### Simulating the front-end clock distribution jitter



Sensor = 30 ps, RJ = 10 ps, and DJ = 20 ps,

- Without DJ: Sigma 31.60 ps
- With DJ: Sigma 33.08 ps (Gaussian fit)



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#### µTCA: two crates two central PLLs



 $\sim$ 3ps RJ increase and  $\sim$ 30ps DJ increase are observed with respect to the simpler BE clock distribution (see GBTx tests).



#### Simulating the clock distribution jitter



- The simulation of 30 ps RMS (sensor) convoluted with 11.5 ps RJ and 50.7 ps
  DJ assuming the dual-dirac jitter model. RMS of the resulting distribution is
  40.9 ps
- DJ becomes significant; it is important to keep (if possible to minimalize) the deterministic jitter under control.



#### What to expect?

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## Outlook

- The ATCA crate tests will be performed:
- Awaiting for the ATCA components: we will start with the Imperial College Serenity HGCAL-DAQ board.
- We are in contact with other Phase II hardware designers as well.
- Variations in the deterministic jitter indicate that a monitoring system is necessary. This may have an impact on the board design.
- Moreover, we are investigating industry based solutions (e.g. Greenfield Technologies) for the "pure clock" distribution (Type-II).
  - We already received our first custom precise clock and delay generator module from Greenfield Technologies. The module is already being used for the HGCAL HGROC-TDC and PLL measurements effectively.
  - We are also studying the specifications of a possible new radiation-hard front-end clock distribution ASIC.





#### ATCA clock distribution



- **DTH (CERN)** Clock and trigger distribution, and DAQ.
- Serenity (Imperial College) DAQ leaf board. We will monitor the electrical clock distribution using an SMA daughterboard (CEA-Irfu).
- Initially using the GBT-FPGA and GBTx we will test the encoded clock. GBTx is soon to be replaced with IpGBT; enabling us to evaluate the Phase-II FE clock distribution.



## Conclusion

In our tests, conceptually, we obtained encouraging results: indicating that with a well thought and built back-end, and a precision clock-distribution aware FE, the system should be capable of delivering  $\sim 10 \text{ ps}$  RMS RJ jitter with the current electronics in the encoded system.

However, it requires a **careful design and installation for both back-end and front-end components**. Deterministic jitter should be tested and monitored during the operation.

- What would be the overall performance with next generation electronics (particularly lpGBT)?
- A huge amount of work ahead of us to make sure that we can achieve such a performance with the Phase-II detectors. A close collaboration between back-end and front-end developers is crucial.
- A monitoring system is necessary and various options should be explored.
- Our initial tests indicate that the cable length has a negligible impact on the jitter performance.
  - We are investigating the **temperature effects**. Studies are ongoing particularly for the 100m fibre.
- Our short-term main goal is to obtain ATCA measurements including the ATCA DAQ board evaluations



# Backup

#### BE tests: inventory

#### CEA PCD test-stand:

- Stanford CG635 clock generator
- Lecroy SDA 820Zi-B (20 GHz)
- 2 x Xilinx KCU105 evaluation board
- Schroff and Vadatech µTCA crates
- Schroff ATCA crate
- MCHs, Power supplies
- 2 × AMCI 3XG
- $2 \times FC7$ ,  $\mu TCA$  extender board
- 2 x VLDB (GBTx) and MM VTRx
- Si5344 Evaluation board
- Finisar SM SFP+, Avago MM SFP+
- Lecroy high-speed differential and optical probes.
- High quality shielded cables, converters.





#### FE tests: inventory

#### CERN HPTD test-stand:

- Stanford CG635 clock generator
- Keysight DSA91204 scope (12 GHz)
- Keysight SSA-E5052B spectrum analyzer
- 2 x Xilinx KCU105 evaluation board
- 2 × VLDB (GBTx) and MM VTRx
- Si5344 Evaluation board
- Finisar SM SFP+, Avago MM SFP+
- Keysight optical reference receiver
- High quality shielded cables, converters.





#### Jitter cleaner tests





## µTCA clock input



- We generate the 80.156 MHz clock using CG635, and use Si5344 to clean the clock (also obtain a reference for measurements with oscilloscope). The optical TTC clock signal is emulated using the clock injector module.
- This clean optical clock is used as an input to the  $\mu$ TCA crate.



#### µTCA: two crates two central PLLs



#### e-link wrt Si5344 RJ 8.2 ps DJ 32.7 ps



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#### µTCA: two crates single central PLL





## µTCA Clock distribution



- We have also investigated the effect of different slots:
  - Low variation both in RJ (<0.2 ps) and DJ (<4.5 ps)
- No visible correlation between the jitter and the distance to the central module is observed.



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#### GBTx tests: two channels



After optimizing Si5344 PLL, we obtained **8.2 ps jitter** (8.9 ps with the spectrum analyzer in a range of 1 Hz - 10 MHz).



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#### GBTx tests summary

Two channels - two BEs - Si5344 PLL  $8.2 \pm 0.1$   $18.6 \pm 2.3$ 

- <u>https://github.com/osahin/jitter-analyzer</u>
- The simulations are done assuming the Dual-Dirac model.





