Test results and prospects for RD53A, a large scale 65 nm CMOS chip for pixel readout at the HL-LHC

Luigi Gaioni\textsuperscript{a,b}

On behalf of the RD53 Collaboration

\textsuperscript{a}University of Bergamo

\textsuperscript{b}INFN Pavia

14th Pisa Meeting on Advanced Detectors
La Biodola, Isola d'Elba, May 27 - June 2 2018

Supported by the H2020 project AIDA-2020, GA no. 654168
http://aida2020.web.cern.ch
• Focused R&D program aiming at the development of pixel chips for ATLAS/CMS phase 2 upgrades

• 24 Institutions from Europe and US
  • Annecy-LAPP, Aragon, Bergen, Bonn, CERN, FH-Dortmund, FNAL, INFN (Bari, Milano, Padova, Bergamo-Pavia, Pisa, Perugia, Torino), LBNL, Marseille-CPPM, New Mexico, NIKHEF, Orsay-LAL, Paris-LPNHE, Prague IP-FNSPE-CTU, RAL-STCF, Sevilla, Santa Cruz

• 65 nm CMOS is the common technology platform

• RD53 Goals:
  • Detailed understanding of radiation effects in 65nm $\rightarrow$ guidelines for radiation hardness
  • Development of tools and methodology to efficiently design large complex mixed signal chips
  • Design of a shared rad-hard IPs library
  • Design and characterization of common engineering run with full sized pixel array chip
The efforts of the RD53 collaboration led to the submission of the RD53A chip.

400 x 192 pixel, 50um x 50um pixel, 20mm x 11.5mm chip (half size of production chip).

**Goal:** demonstrate in a large format IC

- suitability of 65nm technology (including radiation tolerance)
- high hit rate: 3 GHz/cm^2
- trigger rate: 1 MHz
- Low threshold operation with chosen isolation strategy and power distribution

Not intended to be a production chip

- contains design variations for testing purposes (with 3 different versions of the analog very front-end)

Submitted at the end of August 2017 (shared engineering run with CMS MPA/SSA and other test chips for cost sharing).
RD53A - Large Scale prototype

Chip size: 20.066 x 11.538 mm²
400x192

- Aug. 31, 2017: Submission
- Dec. 6, 2017: First chip test
- Mar. 15, 2018: 25 wafers ordered
- Apr. 13, 2018: First bump-bonded chip test
RD53A floorplan

Top pad row (debug)

400 columns x 192 rows

Digital Chip Bottom (DCB)

Analog Chip Bottom (ACB)

ADC
Calibr.
Bias DACs
CDR/PLL
POR
Sensors
Ring osc.

ShLDO_An
ShLDO_Dig
ShLDO_An
ShLDO_Dig
ShLDO_An
ShLDO_Dig
ShLDO_An
ShLDO_Dig

Padframe

120 µm

9.6 mm

~1.5 mm

~270 µm
RD53A is designed to operate with **Serial Powering** → constant current to power chips/modules in series

- Based on ShuntLDO
- Dimensioned for production chip

**Three operation modes:**

- **ShuntLDO:** constant input current $I_{in}$ → local regulated $V_{DD}$
- **LDO (Shunt is OFF):** external un-regulated voltage → local regulated $V_{DD}$
- **External regulated $V_{DD}$ (Shunt-LDO bypassed)**

**On-going test**
RD53A testing plans

- Two test systems:
  - BDAQ53 - Bonn University [https://gitlab.cern.ch/silab/bdaq53](https://gitlab.cern.ch/silab/bdaq53)
  - YARR - LBNL [https://gitlab.cern.ch/YARR/YARR](https://gitlab.cern.ch/YARR/YARR)
- Debugging of test systems (now): improvements in software, firmware, hardware
- Functional testing of RD53A (on-going)

RD53A chips assembled on a SCC (designed in Bonn)

- Distribution of setups across collaboration has started
- Radiation campaigns in different sites
  - Irradiation with X-rays @ CERN (March 2018: done, scheduled a new campaign in June)
  - Gammas, protons, low-dose betas, all being planned
- Wafer probing
  - Developed needle probes card for fast sequential testing of RD53A on wafers
- Bump-bonding with first sensors:
  - wafers under processing at IZM for bump-bonding to CMS and ATLAS sensors (April 2018)

RD53A public plots: [https://twiki.cern.ch/twiki/bin/view/RD53/RD53APublicPlots](https://twiki.cern.ch/twiki/bin/view/RD53/RD53APublicPlots)
Analog scan

- Local generation of the analog test pulse starting from 2 defined DC voltages CAL_HI and CAL_Mi distributed to all pixels and a 3rd level (local GND)
- Two operation modes which allow to generate two consecutive signals of the same polarity or to inject different charges in neighboring pixels at the same time
- DC Calibration levels generated by 12-bit on-chip DACs

- Full chip responds
- High injection (30 ke-)

![Diagram showing the circuitry of Analog Scan with labels for S0, S0b, S1, S1b, CAL_HI, CAL_Mi, EN, and PIXEL_IN]
• **One stage CSA** with Krummenacher feedback for linear ToT charge encoding

• **Synchronous discriminator**, AC coupled to CSA, including offset compensated differential amplifier and latch

• Threshold trimming by means of autozeroing (no local trimming DAC)

• **Fast ToT counting** with latch turned into a local oscillator (100-900 MHz)
**SYNC front-end: preamplifier response**

- Telescopic cascode with current splitting and source follower
- Two switches controlling the feedback capacitance value
SYNC front-end: noise and threshold distributions

- Synchronous FE fully functional and can be operated at low threshold

\[ \mu = 570 \text{ e}- \quad \sigma = 75 \text{ e}- \]

\[ \mu = 77\text{e}- \quad \sigma = 6 \text{ e}- \]
Synchronous FE irradiation test results

An X-ray irradiation campaign has been performed at CERN in March.
- Temperature: -10$^\circ$C
- TID up to 500 Mrad
Linear Analog Front-end

- **One stage CSA with Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- High speed, low power asynchronous **current comparator**
- **4 bit local DAC** for threshold tuning
**LIN front-end: preamplifier response**

- Gain stage based on a **folded cascode** configuration (~3 uA absorbed current) with a regulated cascode load

---

**Preamplifier output (TOP PAD frame)**

- Circuit diagram showing transistors and current sources.
- Graph showing transient response with labels.

---

**Preliminary**
• Linear FE is fully functional
• Tuning procedure under optimization
• ENC ~ 64 e rms
Differential Analog Front-end

- **Continuous reset integrator** first stage with DC-coupled pre-comparator stage
- Two-stage open loop, **fully differential input comparator**
- **Leakage current compensation** a la FEI4
- **Threshold adjusting** with global 8bit DAC and two per pixel 4bit DACs
• Straight regulated cascode architecture with NMOS input transistor in weak inversion
• Bug in the A/D interface: missing P&R constraint on the Diff. FE hit output → Varying load capacitance on comparator output → systematic variation of delay and ToT

• This bug did not prevent the Diff FE full characterization → Non default parameters to minimize the effect of load capacitance

• Low threshold achieved with 35 e- rms threshold dispersion in non-default configuration → (slower wrt nominal)
First results of RD53A with sensor

- **4 RD53A chips with sensor** arrived in Bonn in April 2018
- Image of a nut placed on the sensor backside, illuminated with Am241 source
- Hit-OR-trigger scan, LIN and DIFF FE, both set to 3 ke- threshold, un-tuned
- Need some more FW/SW development to implement auto-zero sequence for SYNC FE
Conclusions

• The RD53A demonstrator has been submitted in August 2017 in the framework of the RD53 Collaboration in a 65 nm CMOS technology.

• RD53A is alive and preliminary test results are very promising.

• Test systems will be soon available for the institutes to test sensors with RD53A.

• First production lot (25 wafers) bought.

• RD53B design framework under development for final pixel chips for submission in 2019 involving ~ 20 designers.
Backup
IREF measurement and trimming

- All biases provided by internal current DACs, using an internally generated reference current IREF (4 µA nominal) derived by a Bandgap Reference circuit (independent from T, tolerant to TID)

- To compensate for process variations, we can tune IREF by means of 4-bit DAC set by hard-wired connections

Statistical evaluation of the IREF output for IREF Trimming setting = 8 for a sample of 15 chips
RD53A Pixel floorplan

- 50% Analog Front End (AFE) - 50% Digital cells

A “quad”

- The pixel matrix is built up of **8x8 pixel cores** → 16 analog islands (quads) embedded in a flat digital synthesized sea

- One Pixel Core contains multiple Pixel Regions and some additional arbitration and clock logic

- Pixel Regions share most of logic and trigger latency buffering

Distributed Buffering Architecture (FE65_P2 based):
- distributed TOT storage
- Integrated with Diff and Lin FE

Centralized Buffering Architecture (CHIPIX65 based (4x4)):
- centralized TOT storage
- Integrated with Synch FE
LDO: Line regulation

(internal Vref from BGR)

(external Vref = 0.6 V)

\[ \Delta V_{DDA} = 49.1 \text{mV} \]
\[ \Delta V_{DDD} = 63.6 \text{mV} \]

\[ \Delta V_{DDA} = 1.4 \text{mV} \]
\[ \Delta V_{DDD} = 1.1 \text{mV} \]
ShuntLDO: Line regulation

(internal Vref; internal Vofs) ↔ (external Vref=0.55V; external Vofs=0.4V)

Note: here Vofs means 1/2 of effective ShLDO Voffset

![Graphs showing voltage vs. input current for RDS3 Internal with ΔVDDD=29.7mV and ΔVDDA=41.4mV on the left, and ΔVDDD=3.8mV and ΔVDDA=4.4mV on the right.]}
Synchronous Analog Front-end #2

**ToT - Without fast ToT**

Time-over-Threshold distribution ($\Sigma = 1411687$)

**ToT - With fast ToT**

Time-over-Threshold distribution ($\Sigma = 1403676$)

Default configuration
Frequency $\sim 100$ MHz

RD53 Internal
RD53A Power consumption

<table>
<thead>
<tr>
<th>Configuration</th>
<th>VDDD [mA]</th>
<th>VDDA [mA]</th>
</tr>
</thead>
<tbody>
<tr>
<td>No clock in pixel cores (at startup)</td>
<td>124</td>
<td>365</td>
</tr>
<tr>
<td>Full chip enabled</td>
<td>442</td>
<td>365</td>
</tr>
</tbody>
</table>

- Direct powering
- Default bias settings
- **Value mostly as expected**

- On average (including Chip Bottom): 5.7 µA/pix (digital) -- 4.7 µA/pix (analog)
- In final chip less contribution from the Chip Bottom
- Further optimizations in both analog/digital pixels under investigation for final chips
RD53A main specifications

From the Spec. document

http://cds.cern.ch/record/2113263

• **Hit rate**: up to 3 GHz/cm² (75 kHz pixel hit rate)
• **Detector capacitance**: < 100 fF (200 fF for the edge pixels)
• **Detector leakage**: 10 nA (20 nA for the edge pixels)
• **Trigger rate**: max 1 MHz
• **Trigger latency**: 12.5 us
• **Low threshold**: 600 e− → severe requirements on noise and dispersion
• **Min. in-time overdrive**: < 600e-
• **Noise occupancy**: < 10⁻⁶ (in a 25ns interval)
• **Hit loss @ max hit rate**: 1%
• **Radiation tolerance**: 500 Mrad @ -15° C
Analog bias

- **AFE area & arrangement** → 35um x 35 um aspect ratio with “analog island” arrangement
- Same bump PAD structure
- Common strategy for power, bias distribution & shielding

- **M6 V lines** for the analog bias
- **M5/M7 shield** for bias lines in the digital section of the pixel
- **AP/M9/M8 V supplies**
Pixel array logic organization

- Each Pixel Core receives all input signal from the previous core (closer to the Digital Chip Bottom)

- Regenerates the signals for the next core.

- The timing critical clock and calibration injection signals are internally delayed to have a uniform timing (within 1-2 ns)