

Recent developments in the CBC3: a CMS micro-strip readout ASIC for track-trigger modules at the HL-LHC

a CIVIS MICLO-SUTIP readout ASIC IOF Grack-Grigger modules at the HL-LHC

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CMS Outer Tracker Upgrade High-Luminosity LHC (HL-LHC) Upgrade (Phase II)

- CERN Accelerator complex will be upgraded during 2024-2026 to increase instantaneous luminosity of the LHC by a factor of 5 to 5x10³⁴ cm⁻²s⁻¹
- CMS plans to replace the current tracker during the last LHC shut-down before HL-LHC
 - improve radiation resistance, reconstruction efficiency at high pile-up, reduce material budget
 - include tracker information to improve L1 trigger performance and meet target rate of 750 kHz



- Outer tracker made up of pT modules : module sensing element made up of two sensors separated by a few mm along the track direction
 - correlating clusters in the two sensor layers for discrimination between high and low pT tracks
 - stubs [high pT tracks] transmitted off module to the L1 track finding system at 40 MHz



CMS Binary Chip (CBC)

Readout ASIC for for Outer Tracker Strip-Strip (2S) modules

- CBC3 (Imperial College,Rutherford Appleton Laboratory) final prototype of ASIC in 130 nm CMOS. Full description provided by Prydderch et. al in [1]
 - all logic necessary to identify and transmit high pT track primitives (stubs)
 - unsparsified binary readout provides stub data at 40 MHz and read-out data at 750 kHz
 - expect 1000 e- noise , 20 ns peaking time, 50 ns return to baseline



- Even/odd channels on chip used to read-out top/bottom strips with data combined to select high pT tracks (*stubs*). Communication across the chip boundaries to form stubs
 - full stub information (position, bend) sent to aggregator ASIC (CIC)



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CMS Binary Chip (CBC) CBC3 Testing Campaign in 2017





- Single Event Upsets Tests using the Light Ion Facility (LIF) at the Cyclotron Resource Centre in Louvain-La-Neuve, Belgium (complete results published by Uchida et. al in [2])
 - SEUs showed an order of magnitude improvement on previous prototype [CBC2]
- Total Ionizing Dose Tests using the CERN X-ray irradiation facility : 8 chips irradiated at two temperatures (x4 dose rates) while monitoring :
 - pedestal and noise, DAC linearity
 - current consumption on the power rails supplying V_{DDD} and V_{DDA}
- In-beam performance of pT module prototype with CBC3 readout



- Similar effect to that observed in the other 130 nm CMOS ASICs using linear NMOS transistors (CBC2, ATLAS FEI4):
 - increase only present on the digital side [independent monitoring of power consumption on digital/analogue rails of the ASIC]increase saturates after about 12 kGy of TID, and begins to decrease after that. Does not affect functionality of ASIC.





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 - maximum current increases with increasing dose rate and decreasing temperature





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 - maximum current increases with increasing dose rate and decreasing temperature
- What can we expect at HL-LHC operating conditions? [2.4 Gy/h and -15°C]



Reminder of damage from ionizing radiation in oxides

- The electron-hole pairs generated by ionizing radiation interact with existing defects and impurities in the oxide (e.g. STI in an NMOS transistor) to introduce :
 - trapped positive charge (Not) in the oxide and interface traps (Nit) at the interface





Radiation induced leakage current in linear NMOS transistors Backhaus parametrization in terms of the effective charge (Not-Nit) build-up

• Radiation induced leakage path due to charge build-up in the STI can be modelled as a parasitic transistor with a transfer characteristic given by

 $I_D \approx 0 \text{ for } V_{GS} < V_{th}$ $I_D \approx K_0 (V_{GS} - V_{th})^2 \text{ for } V_{GS} \ge V_{th}$



• where V_{GS} and V_{th} are proportional to the effective charge build up in the silicon ($N_{ot} - N_{it}$) and the critical charge (N_{th}) required to activate the parasitic transistor so that

$$I = I_{
m pre-Irradiation}$$
 for $N_{
m OT} - N_{
m IT} < N_{
m th}$
 $I = I_{
m pre-Irradiation} + K(N_{
m OT} - N_{
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• In linear NMOS transistors :

• interface traps (Nit) are negatively charged and therefore compensate for the positive charge build-up (Not)





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Used to fit measured current increase

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 - interface traps (Nit) are negatively charged and therefore compensate for the positive charge build-up (Not)





CBC3 Radiation Damage Model

Dose rate dependance of current increase [at a fixed temperature]

• Global fit of measured increase in digital current for all chips irradiated at a fixed temperature :



Fit parameters describing effective charge build-up

- \dot{D} dose rate of ionizing radiation
- $d_{\scriptscriptstyle ext{critical}}$ critical dose at which parasitic transistors are activated
- f_{or} probability of a hole being trapped in a deep trap in the STI
- $r_{\rm ot}$ de-trapping rate of trapped holes in the STI
- f_P probability of a hole being trapped by a hydrogen containing defect
- f_I probability of an available dangling bond capturing a free proton



CBC3 Radiation Damage Model

Dose rate dependance of current increase [at a fixed temperature]

• Fit results used to parametrize dose-rate dependance of model parameters and extrapolate current increase to lower dose-rates

 1) Global fit



Using radiation damage model to extrapolate to HL-LHC conditions Expected increase in current consumption of CBC3

CMS

- Predicted lowest expected temperature on the 2S modules is $\sim -15^{\circ}$ C :
 - can use results from irradiations at -19°C and 5°C to set bounds on the expected increase per CBC for a 2S module [parameters extracted from fit used to predict effect at lower dose rates]



Using radiation damage model to extrapolate to HL-LHC conditions Expected increase in current consumption of CBC3

- Predicted lowest expected temperature on the 2S modules is $\sim -15^{\circ}C$:
 - can use results from irradiations at -19°C and 5°C to set bounds on the expected increase per CBC for a 2S module [parameters extracted from fit used to predict effect at lower dose rates]
 - dose rate at HL-LHC taken from FLUKA simulation of the CMS PhaseII detector





Using radiation damage model to extrapolate to HL-LHC conditions Expected increase in power consumption of 2S modules

- Results from irradiations at -19°C used to set upper limit on the expected increase in power consumption of a 2S module at the dose rates expected at the HL-LHC assuming :
 - x16 CBCs powered by a single service hybrid on a 2S module
 - operating voltage of 1.25 V per CBC
 - x3 safety factor applied to dose rate from FLUKA simulation of the CMS PhaseII detector

Predicted increase in power consumption of 2S modules in the Outer Tracker barrel





Radiation Qualification of the CBC3 CBC3 Testing Campaign in 2017



- Single Event Upsets Tests using the Light Ion Facility (LIF) at the Cyclotron Resource Centre in Louvain-La-Neuve, Belgium (complete results published by Uchida et. al in [2])
 - SEUs showed an order of magnitude improvement on previous prototype [CBC2]
- Total Ionizing Dose Tests using the CERN X-ray irradiation facility : 8 chips irradiated at two temperatures (x4 dose rates) while monitoring :
 - pedestal and noise, DAC linearity
 - current consumption on the power rails supplying V_{DDD} and V_{DDA}
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Prototype based on a 2CBC3 Front End Hybrid (FEH)

 First prototypes (CERN DT) using 50 mm long n-on-p sensors (200 μm active thickness silicon) and a 2CBC3 flexible hybrid (CERN EP-ESE)



Mini-module design

Mini-module @ FNAL BT

first opportunity to test bump-bonded CBC3s all previous measurements performed on wire-bonded chips





In beam performance of 2CBC3 mini-module Fermilab Test Beam Facility : CMS Pixels Phase0 Telescope

CMS

- 120 GeV proton beam (primary beam) bunched at 54 MHz (4.2 s spill every minute)
- FNAL Beam Telescope used to reconstruct tracks pointing towards the 2S prototype
 - PSI46 analogue chip based readout [$100x150 \mu m2$ pixel cells : 80 rows and 52 columns]
 - Resolution of ~ 8μ m in both directions [at nominal location]
 - $1.6x1.6 \text{ cm}^2$ coverage (size of sensor ~ $2.2x5 \text{ cm}^2$)
- Mini-module (2S-prototype) placed in the center of the telescope on a rotation stage :
 - rotating the mini-module about y mimics the behaviour of high momentum tracks in a magnetic field







In beam performance of 2CBC3 mini-module Nominal threshold [~3.2e3 electrons from the pedestal (~4.2 σ_{Noise})] and 0° tilt

- Resolution and cluster detection efficiency at nominal threshold on one of the two sensor planes :
 - resolution consisted with 90 μ m pitch strips (expected binary resolution of ~ 26 μ m)
 - cluster detection efficiency (>99%) uniform across module



In beam performance of 2CBC3 mini-module Nominal threshold [~3.2e3 electrons from the pedestal (~4.2σ_{Noise})]

- Stub turn on curves measured for different correlation windows
 - (as expected) pT cut-off decreases as the size of the correlation window is increased
 - cut-off seems to match expected* value well : 2.13 GeV, 1.72 GeV, 1.45 GeV









Conclusions CBC3 : a readout ASIC for for Outer Tracker Strip-Strip (2S) modules



- Qualification of CBC3 (TID, SEUs) for HL-LHC levels completed in first half of 2017
- Design changes (rel. to CBC2) improved the radiation hardness of the CBC3
- Data taken during qualification used to build a radiation damage model to parameterize the radiation induced current increase on the digital side of the ASIC
 - model used to predict impact of radiation on the power consumption of a single 2S module at HL-LHC operating conditions : max. expected current increase in CBCs would increase power consumption of a 2S module by <1 %
- Successful test beam at FNAL with the first 2CBC3 based 2S prototype performed at the end of 2017



Back-up Slides

Radiation Qualification of the CBC3 Summary of test campaigns conducted in first half of 2017



- Single Event Upsets Tests using the Light Ion Facility (LIF) at the Cyclotron Resource Centre in Louvain-La-Neuve, Belgium (complete results published by Uchida et. al in [2])
 - no SEUs observed in pipeline data and logic cells
 - SEUs showed an order of magnitude improvement on previous prototype [CBC2]
 - ~1.5 bit flips/day at HL-LHC [a few % of the 2640 I2C bits are related to global configuration registers] → reconfiguration upon error detection possible

Type of Cell	ф _{LiF} [cm ⁻² s ⁻¹]	ф* _{HL-LHC} [cm ⁻² s ⁻¹]	# observed bit flips	Time [hrs]	σ _{SEU} [x 10 ⁻¹¹ cm ⁻²]	ER _{HL-LHC} [bit flips/h]
Pipeline Data	2.2E+08	7.45E+06	0	10.7	< 0.027	< 0.008
Pipeline Logic	2.2E+08	7.45E+06	0	1.4	< 0.21	< 0.054
I2C Registers	2.2E+08	7.45E+06	25	12.4	0.27 ± 0.05	0.069 ± 0.013

- Total Ionizing Dose Tests using the CERN X-ray irradiation facility (EP-ESE-MIC)
 - 8 chips irradiated at two temperatures (4 dose rates) while monitoring :
 - current consumption on the power rail supplying V_{DDD} and V_{DDA}
 - pedestal and noise



- Similar effect to that observed in the CBC2 and ATLAS FEI4 (130 nm CMOS):
 - increase only present on the digital side [independent monitoring of power consumption on digital/analogue rails of the ASIC]increase saturates after about 12 kGy of TID, and begins to decrease after that



CBC3 vs. CBC2 layout





CBC2 layout

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C4 layout, 250um pitch, 19 columns x 43 rows

30 inter-chip signals (15 in, 15 out), top and bottom gives continuity across chip boundaries

 right-most column wire-bond (for wafer probe test) access to: power fast control l2C outputs

prototype powering features retained CERN bandgap, LDO for analog powering, same as prototype improved DC-DC switched capacitor circuit (CERN) slower switching edges & rad-hard layout

chip submitted for fabrication July 2012

wafers back January 2013 wire-bondable (other users) and C4 processed (CBC2)

Davide Braga, Mark Prydderch, Peter Murray (RAL)



CBC3 vs. CBC2 layout







CBC3 Irradiation Tests Summary

Temperature and dose-rate dependence of pedestal/noise

- Pedestal (averaged across all 254 CBC channels) during irradiation [1.25 V]
 - 6 chips irradiated at 3 different dose rates, and 2 different temperatures







CBC3 Irradiation Tests Summary

Temperature and dose-rate dependence of pedestal/noise

- Noise (averaged across all 254 CBC channels) during irradiation [1.25 V]
 - 6 chips irradiated at 3 different dose rates, and 2 different temperatures







CMS Phase 2 Tracker Upgrade Level1 (L1) Triggering at the HL-LHC

- Two level trigger system currently implemented in CMS
 - Level 1 (L1) hardware trigger using information from calorimeters and muon detectors [design specification : 100 kHz, latency of $3.2 \,\mu s$]
 - High Level Trigger (HLT) software trigger including information from the tracker
- Increase in luminosity will lead to increased production rates and pile-up [53 at the highest instantaneous luminosity reached in 2016 → 200 at HL-LHC] which poses a challenge for the current L1 trigger system. Therefore upgrade of the L1 system also expected for HL-LHC
 - target specification for L1 trigger for HL-LHC is 750 kHz and a latency of 12 μ s
 - include tracker information to improve L1 trigger performance



CMS Phase 2 Tracker Upgrade Level1 (L1) Triggering at the HL-LHC

- All tracker data cannot be read out at bunch crossing frequency (40 MHz) therefore a reduction in the amount of data on the module used for L1 tracking is required which has led to the pT module concept :
 - module sensing element made up of two sensors separated by a few mm along the track direction
 - correlating clusters in the two sensor layers allows discrimination between high and low pT momentum tracks (charged particles bend in CMS's 3.8T field)
 - stubs [high pT tracks] can then be transmitted off module to the L1 track finding system at 40 MHz
 - tracks are combined in the L1 trigger system with calorimeter and muon information







CBC3 Irradiation Tests Summary

Lessons learned from the CBC2 Irradiations : Radiation induced leakage

- Ionizing dose tests on CBC2 showed an initial spike in the current consumption of the chip :
 - identified as radiation induced leakage in the pipeline logic
 - non-enclosed NMOS transistors in pipeline suspected
 - effect also manifests as failure of some channels to respond to the test pulse



- Radiation hardness of pipeline SRAM block in the CBC3 improved by :
 - replacing NMOS read and write access transistors by more rad hard PMOS devices
 - replacing NMOS pull-down transistors with enclosed NMOS devices

CBC3 X-ray Irradiation : Digital Current, Un-cooled, 20 kGy/hr , max. dose of 350 kGy

- Similar effect to that observed in the CBC2 :
 - increase only present on the digital side
 - increase in the digital current observed near the start of the irradiation (dose of $\sim 2.3 \text{ kGy}$)
 - increase saturates after about 12 kGy of TID, and begins to decrease after that



- Changes implemented in the CBC3 have improved the radiation tolerance, however :
 - radiation induced leakage still present in the ASIC

CBC3 Irradiation Tests Summary

Lessons learned from the CBC2 Irradiations : SEU sensitivity

- Single Event Upset tests on the CBC2 showed that the I2C registers were susceptible to SEUs :
 - triplicated I2C registers used in the CBC2
 - but with insufficient separation $(2.4 \,\mu m)$ between the three nodes of the cell
 - cells susceptible to simultaneous upsets in multiple nodes







CBC3 Irradiation Tests Summary Lessons learned from the CBC2 Irradiations : SEU sensitivity

- Single Event Upset tests on the CBC2 showed that the I2C registers were susceptible to SEUs :
 - triplicated I2C registers used in the CBC2
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 - cells susceptible to simultaneous upsets in multiple nodes





- Sensitivity of the CBC3 to SEUs improved by :
 - replacing triplicated I2C registers with Whitaker latches
 - n+ diffusions used to store 0's (an SEU can only change their state from $1 \rightarrow 0$)
 - p+ diffusions used to store 1's (an SEU can only change their state from $0 \rightarrow 1$)

- 1.4 hours of beam time dedicated to measuring the SEU rate in the data stored in the CBC3's pipeline.
 - no errors which can be attributed to SEUs
 - *upper limit* placed on expected SEU cross-section using LIF data : 2.1x10⁻¹² cm²
 - *upper limit* placed on error rate expected at HL-LHC : 1.5x10⁻⁵ s⁻¹ per chip → 1.3 errors per day



ER [bit flips/s]_{Upper Limit} =
$$\frac{-ln(1 - \text{CL})}{t_{\text{no errors}}}$$

 $\sigma_{\text{SEU}} = \frac{\text{ER [bit flips/s]}}{\phi [\text{cm}^{-2}\text{s}^{-1}]}$

CBC3 Irradiation Tests Summary SEU Testing of the CBC3 : SEU Rates in I2C Registers

- 12.4 hours of beam time dedicated to measuring the SEU rate in the configuration bits stored in the CBC3's I2C registers.
 - 25 bit flips observed in CBC3 in the beam
 - *measured* SEU cross-section using LIF data : 2.6x10⁻¹² cm²
 - error rate expected at HL-LHC : 1.8×10^{-5} s⁻¹ per chip $\rightarrow 1.5$ errors per day per chip



$$\sigma_{\rm seu} = \frac{\rm ER \ [bit \ flips/s]}{\phi \ [cm^{-2}s^{-1}]}$$

CBC3 Irradiation Tests Summary SEU Rates in I2C Registers : CBC3

- Why are we still seeing SEUs in the I2C registers?
 - RAL identified some nodes of the I2C registers that might still be sensitive to SEUs
 - Write and Reset nodes of the I2C registers
 - Write (Wr)
 - Causes the storage cell to flip to the last write transaction data left in the bus
 - Reset (RN)
 - Causes the storage cell to flip to the default.



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CBC3 Irradiation Tests Summary

Information on tracker layout from TDR



