Front-end, Trigger, DAQ, Data management Poster review (I)

Valerio Re
INFN Pavia and University of Bergamo

14th Pisa Meeting on Advanced Detectors
May 27 – June 1, 2018

A lot is obviously going on…

1) Integrated circuits

- Applications:

Readout of detectors at HL-LHC
Medical imaging (PET)
Nuclear and hadron physics
Neutrino and muon physics

- Technologies:

CMOS (350 nm to the 28 nm CMOS node)
Monolithic pixels (CMOS sensors)
Silicon photonics

- Requirements:

Low noise, high dynamic range, rad-hard, high rate, uniformity of channel performance

2) DAQ, trigger, detector systems

- Applications:

Tracking, triggering and timing at HL-LHC
Luminosity and machine background monitoring
Acquisition of signals from large area PMT and SiPM detectors in dark matter searches
Detector power supply

- Technologies:

Associative memory ASICs for track reconstruction
FPGA for DSP
Front-end and digitizer boards
Algorithms for calibration and parameter extraction

- Requirements:

High sampling speed
Low latency data transmission
Flexibility and capability to interface with diverse detectors and readout chips
Pile-up suppression
Radiation hardness

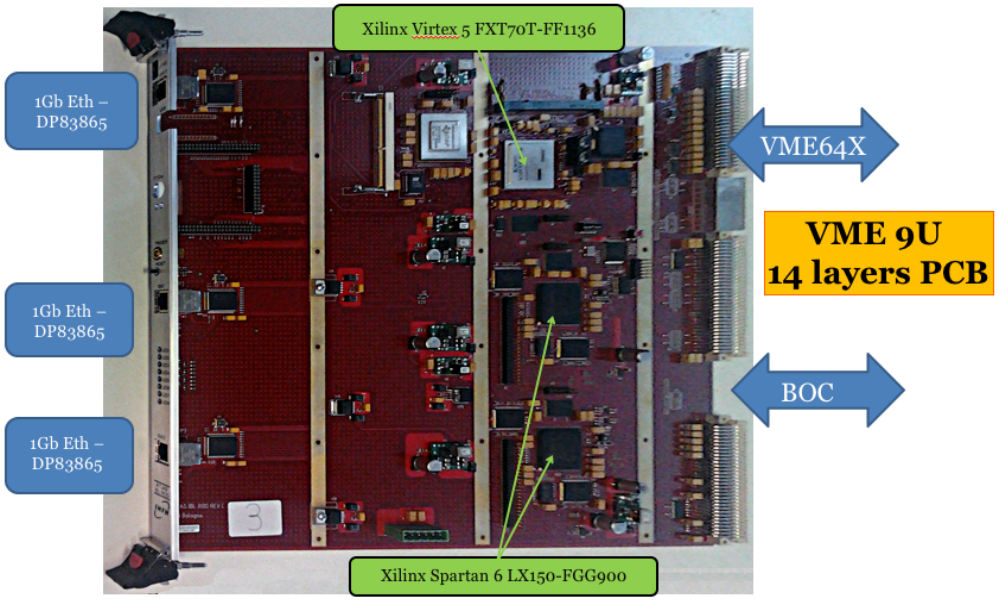
DAQ for tracking and timing at HL-LHC

- **From the Phase-0 DAQ upgrade of entire ATLAS Pixel Detector towards the Phase-2 electronics upgrade** *2'* Speaker: Alessandro Gabrielli (BO)
- **Upgrade of the ATLAS detectors and trigger at the High Luminosity LHC: tracking and timing for pile-up suppression** *1'* Speaker: Mrs. Marianna Testa
- **Design of the ATLAS phase-II hardware based tracking processor** *1'* Speaker: Riccardo Poggi (University of Geneva)
- **Performance of a high-throughput tracking processor implemented on Stratix-V FPGA** Speaker: Mr. Federico Lazzari (Università di Pisa)

From the Phase-0 DAQ upgrade of entire ATLAS Pixel Detector towards the Phase-2 electronics upgrade

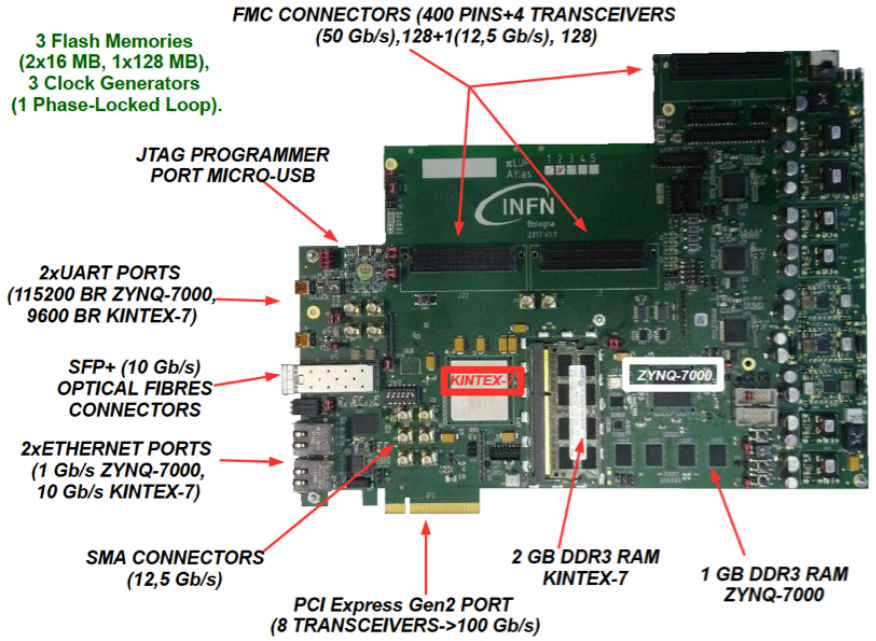
A. Gabrielli[1,2], F. Alfonsi[1,2], G. Balbi[1], G. D'Amen[1,2], D. Falchieri[1], N. Giangiacomi[1,2], R. Travaglini[1]

[1]INFN Bologna, [2] Physics and Astronomy Department University of Bologna (alessandro.gabrielli@bo.infn.it)



From → To

HARDWARE PROPOSAL (π-LUP BOARD)



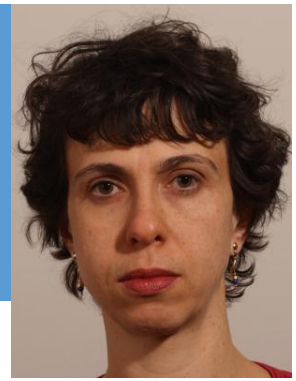
Bit Error Rate of the transceivers I/O (includes the PCI Express Gen2) down to 10^{-14} (10 hours of run)

- **28 nm** FPGAs (xc7z020-1clg484c & xc7k352t-2ffg900c);
- **21 differential bus at 200 MHz DDR** between the FPGAs;
- **Zynq-7000**=>Master with an **ARM Cortex-A9 Dual-Core** processor;
- **Kintex-7**=>Slave with **16 fast links transceivers up to 12,5 Gb/s.**

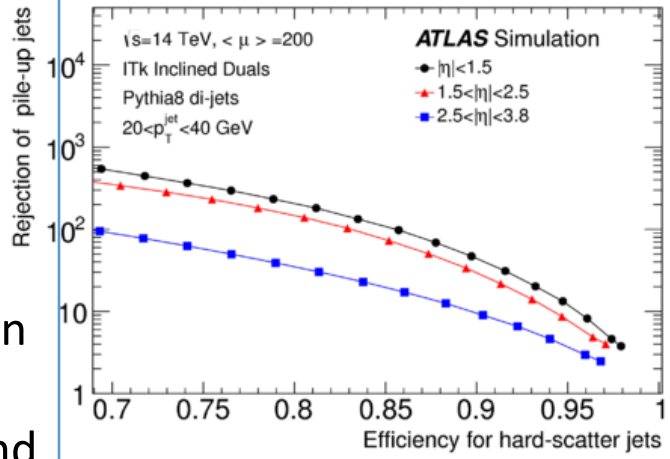
Readout Hardware Upgrade for the ATLAS (Pixel but not only) detector from Phase-0 towards Phase-2

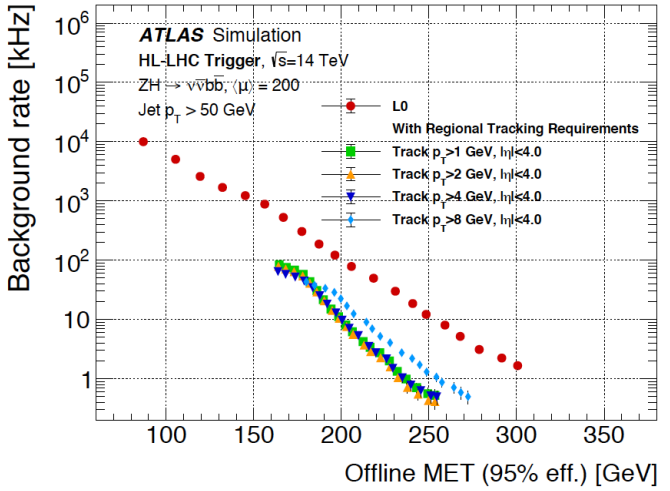
Upgrade of the ATLAS detectors and trigger at the High Luminosity LHC: tracking and timing for pile-up suppression

Marianna Testa, for the ATLAS Collaboration

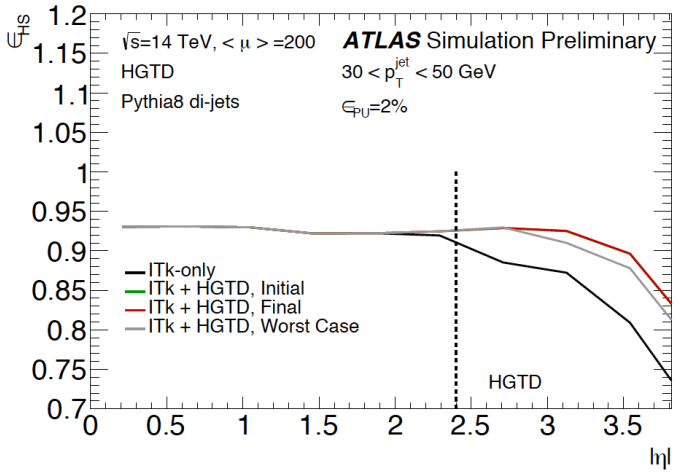


The new all-silicon Inner Tracker (ITk) of the ATLAS detector will be built for the High Luminosity phase of LHC. The finer granularity and the faster readout accompanied by an extension up to $|\eta|<4$ enable powerful pile-up suppression in jets and missing transverse energy (MET) reconstruction, both in the Trigger and in the offline reconstruction.





The proposed High Granularity Time Device (HGTD) improves the pile-up jets rejection in the forward region, degraded due to the vertex merging and larger track impact parameter resolution.



DESIGN OF THE ATLAS PHASE-II HARDWARE-BASED TRACKING PROCESSOR

GOAL

High-luminosity LHC

- Peak luminosity
  - 7.5×10^{34} cm^{-2} s^{-1}
- ATLAS experiment will increase early stage trigger selection power

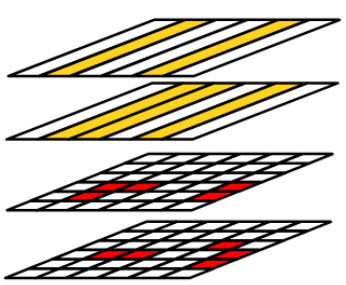
Hardware-based tracking for the trigger (HTT)

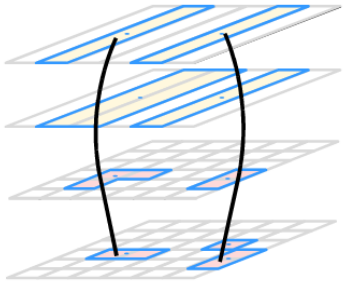
- A combination of
  - Associative Memory ASICs
  - FPGAs
- Provide the software-based trigger system with access to tracking information

Physics Goals

- Allow for reduced pT trigger thresholds
  - Primary lepton selections
- Contribute to pile-up mitigation
  - Essential for hadronic signatures

KEY POINTS





Track Reconstruction

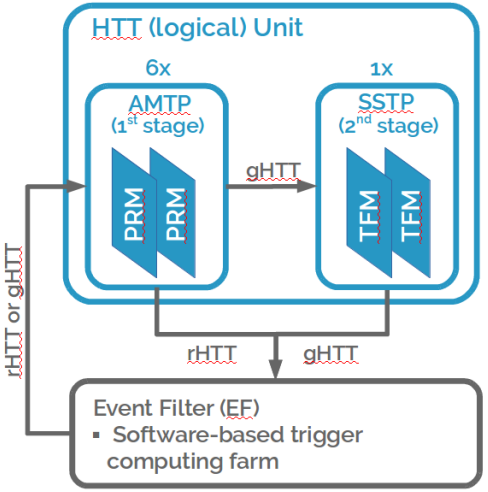
- Pixel and strip detectors
- Cluster aggregation
- Pattern matching and track fitting

Regional tracking

- Hits from 8 outermost ITk layers
- Only 1st stage

Global tracking

- Full ITk coverage
- Two stages



ABOUT ME

Riccardo Poggi

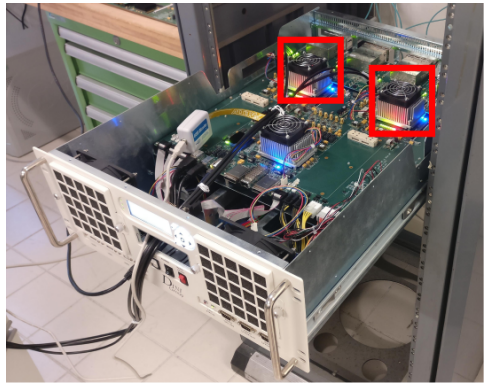
On behalf of the ATLAS Collaboration

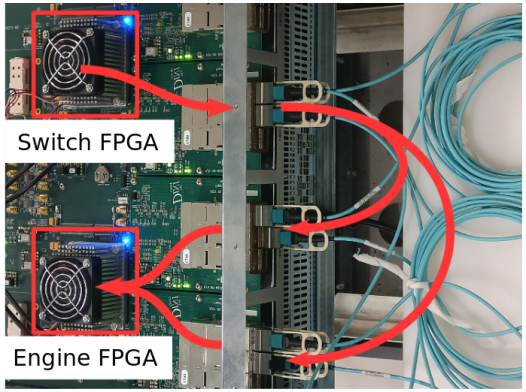
Performance of a high-throughput tracking processor implemented on Stratix-V FPGA

Federico Lazzari Università di Pisa & INFN Sezione di Pisa

WHAT - The "Artificial Retina" tracking processor

- A **high speed, low latency** tracking processor
- Mathematically related to **“Hough transform”**
- Implemented on **FPGAs**
- **Highly-parallel** architecture
- Prototype with 2 FPGAs connected with **optical fibers**



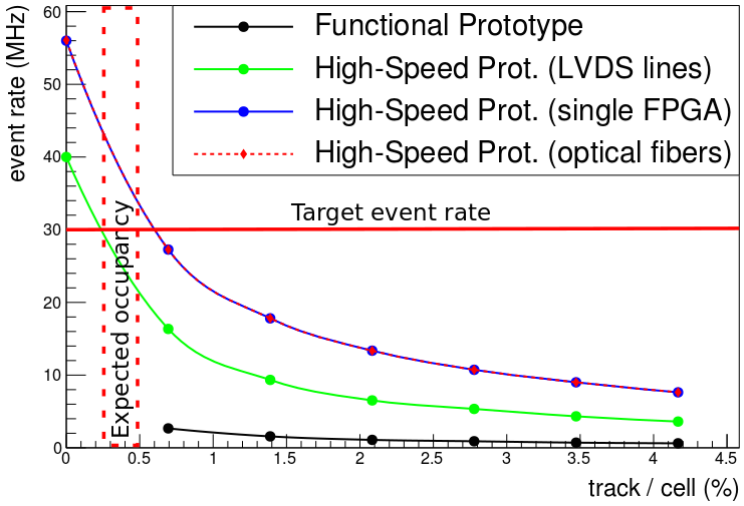


WHY - Tracking at very high rate

- Reconstruction of high quality tracks at beam crossing rate (30 MHz @ LHC)

PROTOTYPE RESULTS

- **High event rate** (> 30 MHz at expected occupancy)
- **Very low latency** (< 500 ns)



AUTHORS

Results achieved by “Retina”, a 3-year project funded by INFN

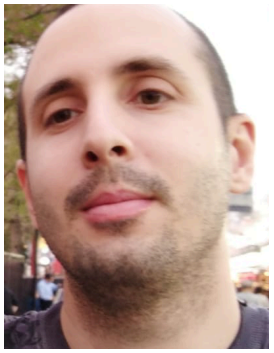
F. Lazzari[1,2], R. Cenci[1,2], P. Marino[2,3], M.J. Morello[2,3], G. Punzi[1,2], L.F. Ristori[4], F. Spinella[2], S. Stracka[2], J. Walsh[2]

[1]Università di Pisa, [2]INFN Pisa, [3]Scuola Normale Superiore di Pisa, [4]FNAL

Trigger and DAQ for muon physics experiments

- **WaveDAQ: an highly integrated trigger and data acquisition system** *1'* Speaker: Luca Galli (PI)
- **Low Latency serial communication for MEG II Trigger system** *1'* Speaker: Marco Francesconi (PI)
- **High performance DAQ for muon spectroscopy experiments** *1'* Speaker: Mattia Soldani (MIB)

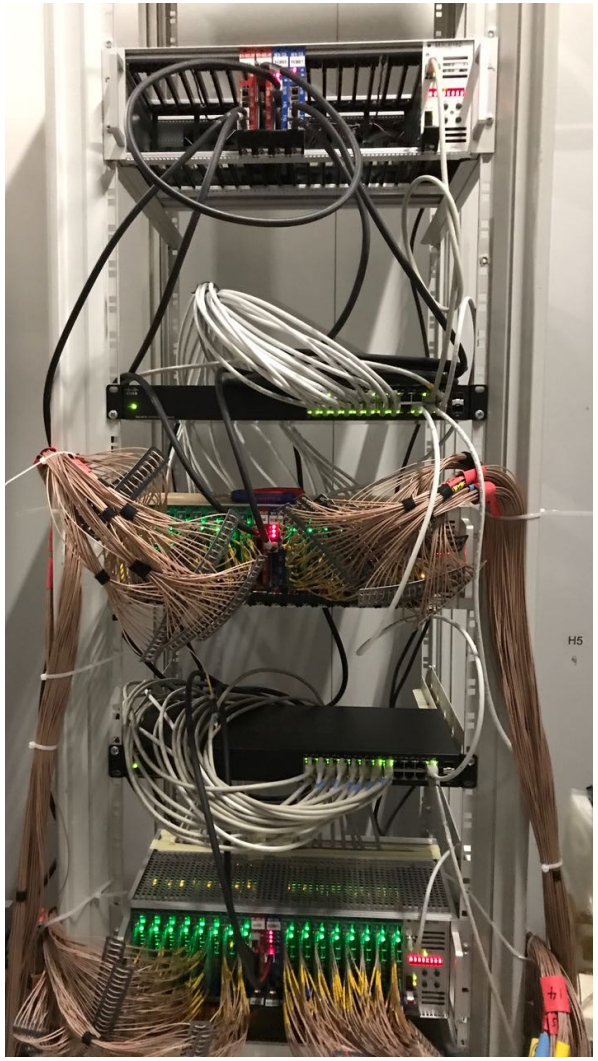
WaveDAQ: an highly integrated trigger and data acquisition system

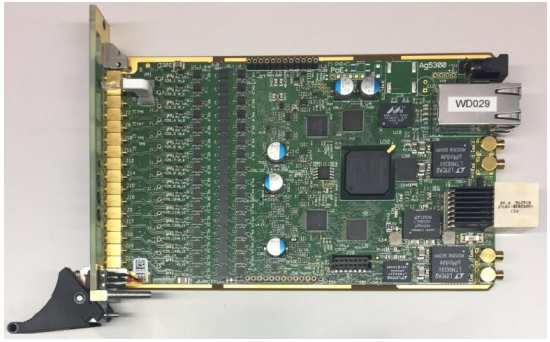


Marco Francesconi[ab], Luca Galli[a], Ueli Hartmann[c], Manuel Meucci[d], Fabio Morsani[a], Donato Nicolò[ab], Stefan Ritt[c], Elmar Schmid[c]

a- Istituto Nazionale di Fisica Nucleare sezione di Pisa b- Università degli studi di Pisa
c -Paul Scherrer Institut d-Istituto Nazionale di Fisica Nucleare sezione di Roma1

WaveDAQ is a full custom, compact and highly integrated trigger and data acquisition system. Despite the decisive urge from the MEG II experiment at PSI aiming at a sensitivity of 6×10−14 on the μ → eγ decay, it is a general purpose device suited for small and medium-sized applications in the range from 16 to about 10000 channels. It exploits the performance of the DRS4 waveform digitiser with a sampling speed programmable from 1 to 5 GSPS; each input channel can supply HV to arrays of SiPMs and provides a front-end amplification chain in the range from 0.5 up to 100 with GHz bandwidth. Input signals are, in parallel to DRS4, digitised at 80 MSPS and used in an FPGA-based trigger; fast linear discriminators associated to each input channel are also used for online reconstruction.
This paper presents the WaveDAQ design principles and the results obtained by a demonstrator in the MEG II pre-engineering run in 2017 fall with a homogeneous LXe detector and a plastic scintillation device both readout by SiPMs and in the tests associated to the ΔE-TOF prototype of the FOOT detector.





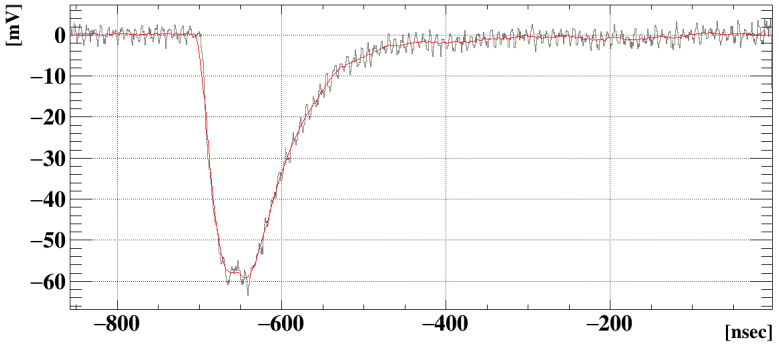
Low Latency serial communication for MEG II Trigger system

Marco Francesconi[ab], Luca Galli[a], Ueli Hartmann[c], Fabio Morsani[a], Donato Nicolò[ab], Stefan Ritt[c], Elmar Schmid[c]

a- Istituto Nazionale di Fisica Nucleare sezione di Pisa
b- Università degli studi di Pisa
c- Paul Scherrer Institut

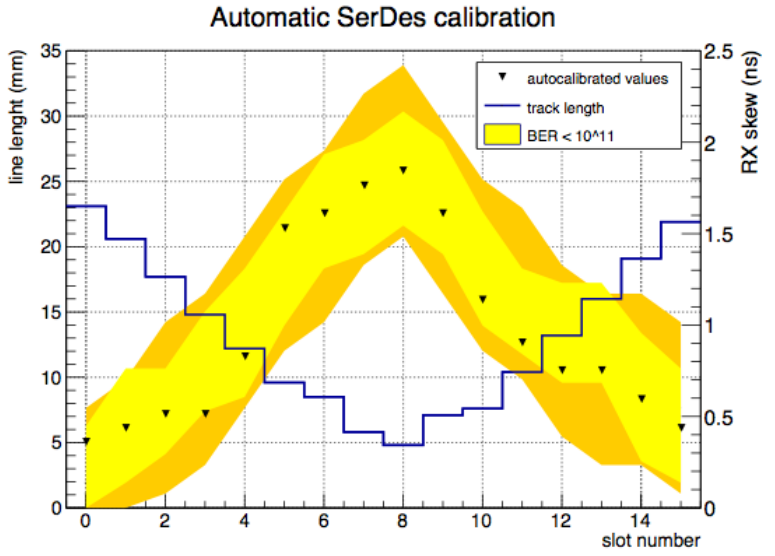
A new **custom-designed** integrated Trigger and Data Acquisition System (TDAQ) is being developed to cope with the increased number of channel of the **MEG II upgrade** Trigger serial connection constitute the **backbone** of the whole system involving up to 800 FPGA Boards in its design configuration

A prototype system composed of 1024 readout channels has been tested with **MEG II Liquid Xenon Detector**.
Total trigger latency can be easily measured to be **700 ns** by pulse position in DRS4 chips.
Out of those **14 clock ticks are due to trigger data transmission including track length**.



An automatic calibration FSM

Having to calibrate thousand of serial links, we implemented a dedicated Finite State Machine to select the appropriate control signals for a stable transmission.



The calibrated delay values anticorrelate well with backplane track length. The Bit Error Rate contour is shown in yellow for comparison.

Contact: marco.francesconi@pi.infn.it

High performance DAQ for muon spectroscopy experiments

M. **Soldani**[1-2] (mattiasoldani93@gmail.com), G. **Ballerini**[1-2], M. **Bonesini**[1-3], F. **Fuschino**[4-5], A. **Hillier**[6], K. **Ishida**[7], E. **Mocchiutti**[8], P. **Oliva**[9-10], L. **Rignanese**[5-11], L. **Tortora**[12], A. **Vacchi**[7-8-13], E. **Vallazza**[8], M. **Clemenza**[1-3]

[1] INFN Milano Bicocca [2] Università degli Studi dell'Insubria [3] Università degli Studi di Milano Bicocca [4] INAF/OAS Bologna [5] INFN Bologna [6] RAL [7] RIKEN [8] INFN Trieste [9] INFN Cagliari [10] Università degli Studi di Sassari [11] Università degli Studi di Bologna [12] INFN Roma Tre [13] Università degli Studi di Udine

Beam from the RIKEN-RAL Muon Facility @ ISIS Neutron and Muon Source

- extracted from ISIS proton synchrotron
- (20,120)MeV/*c* muons
- momentum tuning with a sensitivity of 1MeV/c
- 2 successive spills (~100ns wide) at ~37.5Hz
- 10^4 muons per spill (with μ^- @ ~50MeV/*c*)

FAMU

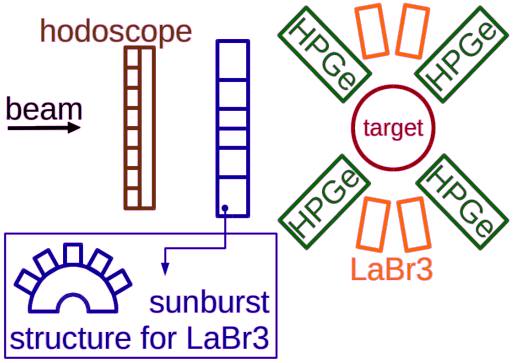
Fisica degli Atomi MUonici

high time resolution spectroscopy: study of out-of-spill X-ray emission resulting from muon transfer between muonic hydrogen and higher-*Z* elements in gaseous mixtures, with the aim of measuring the hyperfine splitting in the ground state of muonic hydrogen

CHNET_TANDEM

Cultural Heritage NETwork

Tecniche Analitiche Non Distruttive per l'archEoMetria



high energy resolution spectroscopy: study of X-ray emission of decaying muonic atoms in metallic artifacts - internal composition analysis with good depth resolution via beam momentum tuning

digitizers-based readout in order to meet many different needs...

	CAEN V1724	CAEN V1730C	CAEN V1742
nr. of channels	8	8	32+2
resolution	14 bit	14 bit	12 bit
input range [Vpp]	10 (custom version)	0.5 or 2 (selectable for each channel)	1
sampling rate (simultaneously on each channel) [MS/s]	100	500	750 to 5k (selectable)
memory depth	512 kS/ch	640 kS/ch	128 ev/ch 1kS/ev
single channel settings	yes	yes	no
comments	wide range needed for HPGe preamplified signals	high speed good for fast spectroscopy setup	large nr. of channels needed for hodoscopes (3 in beam focus search config.)

Electronics for HPGe: ORTEC preamp & ORTEC 672 amplifier (shaping in 500ns) for GLP; GALILEO preamp & ORTEC 579 fast-filter amplifier (shaping in 250ns) for GEM-S

BEAM MONITORING HODOSCOPES

- one with 64 1x1mm^2 squared fibers with EMA & SiPM-based readout - AdvanSiD with side 3mm (cell side40µm)
- 2 with 64 3x3mm^2 squared fibers with Al wrap & SiPM-based readout - Hamamatsu S12752 with side 3mm (cell side 25µm)

FAST SPECTROSCOPY

- many $LaBr_3$(Ce) crystals - decay time 16ns
  - ↘ PMT-read with Hamamatsu R11265-200
  - ↘ SiPM-read with various sensors
- one standard cylindrical 1"×1" BrilLanCe 380

HI-RES SPECTROSCOPY

ORTEC HPGe: one GLP and one GEM-S from INFN Milano Bicocca, one GEM-S and one GMX from RIKEN-RAL Muon Facility

- ↘ FWHM < 1keV @ 122keV for all the detectors

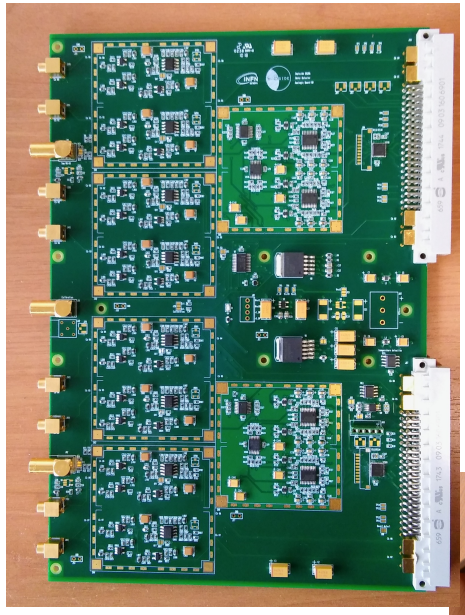
PMT and SiPM readout in dark matter experiments: front-end boards with ADC, TDC,…

- **Front-end electronic system for large area photomultipliers readout** *1'* Speaker: Paolo Musico (GE)
- **A low cost, high speed, multichannel Analog to Digital converter board** *1'* Speaker: Paolo Musico (GE)

Front-end electronic system for large area photomultipliers readout

B. Bottino, A. Caminata, M. Cariello, M. Cresta, S. Davini, **Paolo Musico**, M. Pallavicini, G. Testera

I.N.F.N. Genova – via Dodecaneso, 33 – 16146 – GENOVA (Italy)



A front-end electronic system for large area photomultipliers (PMT) has been developed. Connection to the PMT can be made by a single cable, useful to minimize cabling in a underwater detector.

A front-end board houses 8 channels each one is composed by a preamplifier and a leading edge discriminator. Up to 8 front-end boards can be housed in a crate, giving a modularity of 64 channels.

A controller board is needed to setup and monitor the front-end parameters.

This board implements also scalers and time to digital converters (TDC) with time over threshold (TOT) capability.

Timing synchronization can be made with external clock (GPS driven) or using the WhiteRabbit communication protocol.

The communication with the outside world is made using a standard gigabit Eth

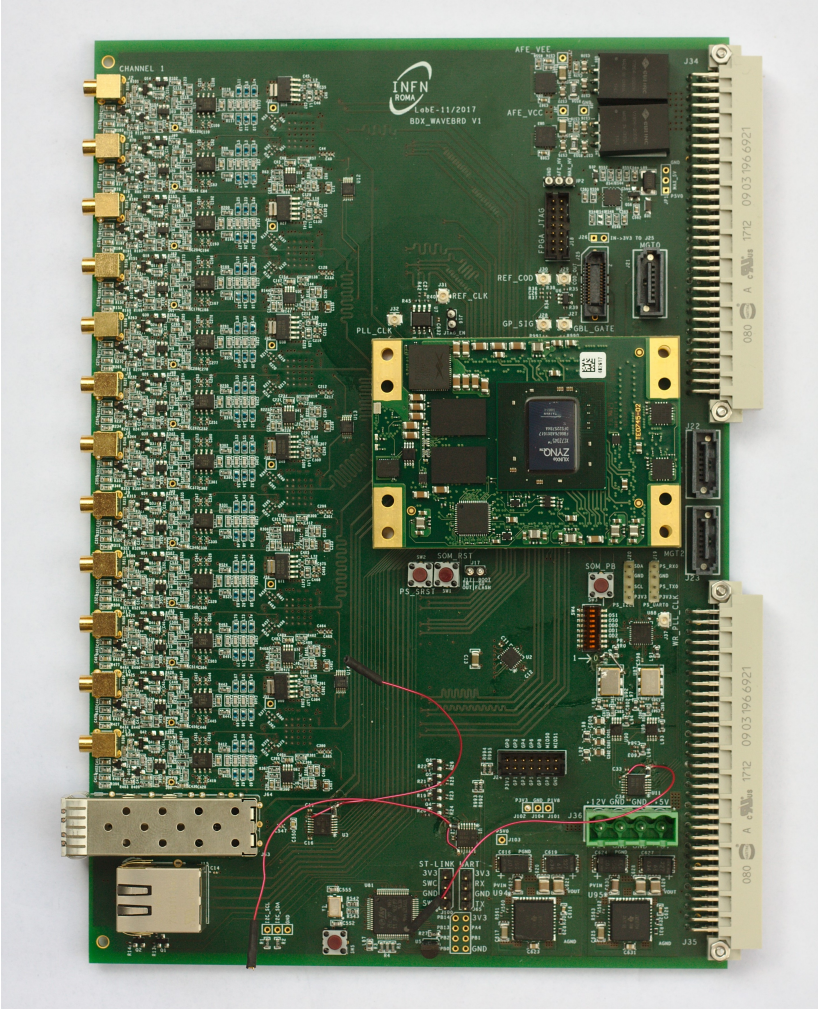
The system is now prototyped and test are in progress.

A low cost, high speed, Multichannel Analog to Digital converter board

F. Ameli[1], M. Battaglieri[2], M. Bondì[3], M. Capodiferro[1], A. Celentano[2], T. Chiarusi[4], G. Chiodi[1], R. Lunadei[1], M. De Napoli[3], L. Marsicano[2], **Paolo Musico[2]**, L. Recchia[1], D. Ruggieri[1], L. Stellato[1]

1) I.N.F.N. Roma – Piazzale A. Moro, 2 – 00185 - ROMA (I)
2) I.N.F.N. Genova – via Dodecaneso, 33 – 16146 – GENOVA (I)
3) I.N.F.N. Catania – via S. Sofia, 64 – 95123 – CATANIA (I)
4) I.N.F.N. Bologna – viale C. Berti Pichat, 6/2 – 40127 – BOLOGNA (I)

A highly configurable digitizer board including 12 complete acquisition channels has been developed: the analog to digital converters (ADC) components can be chosen to tailor the specific application, ranging from 12 bit 65 MHz up to 14 bit 250 MHz.
In this application the front-end circuit is dedicated to the Silicon Photomultipliers (SiPM) of the BDX detector.
The control is made by a commercial FPGA module to guarantee the scalabilty of the system.
Having the possibility to choose the ADC and the "size" of the FPGA on the control module the price can be reduced to the minimum for a given application.
The board has been thought to be used in a triggerless system: all data passing some programmable selection criteria are sent out to a computing farm using gigabit Ethernet standard.
The board permit the time synchronization using various methods including GPS and White Rabbit.
The configurability of the board and the various options implemented permit to use it in a triggerless data acquisition system.
Up to 240 channels can be hosted in a single 6U crate.



Beam monitoring, detector power supply

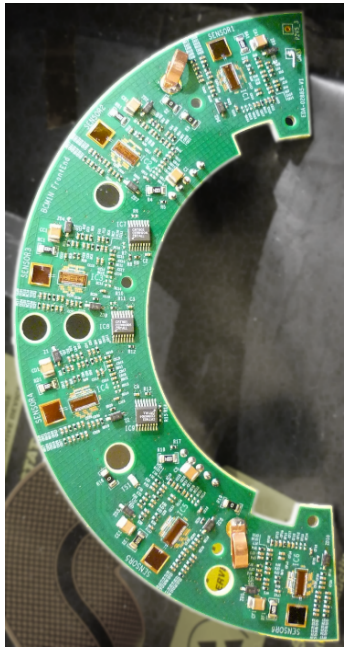
- **Upgraded back-end electronics for the CMS Fast Beam Conditions Monitor** *1'* Speaker: Nicolò Tosi (BO)
- **Development of a high voltage power supply for detectors using photo-diode** *1'* Speaker: Ms. SHARMILI RUDRA (Seacom Engineering College)

Upgraded back-end electronics for the CMS Fast Beam Conditions Monitor

Nicolò Tosi, INFN Bologna, CMS collaboration

In the CMS experiment, the Fast Beam Conditions Monitor (BCM1F) provides an online, bunch-by-bunch measurement of Luminosity and Machine Induced Background. An upgraded back-end electronics has been developed for the BCM1F, based on the µTCA standard.

BCM1F



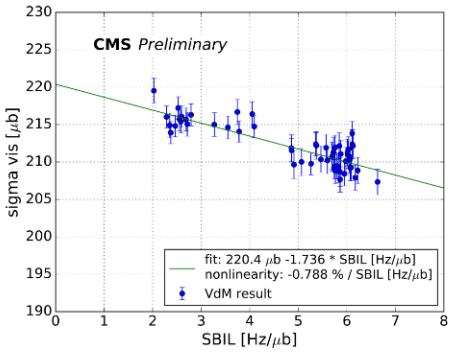
Higher LHC luminosity

↓

Increasing occupancy

↓

Loss of linearity



Upgraded Back-End

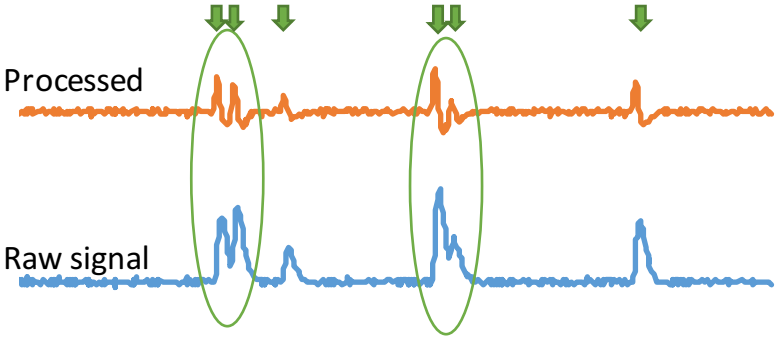
1.2 GS/s ADC + FPGA Digital signal processing

↓

Detection of overlapping signal pulses

↓

Improved detector linearity, better Lumi measurement



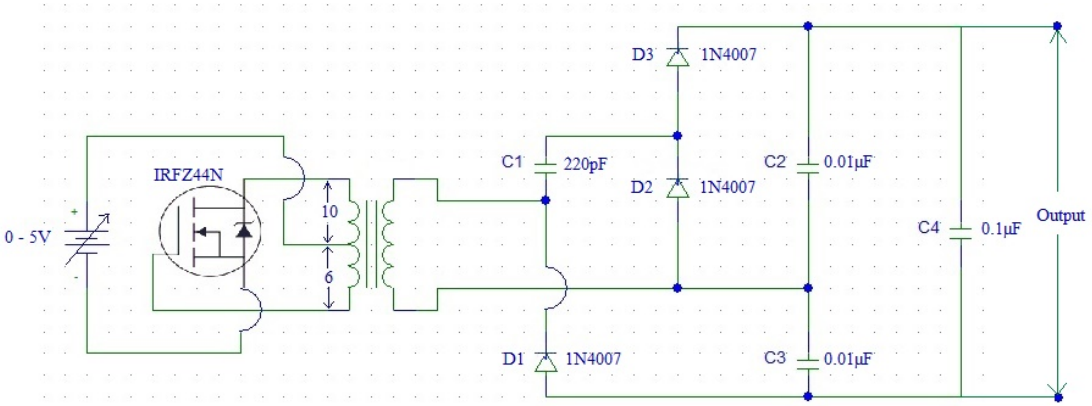
Development of a high voltage power supply for detectors using photo-diode

Sharmili Rudra*, Prabir Ghosh, Tejaswita Kumari, Atanu Chowdhury, Soumya Sen

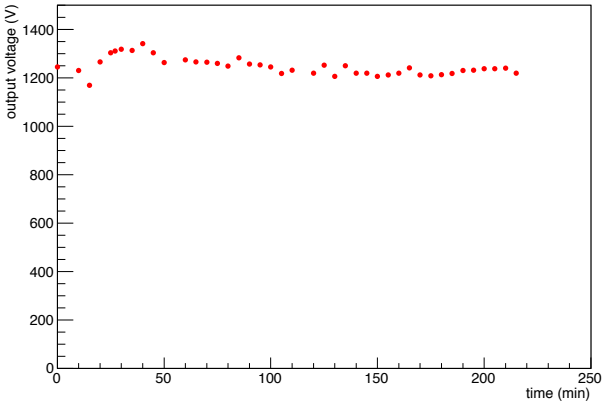
Seacom Engineering College, JL-2: Jaladhulagori (Via Andul Mouri), Sankrail, Howrah-711 302, West Bengal, India

e-mail: *sr.phys@gmail.com

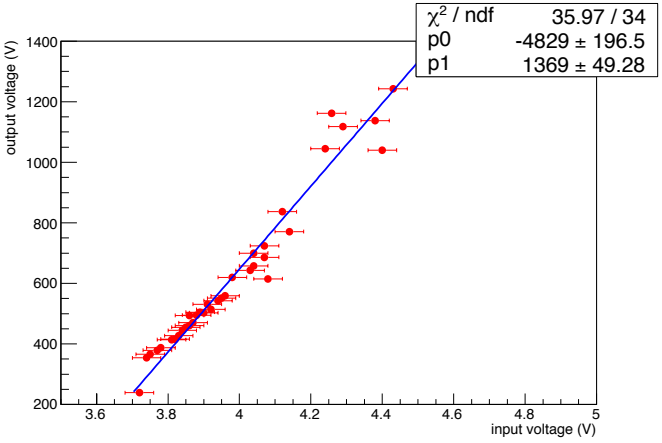
- **A circuit is designed using photo-diode in photo-voltaic mode to convert solar energy into electrical energy.**
- **Input voltage to the transformer is varied using a pot and the output voltage is measured. The output voltage increases linearly with the input voltage. In this set-up a voltage up-to 1250 V is achieved.**
- **In a continuous test of 200 minutes the output voltage remains almost constant at 1250 V within a RMS fluctuation of 2.9%.**
- **The output voltage will be used to power PMT of scintillator detector.**



Circuit diagram



Stability check



Linearity test

FPGA radiation hardness: experimental studies and rad-hard methods

- **Radiation study of FPGAs with neutron beam for the COMET Phase-I** *1'* Speaker: Mr. Yu Nakazawa (Osaka Univ.)
- **Self-Contained Configuration Scrubbing in Xilinx FPGAs for On-detector Applications** *1'* Speaker: Dr. Raffaele Giordano (University of Naples and INFN)

Radiation study of FPGAs with neutron beam for COMET Phase-I

Yu Nakazawa[1], Yuki Fuji[2], Eitaro Hamada[2], MyeongJae Lee[3], Yuta Miyazaki[4], Akira Sato[1], Kazuki Ueno[2], Hisataka Yoshida[1], Jie Zhang[5]

[1]Osaka University, Osaka, Japan; [2]KEK, Tsukuba, Japan; [3]IBS/KAIST, Daejeon, Korea; [4]Kyushu University, Fukuoka, Japan; [5]IHEP, Beijing China

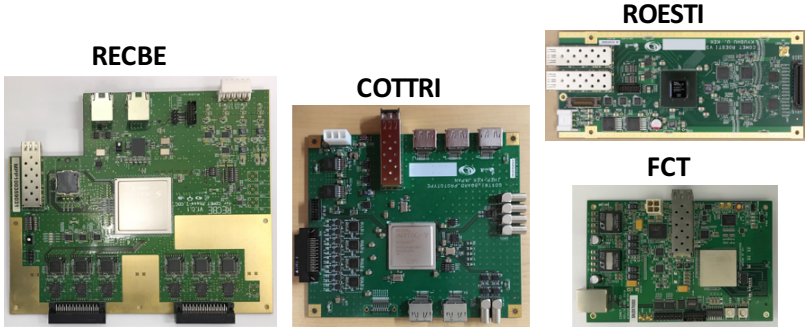
Neutron fluence in COMET Phase-I

: 1.0 x 10^{12} neutron/cm^2 (1MeVeq)

- 150 days measurement time
- safety factor of 5~10

Front-end electronics

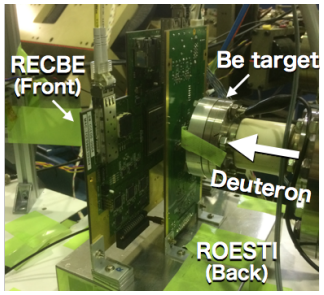
- FPGAs are used for digital signal processing



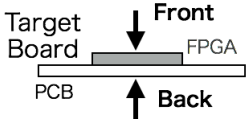
	FPGA	FPGA Size [mm]
RECBE	Virtex-5 (XC5VLX155T-1FFG1738C)	35 x 35
ROESTI	Artix-7 (XC7A200T-2FBG676C)	27 x 27
COTTTRI	Artix-7 (XC7A200T-2FFG1156C)	35 x 35
FCT	Kintex-7 (XC7K160T-2FFG676C)	27 x 27

Neutron irradiation test

- TANDEM @Kobe Univ.
  - 2 MeV neutron beam
  - Flux: 1.9 MHz/cm^2/μA @ 10 cm from the source
- Evaluation Item
  - Soft error rate
    - CRAM SEU & URE
    - BRAM SEU & MBE
  - Recovery system
  - TMR operation

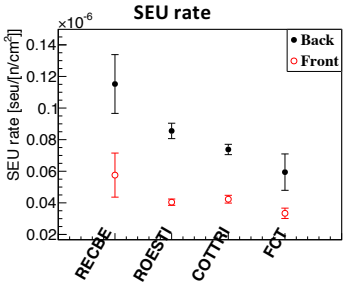


Definition of incident angle



Result

- No permanent damage
- Success
  - Auto-recovery system
  - TMR
  - Re-downloading function
- Incident angular dependence

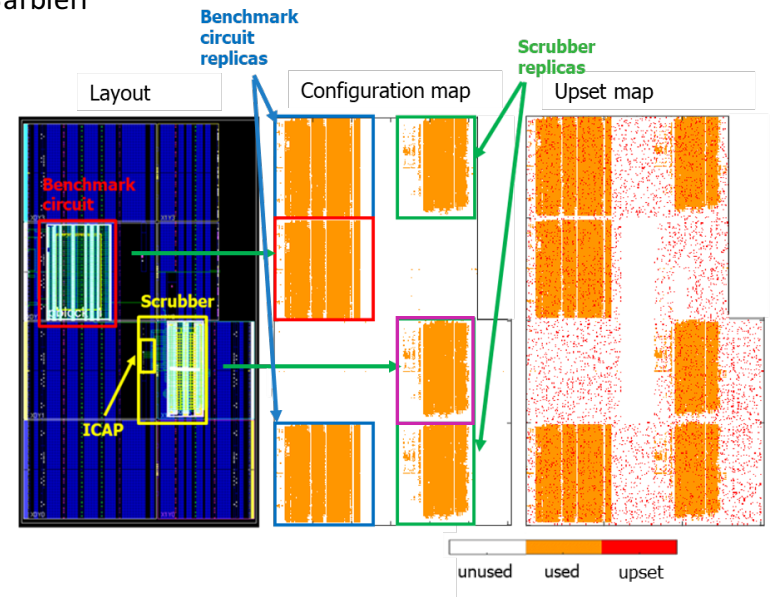


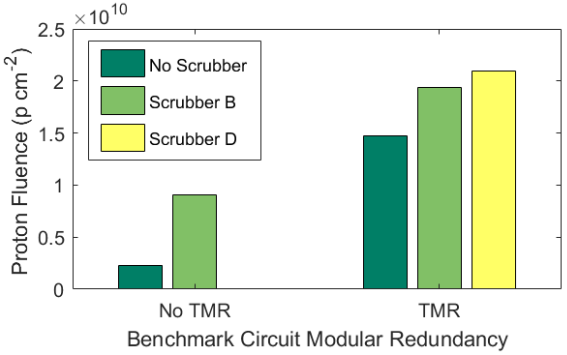
- FPGA dependence of CRAM SEU rate was measured.
- Dead time by soft errors can be suppressed by auto-recovery systems.

Self-Contained Configuration Scrubbing in Xilinx FPGAs for On-detector Applications

R. Giordano, S. Perrella, D. Barbieri

- Radiation-induced configuration upsets limit usage of SRAM-based FPGAs on-detector
- This work is about a self-correcting methodology for Xilinx FPGAs
  - Based on redundant configuration, no external memory needed
  - Corrects configuration upsets in the whole device, even multiple upsets per frame (MBUs)
  - Tiny logic footprint: 500 slices in a 7-Series FPGA
  - Portable on most Xilinx devices
- Results from a beam test w/ 62-MeV protons on a benchmark circuit show
  - accumulated proton fluence before failure improves up to 290%
  - total power consumption is kept stable within 6%





www.roalproject.it

CMOS readout chips and sensors for HL-LHC

- **FATALIC: a fully integrated electronics for the ATLAS tile calorimeter at the HL-LHC** *1'* Speaker: Mr. Romain Madar (Université Clermont Auvergne, CNRS/IN2P3, LPC)
- **Test of a New Octal Amplifier Shaper Discriminator Chip for the ATLAS MDT Chambers at HL-LHC** *1'* Speaker: Dr. Hubert Kroha (Max-Planck-Institut fuer Physik)
- **Towards the large area HVCMOS demonstrator for ATLAS ITk** *1'* Speaker: Ms. Mridula Prathapan (Karlsruhe Institute of Technology)
- **First test results of the CHIPIX65 asynchronous front-end connected to a 3D sensor** *1'* Speaker: Luigi Gaioni (University of Bergamo)

FATALIC: a fully integrated electronics readout for the ATLAS tile calorimeter at the HL-LHC

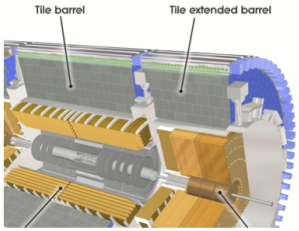
S. Angelidakis, W. Barbe, R. Bonnefoy, C. Fayard, **R. Madar**, S. Manen, M-L. Mercier, E. Nibigira, L. Royer, A. Soulier, D. Pallin, F. Vazeille, R. Vandaële

Laboratoire de Physique de Clermont-Ferrand, Université Clermont Auvergne, CNRS/IN2P3, Clermont-Ferrand, FRANCE

FATALIC is based on a **130nm CMOS technology** and performs the complete processing of the signal (amplification, shaping, digitisation) on a wide range (25 fC to 1.2 nC). The innovative part of this work is to have **a current-reading ASIC** with 3 gains **including a dynamic gain switch**. The chip is made of current conveyors, shapers, 12-bits pipeline analog-to-digital converters.

ATLAS Tile Calorimeter

Sampling calorimeter with scintillating tiles.

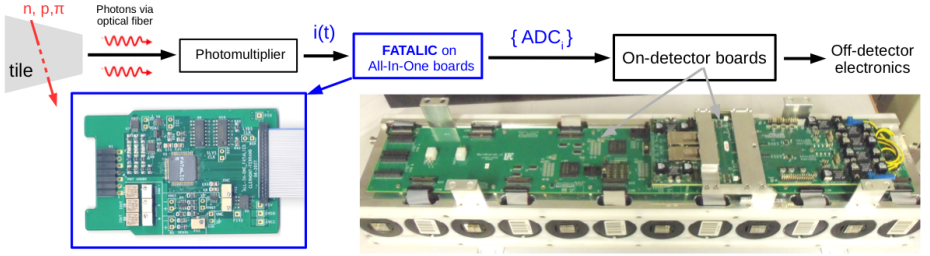


What? Measuring energies from 0.1 to 1000 GeV

Why? Jets leave up to 40% of their energy in this calorimeter

500 000 tiles • ≈ 5 500 cells • 2 PMs/cell

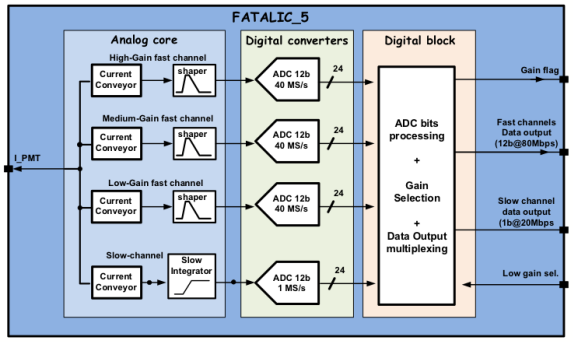
Schematic view of the detection chain



The light produced by tiles is converted by a photo-multiplier (PM) into electric current $i(t)$, which is processed by the *readout electronics* sending ADC counts to the rest of the chain.

Overview of FATALIC readout

ASIC CMOS 130 nm • shaping • digitisation • 3 gains • 12-bits ADC • integrator

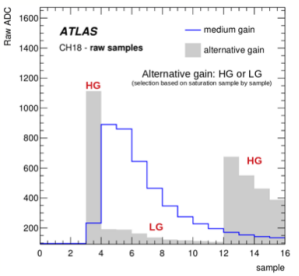


ASIC specifications

Physics (*fast* channel)
$Q = 25\,\text{fC} - 1.2\,\text{nC}$
$\sigma_Q \leq 12\,\text{fC}$
Linear at 1% up to 0.8 nC
25 bits at 40 MHz
Calibration (*slow* channel)
$I = 0.5\,\text{nA} - 11\,\mu\text{A}$
$\sigma_I \leq 0.25\,\text{nA}$
$t_{\text{meas}} = 10\,\text{ms}$

Dynamic gain switch

How to fit the bandwith limitations (25 bits) with the precision of 3 gains (12-bits)?



Sample-by-sample gain selection allows to output only the 2 gains which are relevant

A New Octal Amplifier Shaper Discriminator Chip for the ATLAS MDT Chambers at HL-LHC

S.Abovyan, V.Danielyan, M.Fras, O.Kortner, H.Kroha, R.Richter, Y.Zhao - Max-Planck-Institut for Physics, Munich, Germany

A.Baschirotto, M.De Matteis, F.Resta - University of Milan-Bicocca, Milan, Italy

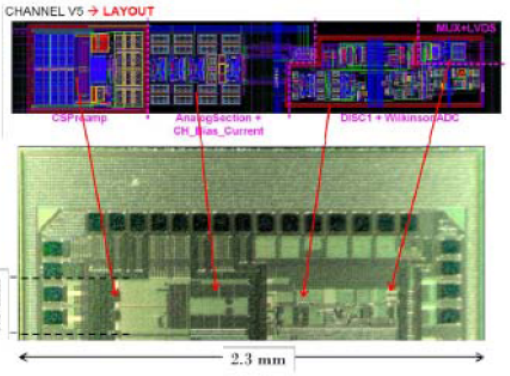
The task

For the luminosity upgrade of the LHC (2025), the ATLAS Muon Spectrometer needs to be prepared for the higher data rates due to background γ radiation by increasing the bandwidth of the readout. In addition, unlike in the past, the data recorded in the MDT drift tubes will be used to sharpen the p_T selection of the the first-level muon trigger and must be available to the trigger processors after a latency of 10 μs.

As a consequence, the complete readout electronics of the 1050 Muon Drift Tube (MDT) tracking chambers needs to be replaced. For this purpose a new Amplifier-Shaper-Discriminator (ASD) chip in modern radiation hard technology had to be designed. It is now ready for mass production of 60000 chips.

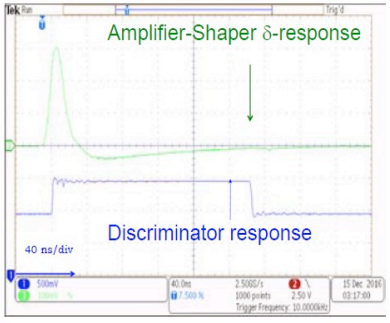
18 prototype chips tested. High uniformity of channel performance, much improved w.r.t. present chip.

Design of a new ASD chip in 130 nm Global Founderies (former IBM) CMOS technology

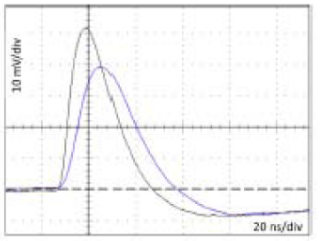


Signal shape

No feedback from signal to analog part.
Prevented by isolation of both in the substrate.

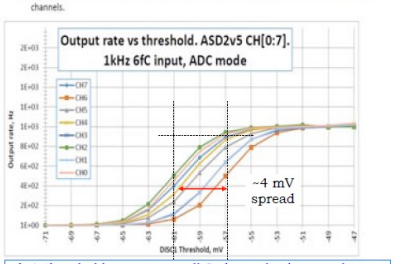


Signal rise time



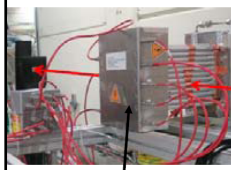
Signal peaking time of 12 ns **without** capacitive load as required (**with 60 pF** capacitive load 15 ns.)
Typical capacitance load of ATLAS MDTs 30 pF.
The gain of the new chip is increased by a **factor 2.**

Threshold scan

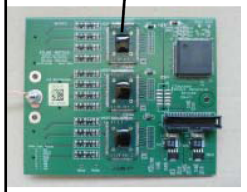


→ A threshold sweep over all 8 channels shows only 4 mV variation.
→ All 8 channels very close to each other

Test on a MDT chamber



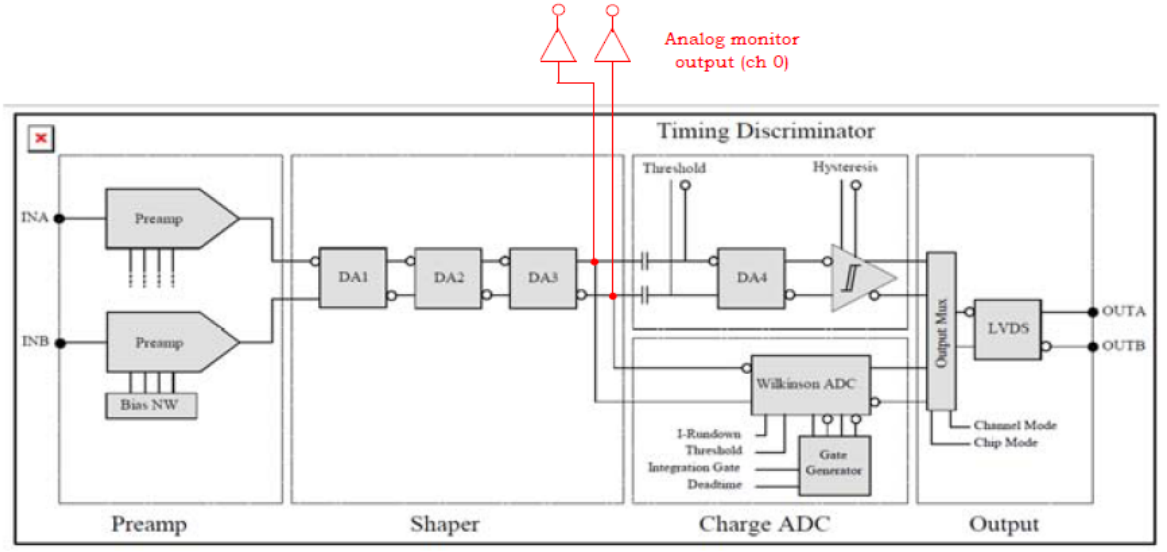
15 mm ∅ drift tube detector in a muon beam and under high γ irradiation at CERN.



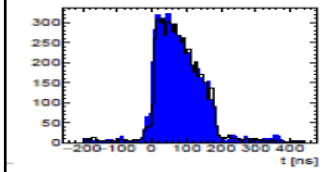
Readout board with 3 new ASD chips and a TDC chip.

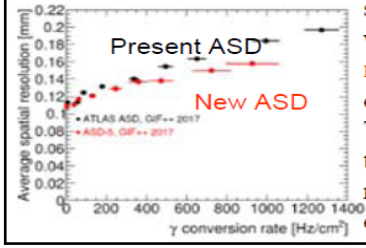
Survives X-ray irradiation of at least 1 MRad, 100 x requirement

Functional diagram of the ASD using bipolar shaping



Beam test results

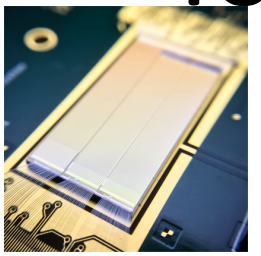


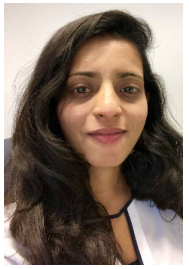


The drift time spectra with the **present ASD** and with the **new ASD** agree very well.

Average drift tube spatial resolution with **present** and **new ASD** as a fct. of the γ count rate. The higher gain of the new ASD reduces time-slewing esp. at high γ rates.

Towards the large area HVCMOS demonstrator for ATLAS ITk



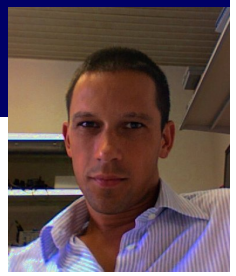


M. Prathapan[6], M. Benoit[4], R. Casanova[3], D. Dannheim[1], F. Ehrler[6], E. Vilella[7], M. Kiehn[4], A. Nürnberg[6], P. Pangaud[2], R. Schimassek[6], A. Weber[5,6], W. Wong[4], H. Zhang[6], I. Perić[6]

[1]CERN, [2]CPPM Marseille, [3]IFAE Barcelona, [4]University of Geneva, [5]University of Heidelberg, [6]KIT Karlsruhe, [7]University of Liverpool

- High Voltage CMOS sensors use commercial CMOS technology for particle detection which makes them cost effective in comparison to the hybrid sensors.
- HVCMOS sensors are fully monolithic, which means the readout electronics is embedded in the sensor chip.
- This contribution presents the progress that has been made towards the final HVCMOS demonstrator targeting the requirements of ATLAS inner tracker
- ATLASpix1 is the first large area prototype in 0.18µm process.
- ATLASpix1_M2 is the proof-of-concept for a novel readout scheme called "Content Addressable hit Buffer (CAB)" readout. The design details of ATLASPix1_M2 will be presented in this contribution.
- ATLASPix2 introduces new ideas for smart pixel grouping to achieve higher spatial resolution. The control unit of ATLASPix2 has several new features such as partial sorting algorithm for excellent readout efficiency at high particle hit rates.
- ATLASpix3 is the planned to be the sensor chip which will be used for module construction. ATLASpix3 test chip introduces double ToT storage concept per hit buffer.
- This poster gives an insight into the design details of ATLASPix series. The test beam measurements on ATLASpix1 shows 99.5% detection efficiency.

First test results of the CHIPIX65 asynchronous front-end connected to a 3D sensor

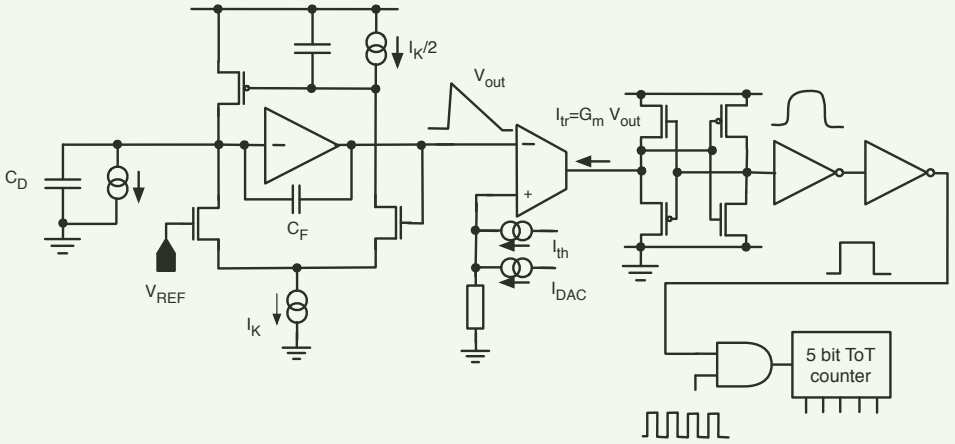


L. Gaioni[1,3], F. De Canio[1,3], M. Manghisoni[1,3], L. Ratti[2,3], V. Re[1,3], M. Sonzogni and G. Traversi[1,3]

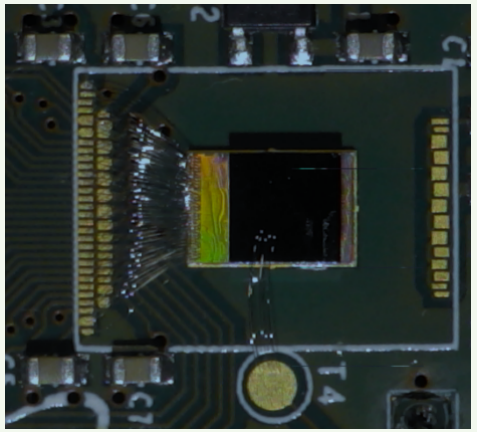
[1]University of Bergamo, [2]University of Pavia, [3]INFN Pavia

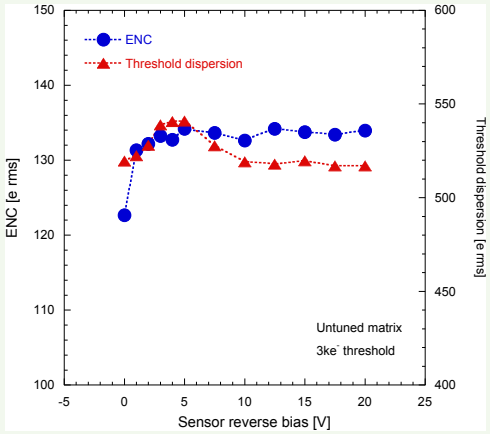
A **low noise, asynchronous front-end** has been designed and integrated in a small scale demonstrator in the framework of the CHIPIX65 project, aiming at the development of an innovative readout chip for the high luminosity upgrades of LHC. The demonstrator has been bump-bonded with **3D pixel sensors** developed by FBK.

In this work, the **design** and **experimental characterization** of the asynchronous architecture is reported.



Schematic diagram of the asynchronous front-end integrated in the CHIPIX demonstrator





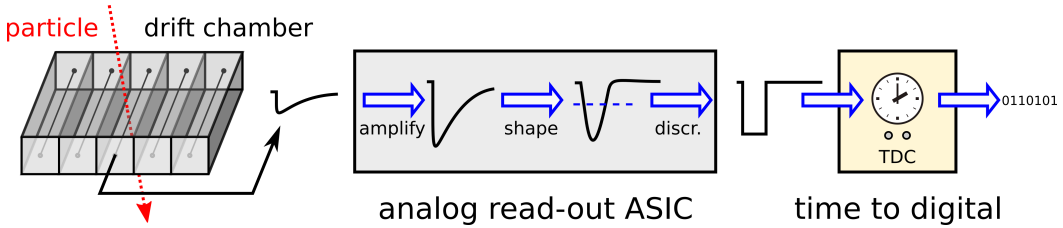
Main analog parameters have been investigated as a function of the sensor reverse bias voltage

CMOS ASICs for particle physics

- **Front-End Electronics of the Electromagnetic Barrel-Calorimeter for the PANDA Target Spectrometer*** *1'* Speaker: Mr. Christopher Hahn (II. Physikalisches Institut, Justus-Liebig-Universität, Gießen)
- **Towards new Front-End Electronics for the HADES Drift Chamber System** *1'* Speaker: Mr. Michael Wiebusch (Goethe-University Frankfurt)
- **Characterization and first field results of a new 64ch custom front-end ASIC for GEM readout** *1'* Speaker: Maxim Alexeev (TO)
- **A new readout electronics for the LHCb Muon Detector Upgrade** *1'* Speaker: Davide Brundu (CA)

Towards new Front-End Electronics for the HADES Drift Chamber System

Michael Wiebusch
Institut für Kernphysik, Goethe-Universität Frankfurt, Germany,
for the HADES Collaboration



- The HADES experiment (heavy ion collisions with fixed target) employs drift chambers for track+momentum reconstruction and particle identification via specific energy loss

- The current front-end electronics, based on the ASD8 ASIC, will be replaced by new hardware with multi-hit TDCs and more stable analog read-out to cope with the high rates and occupancies expected at the new SIS-100 accelerator at GSI/FAIR, Darmstadt

- PASTTREC (a straw tube read-out ASIC, dev. by JU Krakow) is a promising replacement candidate for the legacy ASD8 chip

- PASTTREC was tested for compatibility with the HADES drift chambers in various scenarios including a beam test

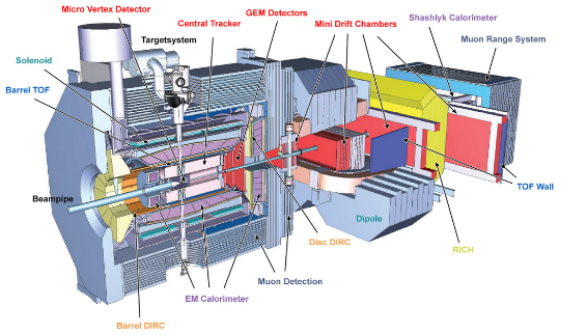
- The measured data is compared to a 3D GARFIELD simulation of the HADES drift cells

Front-End Electronics of the Electromagnetic Barrel-Calorimeter for the PANDA Target Spectrometer

K.T. Brinkmann, M.Moritz, C.Hahn, R. Schubert, U. Thöring, M. Straube, M. Peter,
B. Wohlfahrt and H.-G. Zaunick for the PANDA-Collaboration

2nd Physics Institute, Justus-Liebig-University Giessen, Germany

The planned PANDA detector @ FAIR

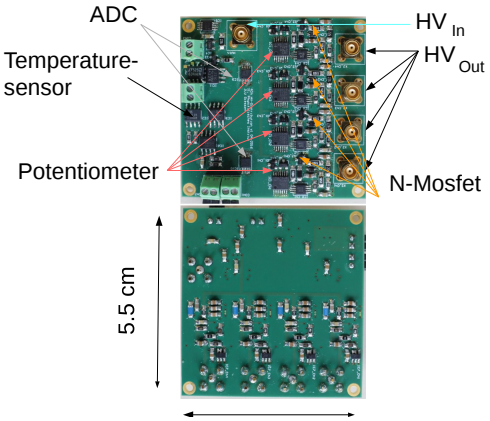


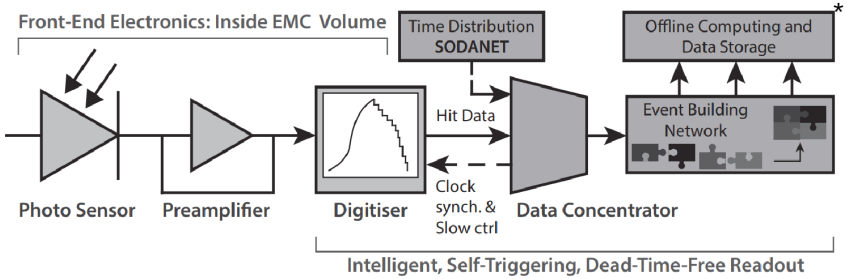
Barrel EMC:

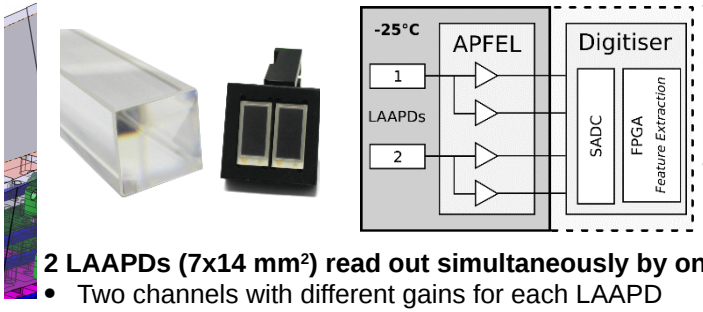
- 15552 $PbWO_4$ crystals (length: 20 cm ~ 22 X_0)
- 13 crystal types (different degree of tapering)
- Type 1: most tapered, type 13: least tapered
- Operation temperature: -25 °C

High-Voltage adjustment through specialized electronics

- Voltage controlled by adjustment of a N-MOSFET
- Seperately configurable channels (for each LAAPD)
- Precision of adjustment up to exactly 0.1 V
- Voltage and current can be measured
- SPI /I2C Interface
- Voltage adjustment electronics inside detector volume but outside of cooled volume
- Recent prototyping showed proof-of-concept by high-precision measurements of APD characteristics







SADC:

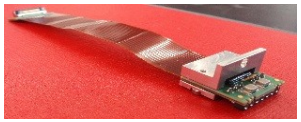
- 50/125 MHz
- No additional timing branch

FPGA:

- Online pulse data processing

2 LAAPDs (7x14 mm²) read out simultaneously by one APFEL ASIC

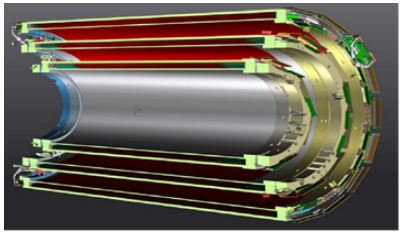
- Two channels with different gains for each LAAPD
- Dynamic range of 10,000 (1 MeV to 12 GeV)
- Programmable amplification of 16/32
- High rate capability (up to 500 kHz)
- Low power consumption: 55 mW/ch



Characterization and first field results of a new 64ch custom front-end ASIC for GEM readout

M. Alexeev[a,b], A. Bortone[a,b], R. Bugalho[c], J. Chai[b,d,f], W. Cheng[b,d,f], F. Cossio[d,b], M. D. Da Rocha Rolo[b], A. Di Francesco[e], M. Greco[a,b], C. Leng[b,d,f], H. Li[b,f], M. Maggiora[a,b], S. Marcello[a,b], M. Mignone[b], A. Rivetti[b], J. Varela[e], R. Wheadon[b]

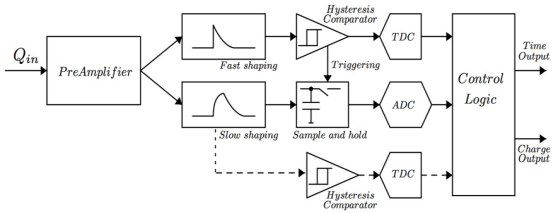
[a]Universita' di Torino, [b]INFN-Sezione di Torino, [c]PETSys Electronics (Lisbona), [d]Politecnico di Torino, [e]LIP (Lisbona), [f]Chinese Academy of Sciences



A new innovative lightweight tracker based on a Cylindrical Gas Electron Multiplier (CGEM) technology is being constructed for the upgrade of the inner tracker of the BESIII experiment at the BEPCII facility.
A custom readout electronics is being developed (TIGER, Torino Integrated Gem Electronics for Read-out) for the readout of this new detector.

Key features:

- to perform an analog charge measurement in parallel to the time stamp, all of this in a constrained power envelop that is due to the position within a superconductive solenoid.
- to achieve a 130um resolution within a 1T magnetic field using strips with 650µm pitch.



The core of the new front-end: **a custom designed 64ch ASIC** providing simultaneous time and charge measurement featuring a fully digital output and operated in triggerless mode.

Key design features:

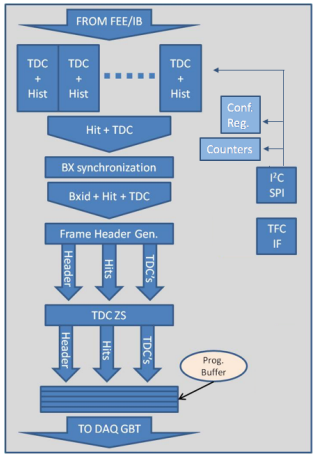
- a charge sensitive amplifier coupled to a dual-branch shaper stage, followed by a mixed-mode back-end that extracts and digitizes the timestamp and charge of the input signal. The TDCs are based on an analogue interpolation technique (time stamps with a time resolution better than 100 ps).
- energy measurement is possible using a time-over-threshold (ToT) method or a 10-bit digitization of the peak amplitude by a sample and hold circuit.

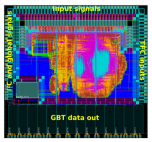
A new readout electronics for the LHCb Muon Detector Upgrade

Davide Brundu, on behalf of the LHCb Muon nSYNC/nODE Electronics Group*
Università degli Studi di Cagliari e INFN

nSYNC Architecture

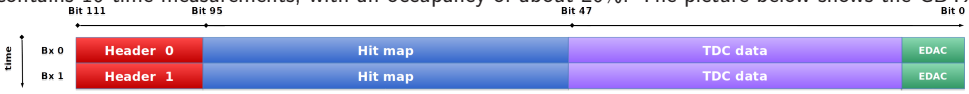
The nSYNC, an ASIC in UMC 130 nm technology, is the main component of the nODE board. It receives, through 48 input channels, the digital signals coming from the front-end electronics of the muon chambers.





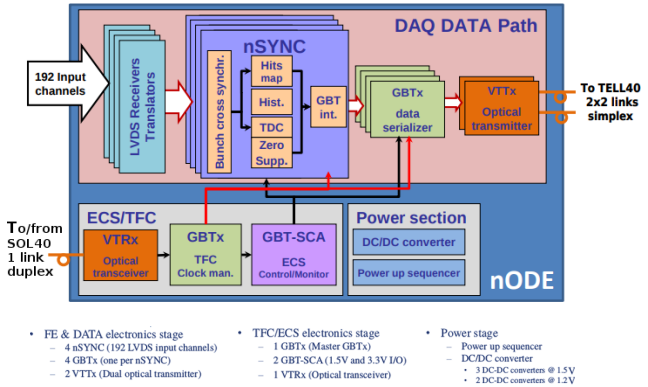
- The arrival time of the signals is measured by a fully digital TDC (one for each input), measuring the phase with respect to the LHC 40 MHz master clock. The TDC can work with several time resolutions, i.e. the number of slices on which the master clock can be divided, from 8 to 32 (16 nominal).
- The output data of each TDC channel consist of a binary flag (the Hit/NoHit information) and a 5 bits-wide word with the measured phase time (if any). This information is available every 25ns.
- These data go through a programmable-lenght pipeline in order to align hits from different channels related to the same bunch-crossing. This allows to uniquely associate the correct 12 bits-wide bunch-crossing identification number (BXid) to the all aligned data and pack these information together.
- The nSYNC creates then the extended frame, composed by Header + HitMap + TDCdata. The data are then Zero Suppressed (ZS)/truncated in order to fit the built frame into the GBTx frame, to be sent through the optical link. The HitMap, that represents the physical information and identifies the channel of the transmitted TDC measurement, is always sent non zero-suppressed, regardless the occupancy. The TDC data instead will be truncated if necessary.

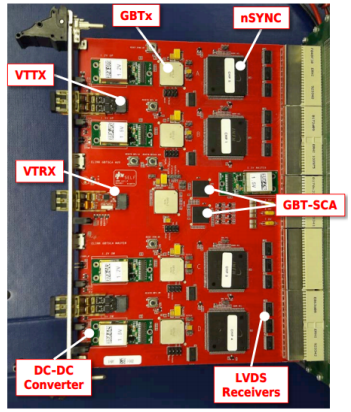
The last 8 bits of the frame are dedicated to the Hamming code, used to correct single-errors or detect double errors. This feature can be disabled to increase the TDC occupancy in the frame. At nominal resolution the frame contains 10 time measurements, with an occupancy of about 20%. The picture below shows the GBTx frame.



nODE Architecture

The main component of the new readout is the new Off-Detector Electronics Board (nODE) that will be equipped with 4 nSYNC chips.





- The nODE has 192 input channels that receive LVDS signals from the front-end electronics.
- Only optical interfaces - based on the **GBT** (GigaBit Transceiver) chipset and Versatile link components - are used to communicate with the data acquisition system, the Timing and Fast Control (**TFC**) framework and Experimental Control System (**ECS**).
- Each nSYNC communicates to its own GBTx chip, using an e-link data rate of 320 Mb/s, to transmit data to the DAQ system.
- An additional GBTx (the Master GBTx) is used to receive the master 40 MHz clock and the TFC commands (i.e. fast reset, synchronization signals ecc.) and to distribute them to the nSYNCs and to the other GBTx.
- Slow control and configuration of the board (i.e. configuration of GBTx and nSYNC chips, voltages monitoring ecc.) is managed by two GBT-SCA chips, that are interfaced with the Master GBTx, sharing the same TFC optical link to perform the slow communication, at 80 Mb/s.

Front-end ASICs for medical imaging

- **Selecting and Designing the Front-end Amplifier for High-gain Photomultiplier Detectors with Optimal Timing Performance** *1'* Speaker: Prof. Francesco Corsi (Politecnico di Bari)
- **Design and Preliminary Characterization Results of BASIC64, a New Mixed-Signal ASIC for SiPM Detectors** *1'* Speaker: Mr. Pietro Antonio Paolo Calò (Politecnico di Bari)
- **Operation of Microchannel Plate PMTs with TOFPET multichannel timing electronics** *1'* Speaker: Dr. Steven Leach (University of Leicester)
- **The MYTHEN-III strip detector prototypes** *1'* Speaker: Marie Andrä (Paul-Scherrer-Institut)

Selecting and Designing the Front-end Amplifier for High-gain Photomultiplier Detectors with Optimal Timing Performance

G. Matarrese, P.A.P. Calò, F. Corsi, C. Marzocca, S. Petrignani

DEI - Dipartimento di Ingegneria Elettrica e dell'Informazione - Politecnico di Bari, Bari, Italy

Summary

- It is shown that, when connecting an high-gain photodetector to an analog front end (AFE) for timing applications, a current buffer (CB) performs better than a Charge Sensitive Amplifier (CSA), which is affected by the normally large input capacitance of the detector;
- The parasitic inductance *L* of the interconnection plays a key role in setting the lower limit to the time resolution $\sigma_t = \frac{\sigma_{no}}{(dV_{OUT}/dt)_{V_{tr}}}$;
- In absence of *L*, the best σ_t is obtained for a front-end input resistance (R_{in}) as low as possible and a bandwidth (*BW*) as large as possible;
- Taking into account *L*, a new time constant, L/R_{in}, arises, which decouples the detector capacitance (C_{eq}) from the input transistor of the AFE, thus reducing the overall noise: $\sigma_t \approx \frac{C_{eq}}{Q_{eff}} \frac{2L}{R_{in}} e_n \sqrt{BW}$;
- Taking into account *L*, the CB outperforms also the time resolution achievable by a VA;
- A companion poster, from the same authors, shows the results of an AFE (BASIC64) which uses a CB as input stage for best time resolution.

Experimental Test and Characterization of "BASIC64", a New Mixed-Signal Front-End ASIC for SiPM Detectors

M. G. Bisogni[1], P. A. P. Calò[2*], F. Ciciriello[2], F. Corsi[2], C. Marzocca[2], G. Matarrese[2], S. Petrignani[2]

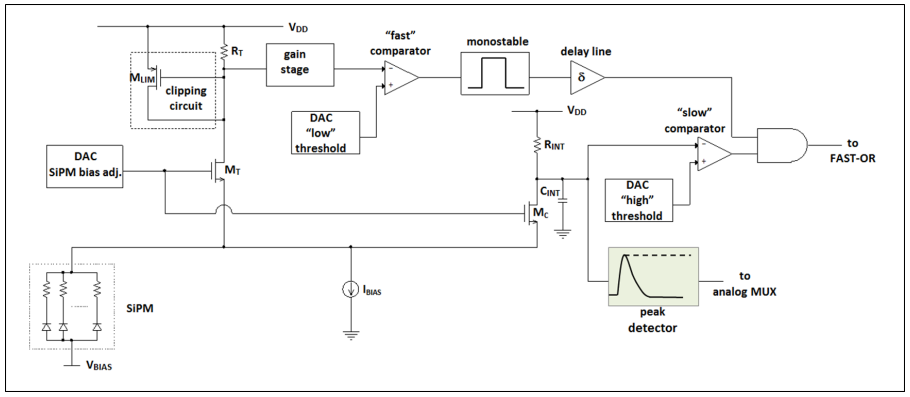
[1] INFN – Sezione di Pisa, Italy
[2] DEI – Politecnico di Bari, Bari, Italy
* Presenting author

We present a CMOS current-mode read-out ASIC for Silicon Photomultipliers, designed for time and energy measurements in PET application systems.

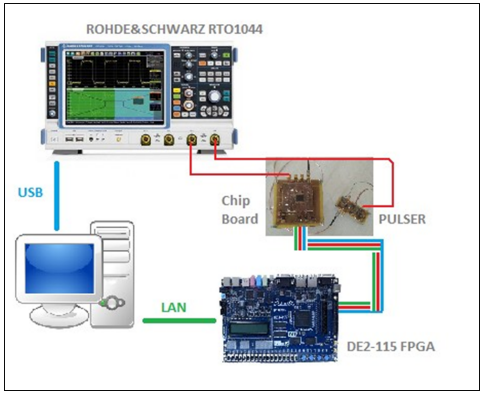
The $100\ nH$ parasitic inductance between SiPM and electronics has resulted in the choice of a preamplifier with relaxed constraints for R_{in} and BW as one viable solution to the issue of reduced output signal slope.

BASIC64 features:

- *Analog channel suitable for both n-on-p and p-on-n SiPMs*
- *SiPM bias voltage adjustable (8 bit DAC)*
- *Trigger disabled for signals under a selectable charge threshold*
- *Internal 10 bit ADC for charge measurements*



Architecture of the analog channel



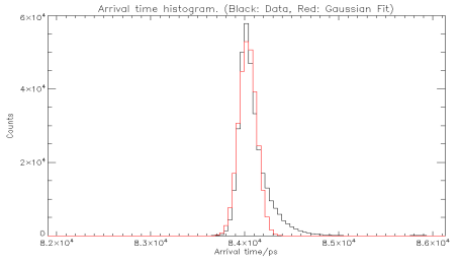
Measurements setup

MEASUREMENTS RESULTS	
PARAMETER	**VALUE**
Timing jitter rms	40 ps
Gain	$3\ mV/pC$
Maximum Input Charge	$5800\ pC$
Non-Linearity Error	1.5 %

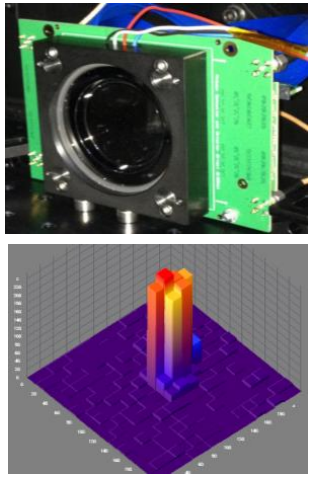
Operation of Microchannel Plate PMTs with TOFPET multichannel timing electronics

Steven Leach, Jon Lapington, University of Leicester, UK
James Milnes, Tom Conneely, Photek Ltd., UK
Ricardo Bugalho, Stephan Tavernier, PETsys Electronics SA, Portugal

- We describe an experimental programme to evaluate the TOFPET ASIC timing electronics
  - Multichannel TOFPET ASIC is developed by PETsys SA
  - Timing performance is evaluated using microchannel plate PMTs in single photon counting mode.
- We present time resolution measurements using:
  - The on-board electronic stim signal,
  - A Photek PMT210 high speed single anode MCP photomultiplier detector
  - A multi-anode MCP detector using a pixelated multi-layer ceramic readout.



Time resolution of 96 ps rms using an MCP-PMT



Multi-anode MCP detector (top) and image of pulsed laser (bottom)

The MYTHEN III strip detector prototypes

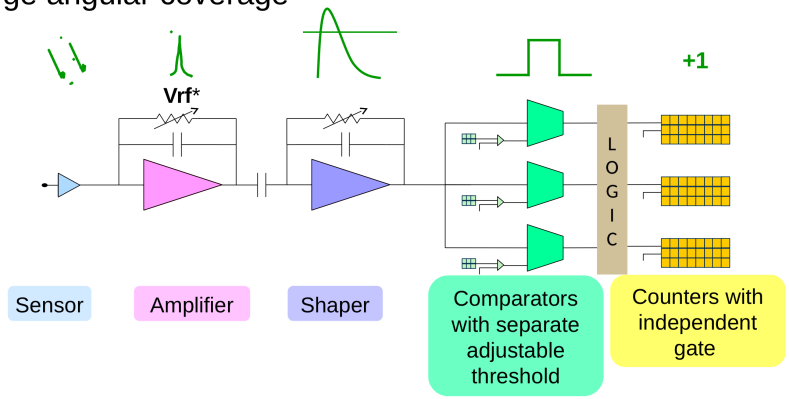
Marie Andrä
SLS Detectors Group
Paul Scherrer Institut
Switzerland

The new Mythen III chip

What is MYTHEN?
- silicon microstrip detector with 50 µm pitch, 8 mm long strips
- single photon counting
- for time-resolved powder diffraction, medical imaging, etc

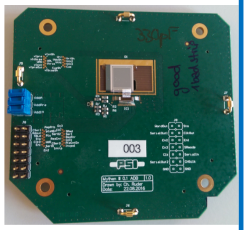
Why a strip detector?
- less channels per area: fast frame rates
- small pitches possible: high resolution
- large angular coverage

Why photon counting?
- ideally noiseless
- large dynamic range
- fluorescence suppression



*Vrf changes the feedback resistance, i.e. the gain and shaping time

What is new?
- three comparators and three 24-bit-counters for:
  - energy-windowing
  - count rate improvement (track pile-up)
  - pump-probing with multiple time slots, counters are independently gateable
- reduced threshold dispersion
- improved noise performance
- small dead time → increased count rate capability



- Microstrip single photon counting detector
- New prototype readout chips:
  - Three comparators and gateable counters
  - Improved noise performance (< 200e^-)
  - Small threshold dispersion (< 10e^- after trimming)
  - Increased count rate capability (< 40ns in fast mode)
  - ~ 100kHz readout

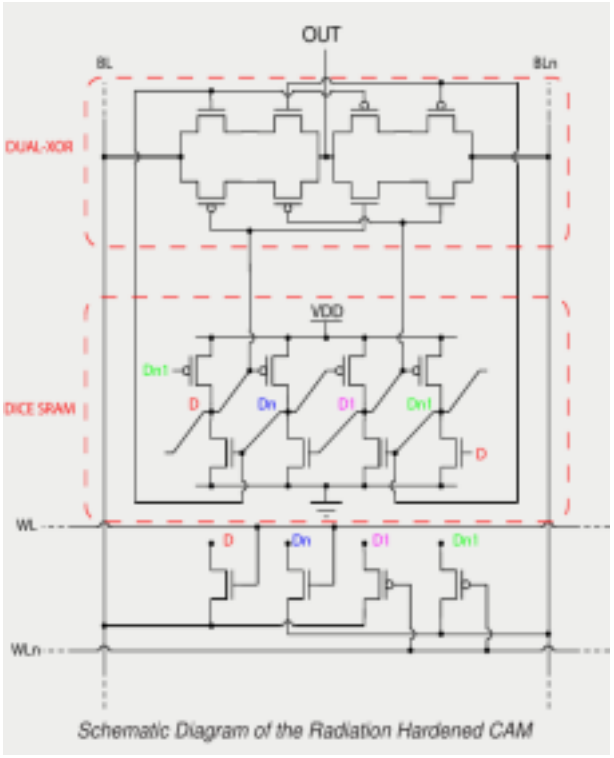
Advanced technologies: 28 nm CMOS, silicon photonics

- **An innovative radiation hardened Content-Addressable Memory** *1'* Speaker: Seyedruhollah Shojaii (MI)
- **Design of a high radiation-hard driver for Mach-Zehnder Modulators based high-speed links for hadron collider applications** *1'* Speaker: Fabrizio Palla (PI)

A Novel Radiation Hardened CAM

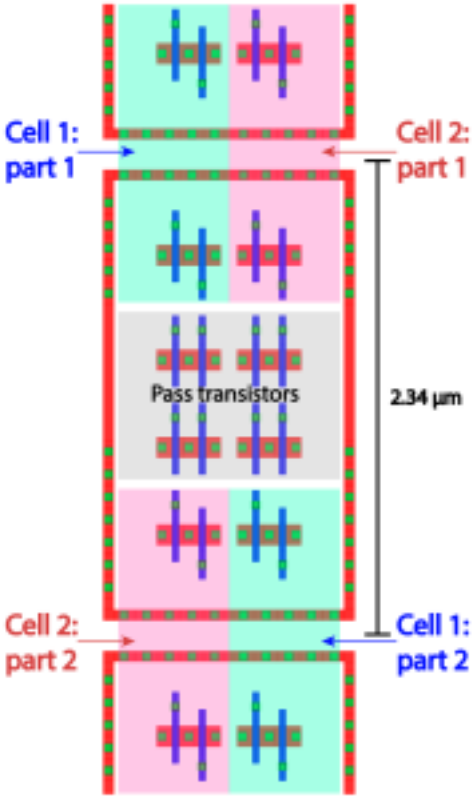
O. Anagnostou[1], V. Liberali[2], M. Mews[1], **S. Shojaii[1]**

1) The University of Melbourne
2) INFN and university of Milan



Schematic Diagram of the Radiation Hardened CAM

- This poster describes an innovative Content Addressable Memory cell with radiation hardened (RH-CAM) architecture.
- An array of proposed architecture can perform on-time pattern recognition tasks in harsh environments, such as front-end electronics in hadron colliders and in space applications.
- The RH-CAM is designed in a commercial 28 nm CMOS technology.
- The circuit has been simulated in worst-case conditions, and the effects due to single particles are analyzed by injecting a fault current into a circuit node.



RH-CAM layout in 28 nm CMOS technology
(two interleaved cells)

Design of a high radiation-hard driver for Mach-Zehnder Modulators based high-speed links for hadron collider applications

G. Ciarpi[1], G. Magazzù[2], F. Palla[2], S. Saponara[1]

1. University of Pisa 2. INFN – Sezione di Pisa

On behalf of the PHOS4BRAIN Collaboration

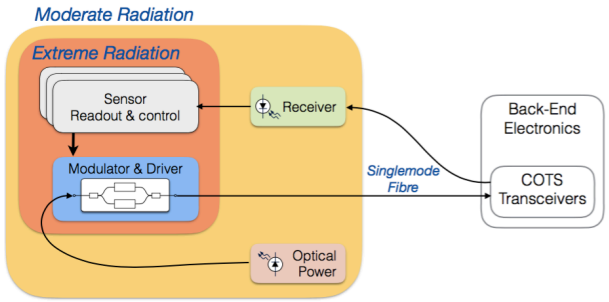
Contact: Fabrizio.Palla@pi.infn.it

Develop a driver circuit in 65 nm CMOS technology to pilot a Silicon Mach-Zehnder Modulator for data transmissions up to 10 Gbps to work at 5-10 MGy Total Ionization Doses and fluences up ~few 10^{16} n_{eq}/cm^2. Use for inner layers of LHC or at FCC experiments.

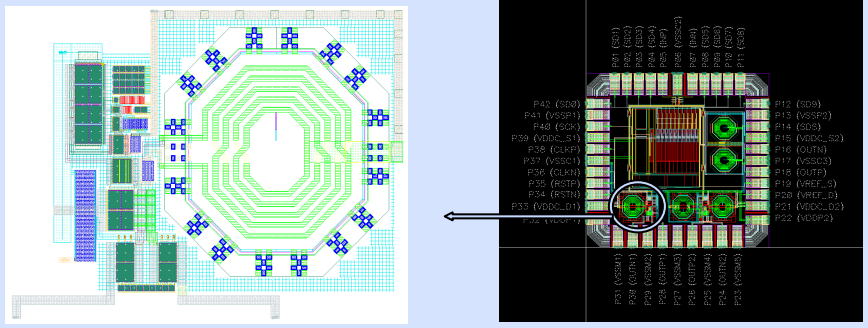
MZM voltage swing of 2 V pp, necessitates a cascode architecture for the driver.

Driver power ~170 mW for 5 MGy and 10 Gbps (from simulation model).

The chip has been submitted in May.



LAYOUT



Area 200 x 180 µm²

Simulated 10 Gbps eye diagrams for a driver with MZM load
Typical (red)
5 MGy (blue)