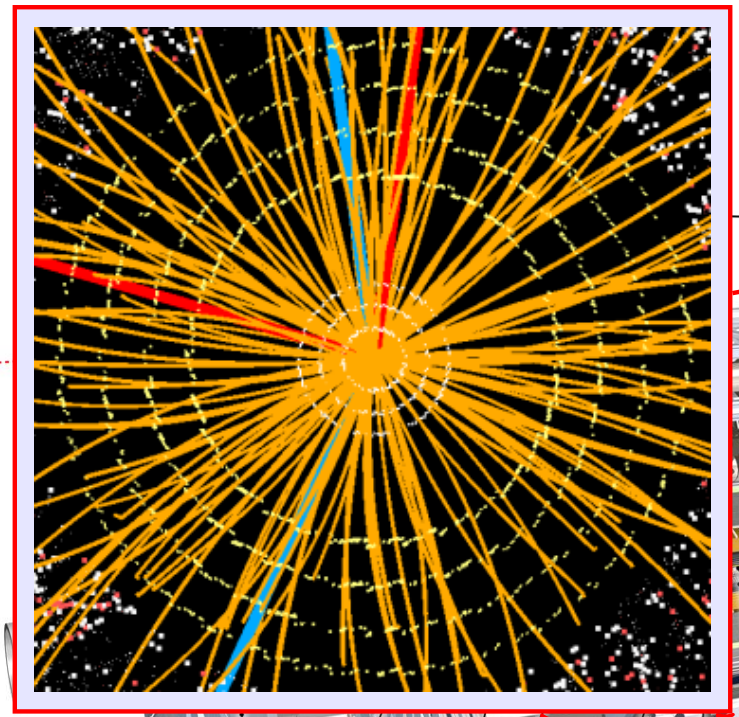
AM07: Characterization of the Novel Associative Memory Chip Prototype Designed in 28 nm CMOS Technology for High Energy Physics and Interdisciplinary Applications

Alberto Stabile, Calliope-louisa Sotiropoulou, Alberto Annovi, Giovanni Calderini, Stefano Capra, Bruno Checcucci, **Francesco Crescioli**, Francesco De Canio, Giacomo Fedi, Luca Frontini, Christos Gentsos, Valentino Liberali, Fabrizio Palla, Jafar Shojaii, Takashi Kubota, Gianluca Traversi, Sebastian Viret

14th Pisa Meeting on Advanced Detectors
1-6-2018

Tracking



Hardware Tracking

Data from the silicon detector
is analyzed in real-time.
The **Associative Memory**
is a powerful computing tool
to do real-time pattern recognition

hits

tracks

phi	η	z	p_T	d
1.2	0.2	1.3	10.5	0.03
0.7	1.1	1.1	4.3	0.14
-1.6	-1.8	1.2	6.6	0.32
-2.2	-0.5	1.3	12.2	0.28
0.9	0.9	1.2	1.9	0.83

25m

Pixel detector

Toroid magnets

LAr electromagnetic calorimeters

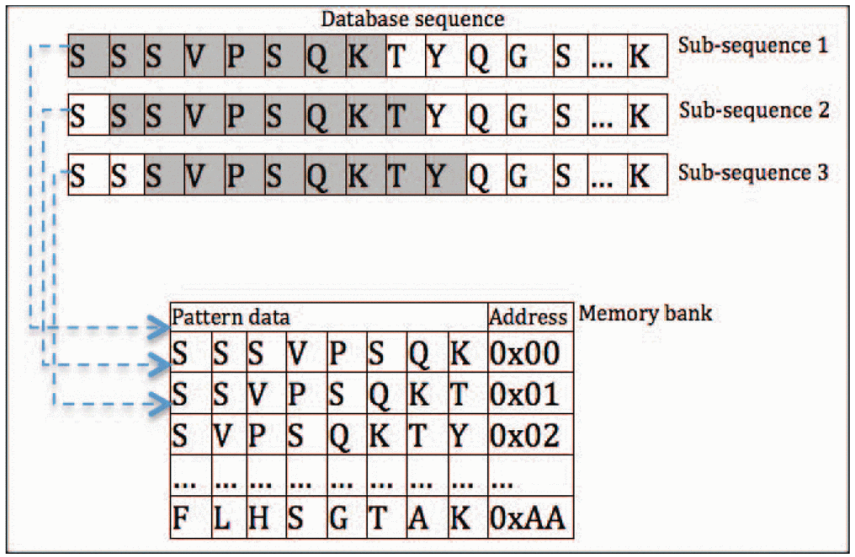
Muon chambers

Solenoid magnet

Transition radiation tracker

Semiconductor tracker

Outside HEP: two examples

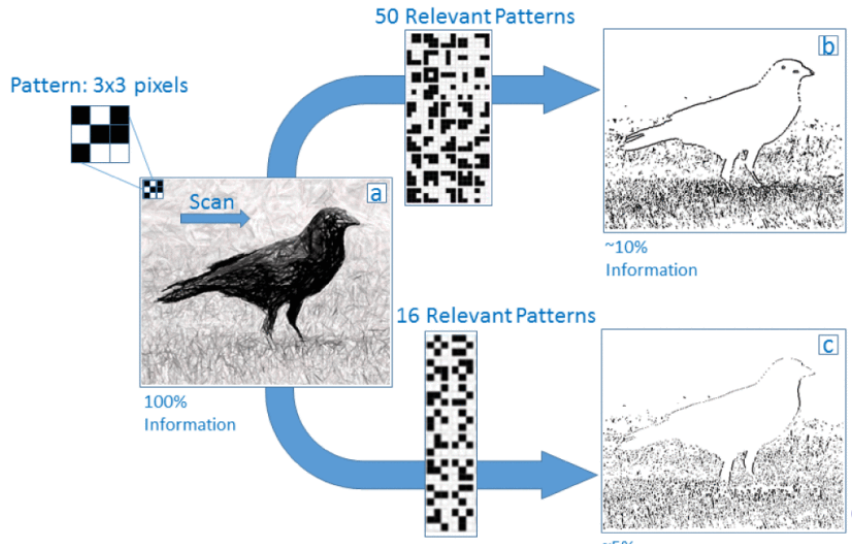


AM-based approach to image processing in medical applications inspired by brain emulation.

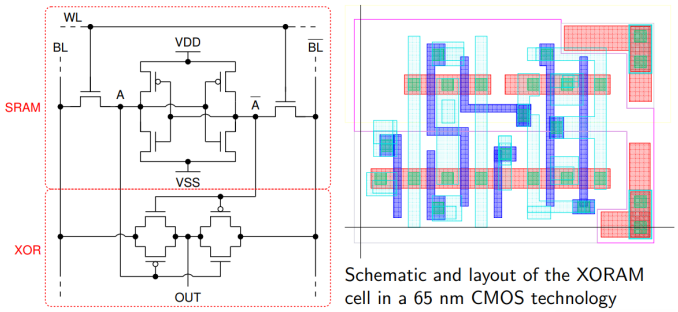
P. Luciano et al., "A Hardware Implementation of a Brain Inspired Filter for Image Processing," in IEEE Transactions on Nuclear Science, vol. 64, no. 6, pp. 1374-1381, June 2017.
doi: 10.1109/TNS.2017.2706061

Fast DNA sequence alignment or feature extractor.

M. A. Mirzaei et al., "A Novel Associative Memory Based Architecture for Sequence Alignment," 2016 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), Chicago, IL, 2016, pp. 473-478.
doi: 10.1109/IPDPSW.2016.21



AMchip06



Schematic and layout of the XORAM cell in a 65 nm CMOS technology

Produced 25 wafers (8000 chips)

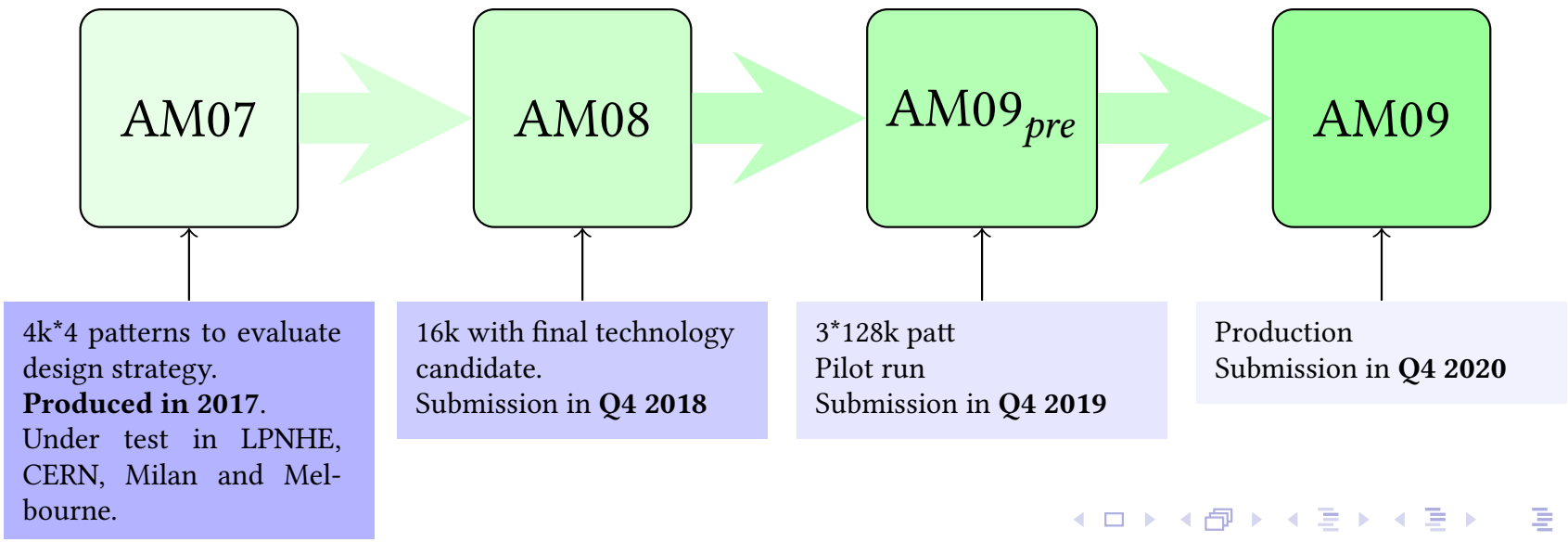
+25 wafers in 2018

- Digital ASIC
  - **65 nm TSMC**
  - 100 MHz
  - 168 mm^2
  - 128k 8x16 bit patterns
    - 2 ternary bits + 14 binary bits
  - Flip-chip BGA
  - MGT I/O at 2/2.4 Gbps
- Full-custom CAM cell
  - XORAM technology
    - doi:10.1109/ICECS.2012.6463629
  - Optimized for low power
- Power consumption during operations avg 3 W

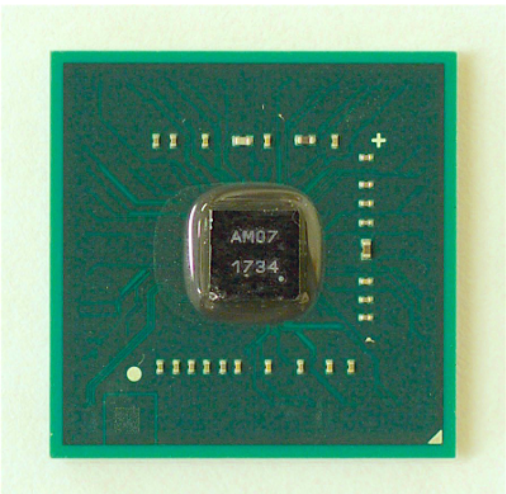
Power consumption figure of merit:
2.3 fJ/bit/comparison @ 1.15 V 1.8 fJ/bit/comparison @ 1.0 V

Goals for the ATLAS/CMS Phase-II chip

- 384k patterns in $\simeq 150$ mm^2
  - 16 bit * 8 busses
  - 2 ternary bits + 14 binary bits
- 250 MHz comparison clock
- LVDS DDR IOs @ 500 MHz to reduce pinout, but to avoid MGT complexity
- At least 1 fJ/bit/comparison
- **28 nm**



AM07

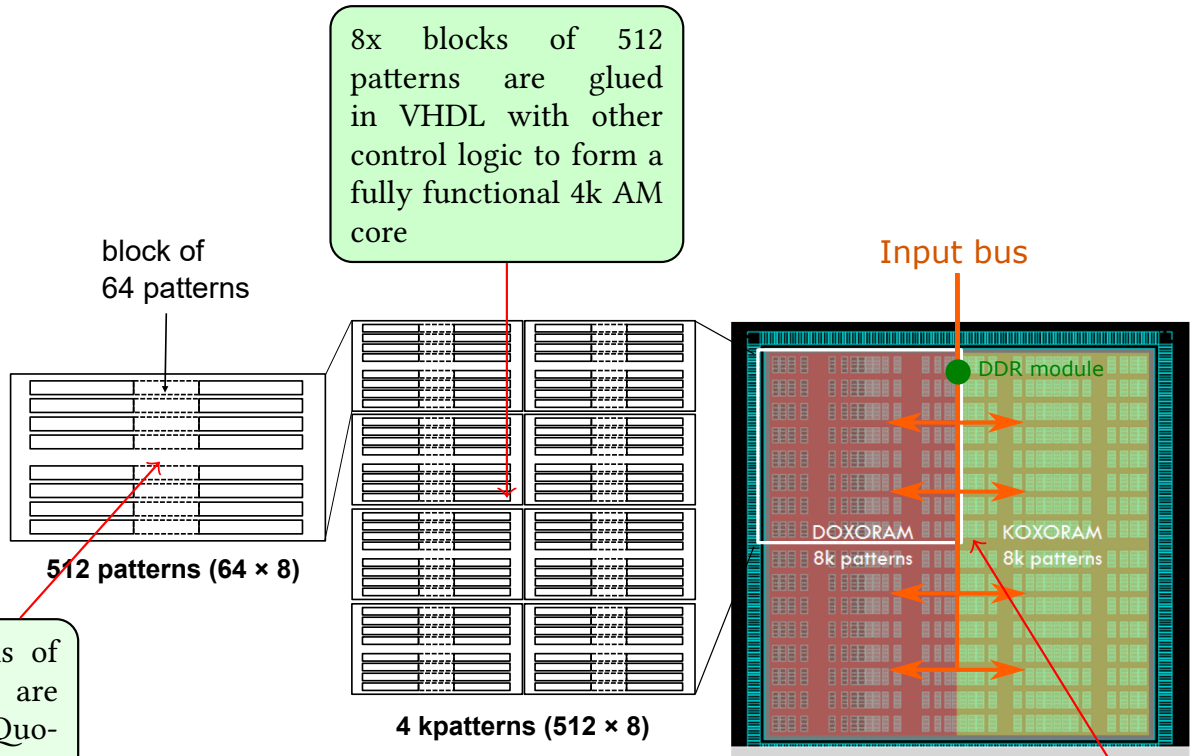


17 × 17 BGA

- 10 mm^2 28 nm
- $4 \times 4k$ patterns organized in independent cores
  - 2x DOXORAM, 2x KOXORAM
  - Both are evolutions of the XORAM of AM06. Patent pending in Italy.
- 1 bus using 9x LVDS pairs in DDR mode (18 bit)
- 7 busses using 18 bit LVCMOS
- 4 outputs LVCMOS (12 bit address + 8 bit hitmap)
- Designed to run internally at 200 MHz
- RX/TX LVDS test drivers

Financed by ANR FTK (LPNHE/IPNL) and INFN IMPART and RD_PHASE2 (ATLAS/CMS) projects

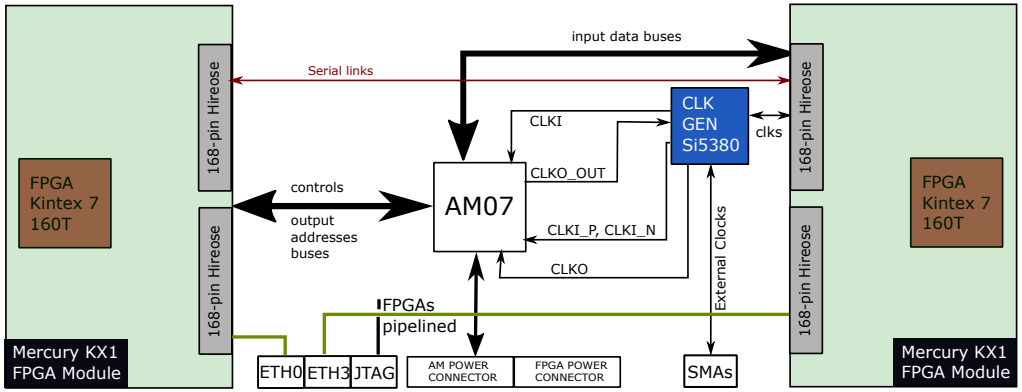
AM07 Internal structure



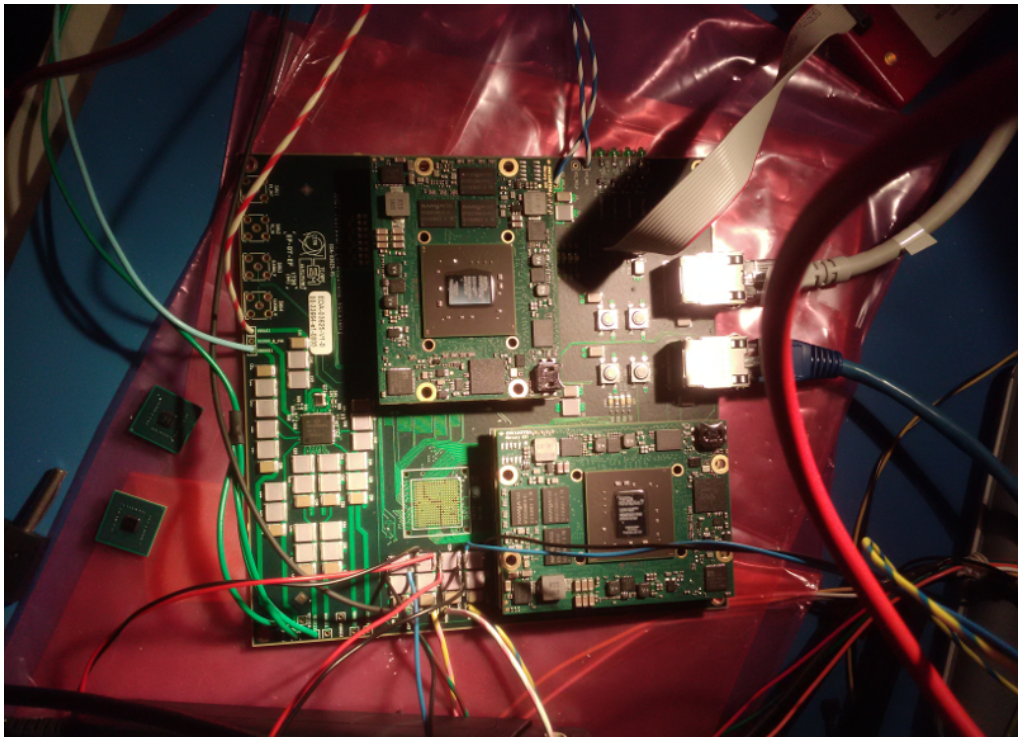
AM07 Design flow

- Full-custom blocks (CAM, LVDS) designed with Cadence Virtuoso
- Standard cell logic synthesized from VHDL using Cadence Genus.
- Top level integration and P&R using Cadence Innovus
- Static timing analysis using Cadence Tempus
- IR drop analysis using Cadence Voltus
- Functional simulation in UVM using Cadence Incisiv

AM07 Test Board



To test the AM07 we need two FPGAs on the test board to drive all the LVCMOS and LVDS signals.

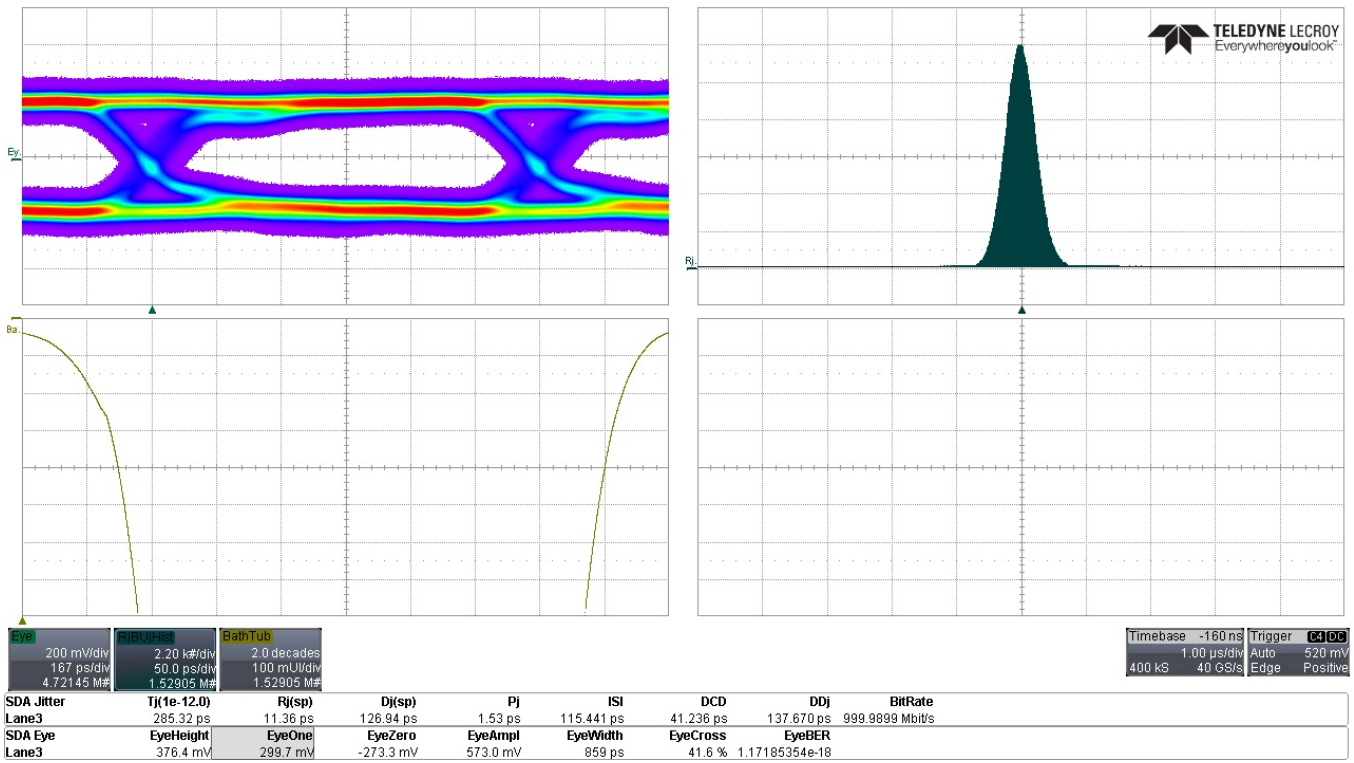


2x Xilinx Kintex 160t
Si5380 low jitter clock manager (LTE freq optimized, not all freq available)
Firmware based on IPBus + python scripts

Functional Tests

- AM07 has an internal feature to scan the pattern bank and produce an unique CRC value
  - Scan is successful up to 245 MHz (chip was designed for 200 MHz)
- LVDS RX/TX tested up to 1.1 gbps
- In the FPGA we can tune all clk relative phases and individual delays for each IO to deskew the busses
  - Zero errors up to 150 MHz using all busses, CLK via LVCMOS
  - Zero errors up to 180 MHz using LVDS bus and CLK via LVDS
- Tests still ongoing, improvements can be acheived on test FPGA fw

LVDS



LVDS TX/RX eye and BER at 1 Gbps

BIST

- The Built-In Self Test is made by two nested loops
  - Outer loop: write 18 pattern banks made by patterns with the form $1 << ((bus + addr + offset) \mod 18)$ changing offset from 0 to 17
  - Inner loop: test with threshold 1 fixed input with the form $1 << offset$ changing offset from 0 to 17
- The CRC-32 of the output sequence is computed and compared to the expected value
- If one bit of memory is not working (write or match operation) as expected the CRC-32 value will be different

BIST Max core frequency

fail	fail	105	184	245	245	245
0.65	**0.75**	**0.85**	**0.95**	**1.00**	**1.05**	**1.10**

Core supply [V]

Power consumption

There are several components of the total power consumption.

Component	Current at 1.0 V (mA)
Leakage	2.94
Clock distribution 105.32 MHz	9.35
Clock distribution 147.46 MHz	10.60
Clock distribution 184.32 MHz	15.4
Hit distribution up to cores at 184.32 MHz	83.1

Power consumption

Matching power consumption is measured with an average bit flip between subsequent hits of 50%.
It is reported as fJ/bit/comp to be able to compare and scale to larger chips.

Tech.	Meas (fJ/bit/comp)	Sim (fJ/bit/comp)
KOXORAM	0.748	0.69
DOXORAM	0.851	0.91

With respect to XORAM cell we gain a factor 2.9 in density with a factor 1.7 less in power consumption.
The next version of KOXORAM will consume 0.42 fJ/bit/comp

More information

Recently published articles about AM07:

- "Characterization of an Associative Memory Chip in 28 nm CMOS Technology" https://doi.org/10.1109/ISCAS.2018.8351801
- "Design and Characterization of New Content Addressable Memory Cells" https://doi.org/10.1109/ISCAS.2018.8351682
- "Characterization of an LVDS Link in 28 nm CMOS for Multi-Purpose Pattern Recognition" https://doi.org/10.1109/ISCAS.2018.8351576

AM08

The purpose of this small area prototype (10 mm^2) is to finalize all the features and interfaces that will be used by the final chip (AM09).

- AM08 submission foreseen in the fall 2018
- New features:
  - All LVDS DDR IOs @ 500 MHz
  - Configuration via SPI (slow) or control words encoded in the input data stream (fast)
  - 250 MHz core freq
  - Internal DPLL
    - To generate 8x 250 MHz clocks 45° apart to be used in different cores and spread the power consumption over the clk period
    - "A Digitally-Controlled Ring Oscillator in 28 nm CMOS technology" https://doi.org/10.1109/ISCAS.2018.8351836
  - Temperature sensor
    - "Temperature Sensor with Process and Mismatch Auto-Compensation Technique in 28 nm CMOS" https://doi.org/10.1109/ISCAS.2018.8351851

Conclusions

- The Associative Memory is a device designed for real-time pattern recognition in high performance computing applications
  - It has been used in tracking hardware processor at hadron collider experiments (CDF SVT, ATLAS FTK) and it will be used in future HL LHC experiments upgrades (ATLAS HTT)
  - To meet new requirements we pursued the development of the AM in 28 nm
- AM07, the first fully functional prototype in 28 nm, has been produced in 2017 and it's under test
  - Functionality has been verified (at least up to 150 MHz, internally up to 245 MHz)
  - Power consumption is compatible with the simulation expectations and in track with our roadmap to the final chip
- AM08 is under design, it will be submitted in fall 2018
  - Features & interface of the final chip