Upgrade of the ATLAS Muon System for the HL-LHC

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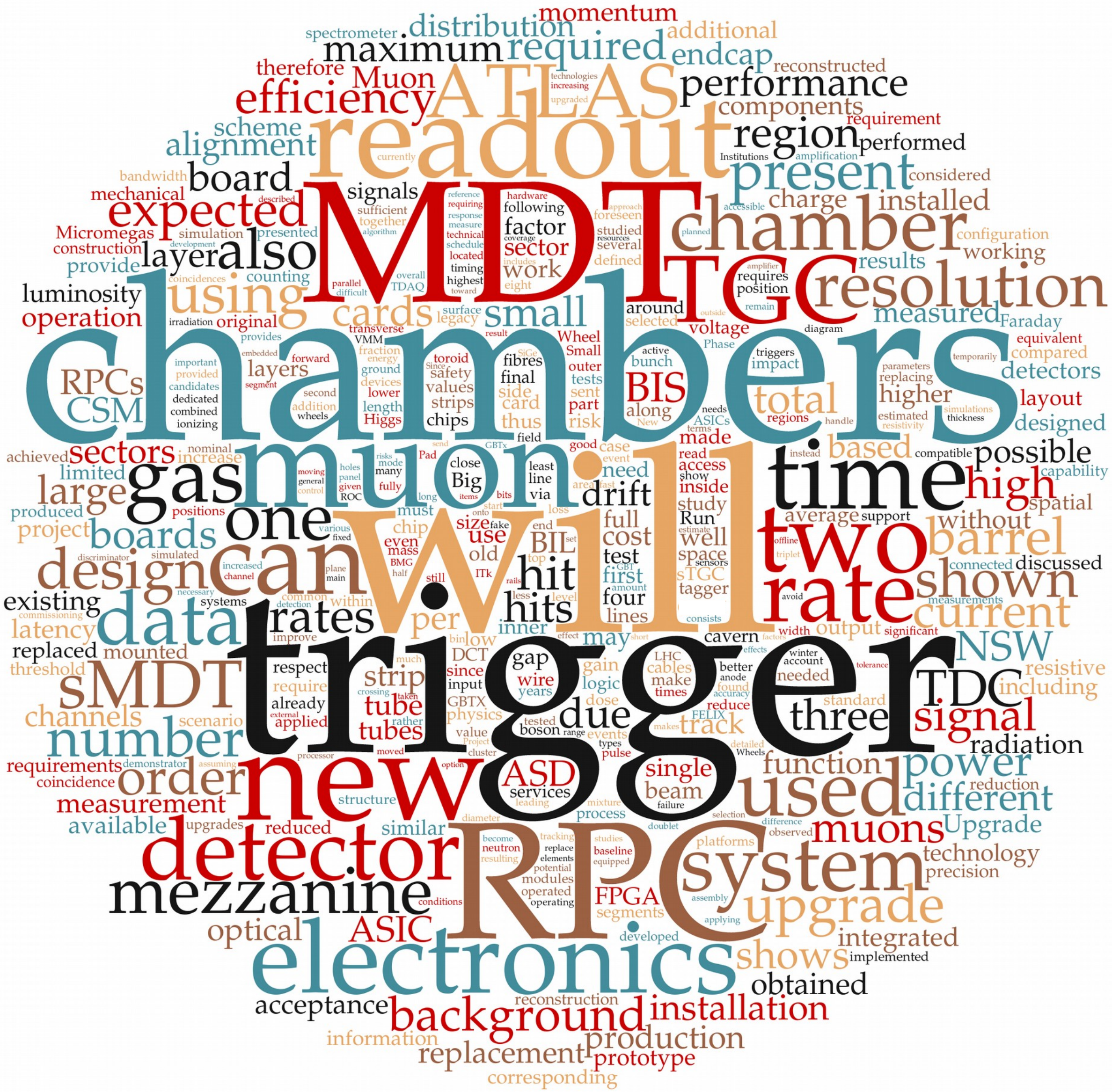
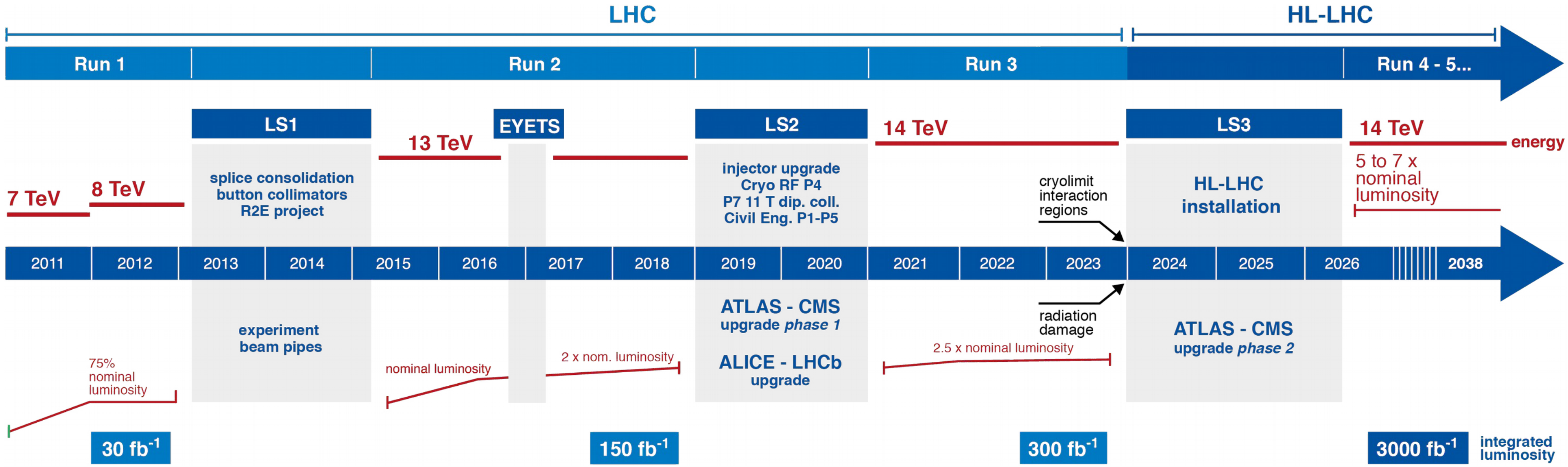
for the ATLAS EXPERIMENT



14th Pisa Meeting on Advanced Detectors, May 28–June 1, 2018

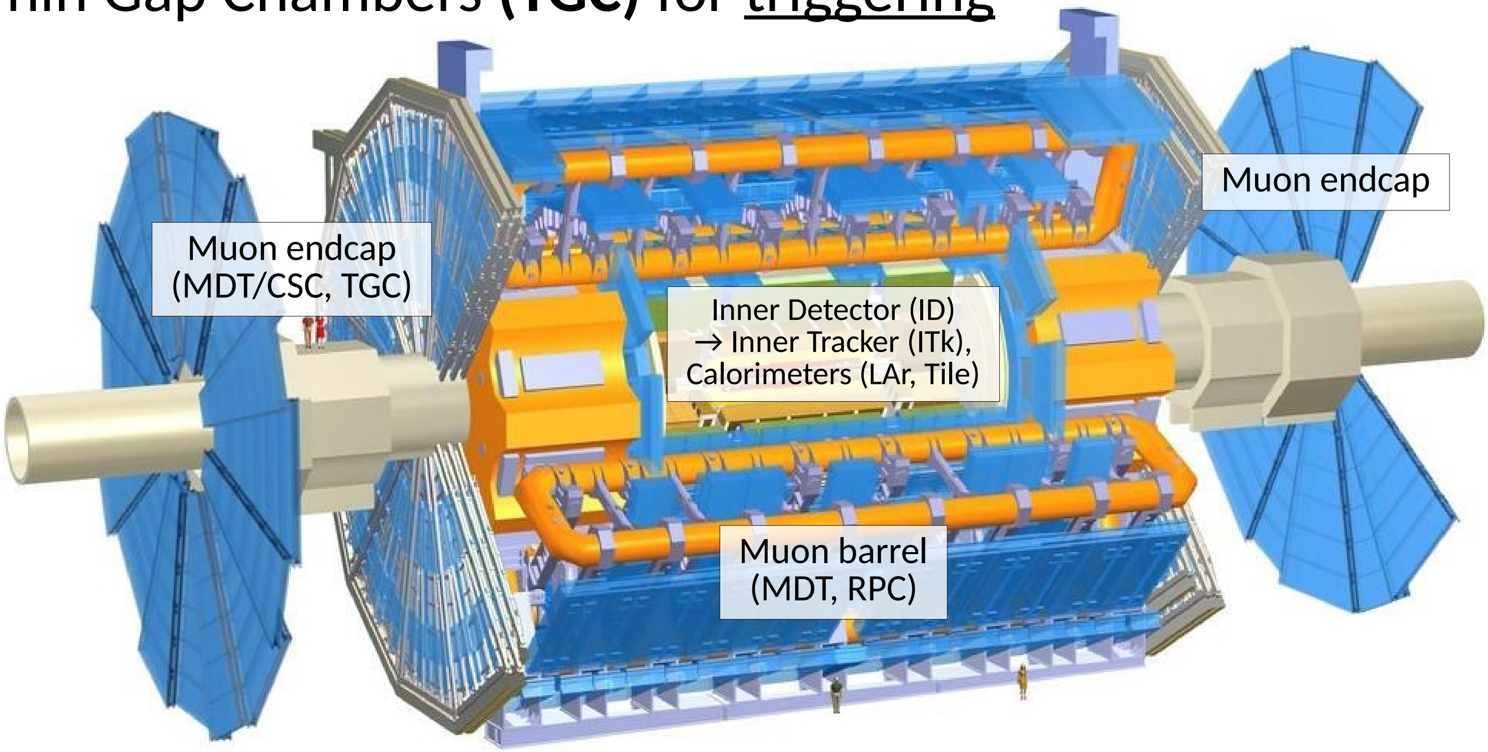
High-Luminosity LHC

- **HL-LHC** upgrade of the LHC: increase **instantaneous luminosity** to 5×10^{34} cm^{-2} s^{-1} (ultimate: 7.5×10^{34} cm^{-2} s^{-1}), total **integrated luminosity** of 3000 fb^{-1} (ultimate: 4000 fb^{-1})
- **ATLAS Phase-I upgrade** in Long Shutdown 2 (LS2, 2 years duration, planned for 2019/20), followed by LHC Run 3
- **ATLAS Phase-II upgrade** in LS3 (2.5 years, presently scheduled for 2024-26), followed by (HL-) LHC Runs 4,5,6,...

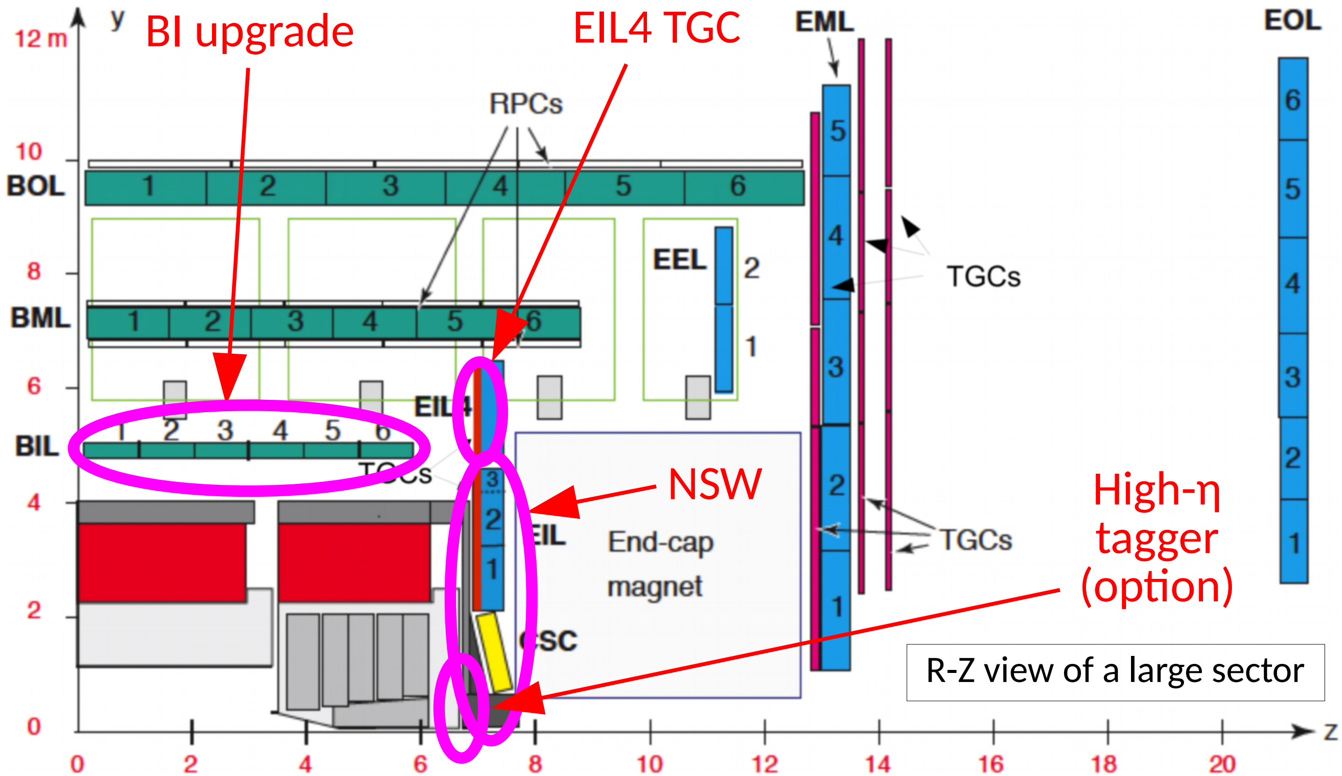


ATLAS Muon System

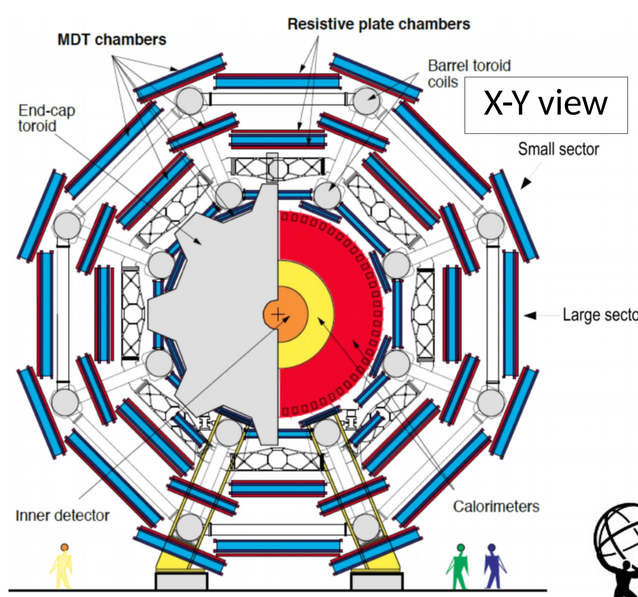
- **ATLAS muon spectrometer: muon chambers** (blue) embedded in air-core **toroid magnets** (orange)
  - Monitored Drift Tube **(MDT)** chambers and Cathode Strip Chambers **(CSC)** for precision tracking
  - Resistive Plate Chambers **(RPC)** and Thin Gap Chambers **(TGC)** for triggering



Muon Spectrometer



- **Muon spectrometer trivia:**
  - **B**=Barrel (|η|<1.0), **E**=Endcap (1.0<|η|<2.7)
  - **I**=Inner, **M**=Middle, **O**=Outer, **E**=Extra
  - **1..6** position in Z/R
  - Most tracks traverse **BI/BM/BO** or **EI/EM/EO**



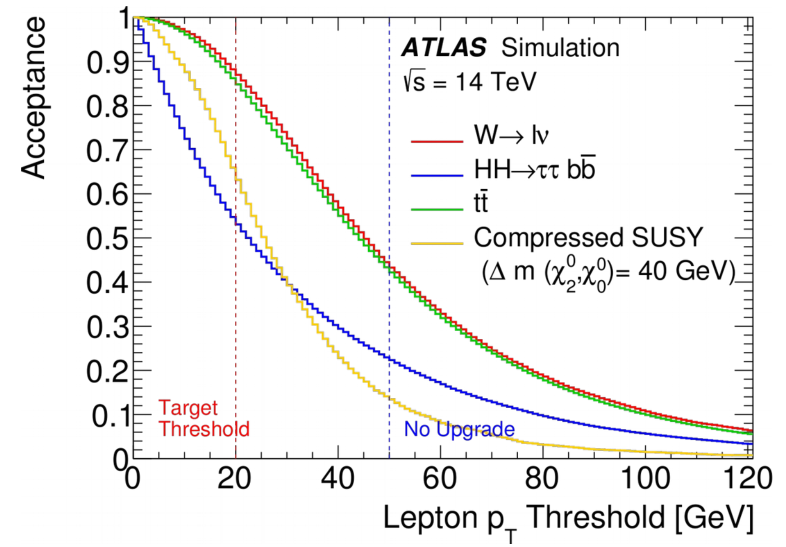
- **8 Large (L) sectors** in-between barrel toroid coils (14°)
- **8 Small (S) sectors** overlapping with toroid coils (8.5°)
- Most tracks traverse either **only L** or **only S** chambers
- Toroid magnets (0.5 T) **bend tracks in η** (ID solenoid: in φ), $\Delta p_T/p_T$ = 4% over large range in p_T, increasing to 11% at 1 TeV

ATLAS Phase-II Upgrade

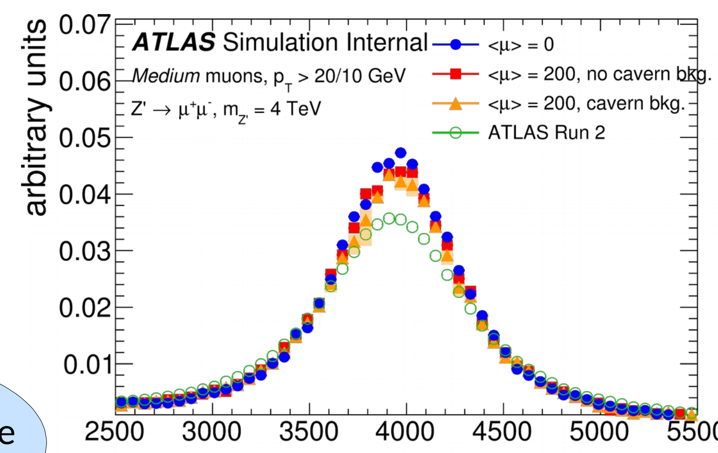
- No upgrade → **lepton trigger thresholds** would have to be increased to ~50 GeV → **unacceptable** impact on physics
- Need **more selective <u>trigger algorithms</u>**
- Need **higher** sustainable **<u>trigger rates</u>**
- <u>Detectors</u> **can cope** with pile-up as high as <μ>=200 (including cavern background) **without major problems**
- **Phase-II trigger upgrade**:
  - L0 trigger at **1 MHz**, **10 μs** latency (present: L1 at **100 kHz**, **2.5 μs** latency)
  - High-Level Trigger (HLT) PC farm, max output rate **10 kHz** (present: **1.5 kHz**)

First trigger level: renamed L1→L0

Option to evolve to an L0/L1 scheme max 4 MHz/800 kHz 10/35 μs



Trigger acceptance for various physics channels as a function of lepton trigger pT threshold



Z' mass peak

Muon System Upgrade

- **Chambers:**
  - BI upgrade: add BIL+BIS **RPC** chambers, replace BIS **MDT** by **sMDT** chambers
  - **New Small Wheels** (NSW): replace CSC and MDT in EI region by **Micromegas and sTGC** chambers
  - EIL4 **TGC** chambers: replace **TGC doublets** by **triplets**
  - Option: **High-η tagger** to identify muons at $2.7<|\eta|<4.0$
- **Electronics:**
  - Replace the **entire MDT** electronics chain
  - Replace **most of** the **RPC/TGC** electronics chain

Address weaknesses of the present detector, increase robustness in a more challenging environment

NSW is a Phase-I upgrade

Skip in this talk

Skip, not yet approved

Enable more sophisticated trigger algorithms, ensure compatibility with new trigger/DAQ scheme

Rate Limitations

- <u>No general rate or longevity issues</u> for ATLAS **MDT** and **TGC**
- **Present** ATLAS **RPC**: GIF++ tests indicate there is a current limit, equivalent to a **maximum long-term sustainable rate** ("safe operating mode") of <u>100 Hz/cm</u>^{2} at nominal HV
- **Expected rates** at HL-LHC: up to <u>300 Hz/cm</u>^{2}
- **Solution**: reduce gas gain (HV) in regions with high rates in order to reduce currents
- **Price**: reduced hit efficiency, worst case: 65% around $|\eta|=1$

RPC rates (Hz/cm^2) at HL-LHC vs η and φ (incl. safety factor 2)

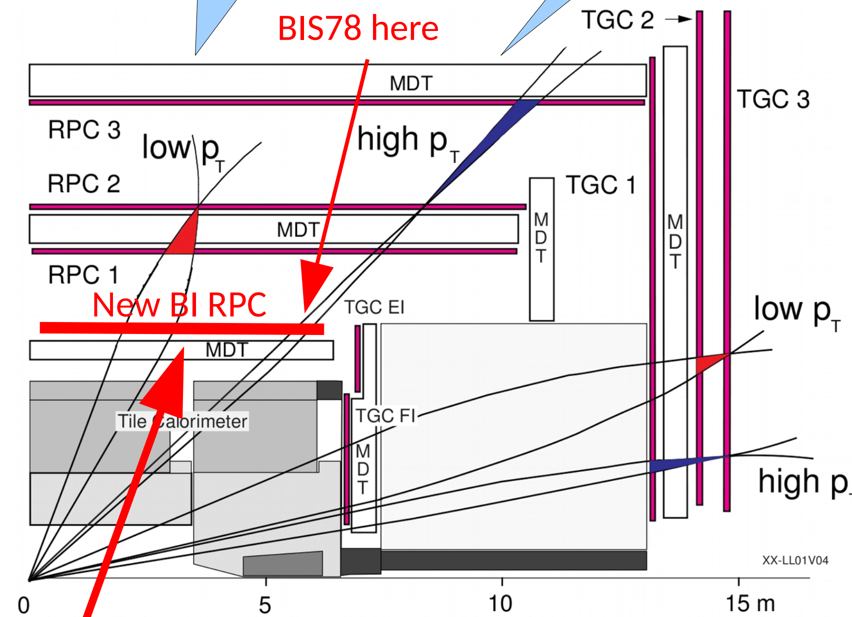
Sector	RPC unit Id. along Z direction																				Average
Φ Id.	-6.2	-6.1	-5.0	-4.0	-3.2	-3.1	-2.2	-2.1	-1.2	-1.1	1.1	1.2	2.1	2.2	3.1	3.2	4.0	5.0	6.1	6.2	
01.01	342	280	301	225	145	114	128	101		61	61	71	113	122	127	136	214	276	269	285	180
01.02	293	281	303	218	159	133	129	143		76	71	75	127	143	140	148	215	295	278	297	188
2	168	204	188	138	109	90	77	63	55	56	45	48	61	79	94	104	140	207	196	152	115
03.01	297	296	281	198	148	128	119	119	68	67	65	71	131	125	114	125	207	329	268	290	177
03.02	300	243	277	210	151	129	155	122	85	75	75	70	122	127	152	132	207	315	243	299	179
4	112	166	158	151	101	83	65	77	41	53	46	41	73	68	92	108	160	196	175	112	101
05.01	171	173	263	138	105	102	140	127	68	60	60	69	124	177	102	137	185	290	173	171	149
05.02	227	198	237	158	109	105	136	143	77	61	63	71	111	136	108	141	200	267	255	282	159
6	175	186	208	163	105	95	90	95	77	59	52	59	84	81	106	124	189	200	227	167	131
07.01	305	263	288	191	154	129	131	114		76	78		122	139	124	148	185	261	268	305	183
07.02	327	258	216	203	141	112	129	108		74	77		105	114	112	152	184	278	276	279	175
8	146	196	195	161	103	85	80	70	50	57	54	54	67	74	85	108	168	196	194	156	118
09.01	319	246	301	206	155	117	149	119		46	64		106	134	124	135	197	283	262	297	181
09.02	347	258	287	205	143	95	107	103		58	67		99	112	95	137	188	285	265	292	174
10	174	201	207	147	99	86	68	71	46	43	41	50	64	69	80	103	148	193	201	170	115
11.01	308	244	237	157	97	84	81	87		40	43		83	94	92	94	148	227	215	278	132
11.02	196	193	157	105	78	66	55	57		33	31		50	62	58	71	98	151	160	185	98
12						80	81	66	51	36	36	51	75	87	80						64
13.01	291	278	253		140	102	96	84	43	41	47	50	87	95	99	123		249	263	319	149
13.02	299	264	262		104	97	105	86	49	48	50	56	93	103	97	110		252	227	294	146
14						142	68	64	52	41	40	49	63	68	136						76
15.01	196	221	148	113	76	71	67	49		38	36		50	59	86	87	104	156	173	196	104
15.02	183	159	246	164	116	98	103	75		44	43		75	106	112	107	158	248	159	183	133
16	173	214	216	173	108	89	54	75	56	59	50	50	77	54	87	103	177	209	208	154	124
Average	229	223	234	167	118	101	96	88	56	52	51	56	86	97	103	118	171	240	221	221	137

BI Upgrade: RPC

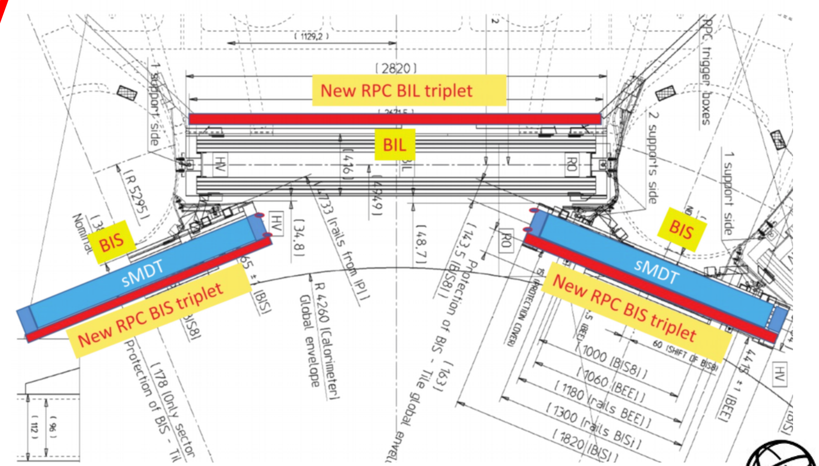
high/low pT: trigger thresholds above/below 10 GeV

All single-muon triggers use high pT

- Present RPC trigger ("high-pT") uses 3/3 coincidence of **3 RPC doublet layers** (2 in BM=middle, 1 in BO=outer)
- Not viable if RPC hit efficiency too low due to **reduced HV**
- To maintain **high trigger <u>efficiency</u>**, loosen coincidence requirements on BM and BO chambers
- To maintain **high trigger <u>selectivity</u>**, need to add more chambers to the coincidence → new layer of RPC: BI RPC project



Present (high/low pT) trigger scheme

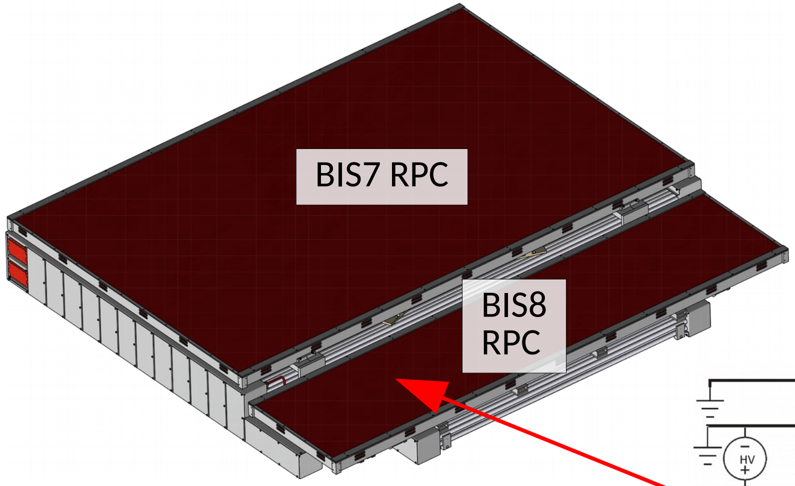


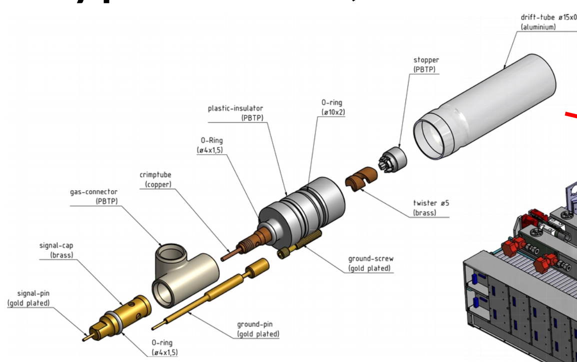
Position of new BI RPCs (X-Y view)

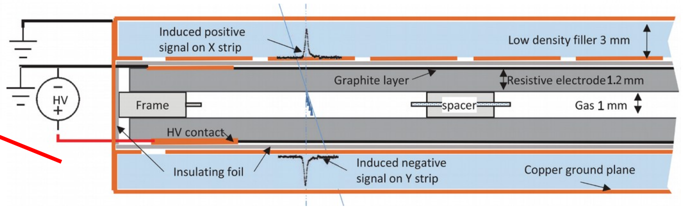
BI Upgrade: RPC+sMDT

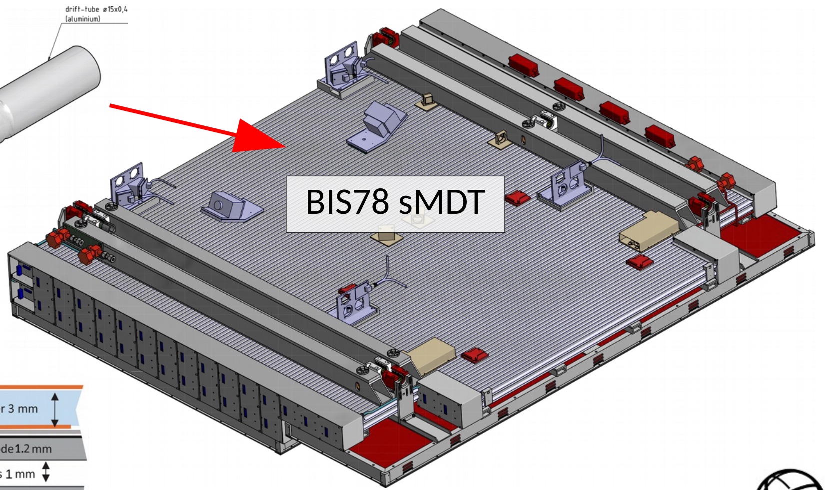
- Install **new RPC triplets** in innermost barrel layer (BI)
- 1 mm gap instead of 2 mm, 5400 V instead of 9600 V, high-sensitivity front-end elx, rate capability = tens of kHz/cm^2
- BIS78 Phase-I **pilot project**: chambers = close to final BI RPC design, electronics = prototypes

- Problem: **insufficient space** in small sectors → replace present BIS **MDT** by **sMDT** → lower profile → gain space for RPC
- **sMDT:** 15 mm tube diameter instead of 30 mm, 2730 V instead of 3080 V (same field)
- **Bonus**: 8× higher rate capability (not really needed)



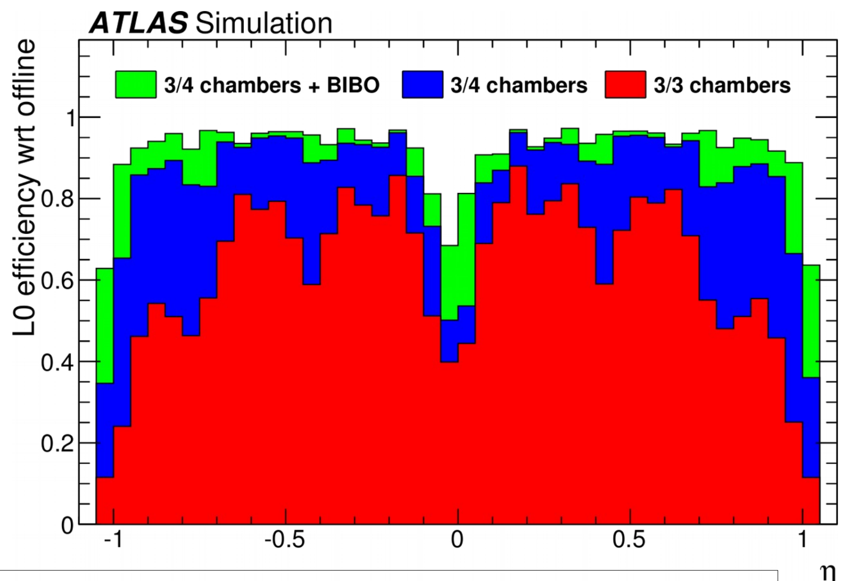




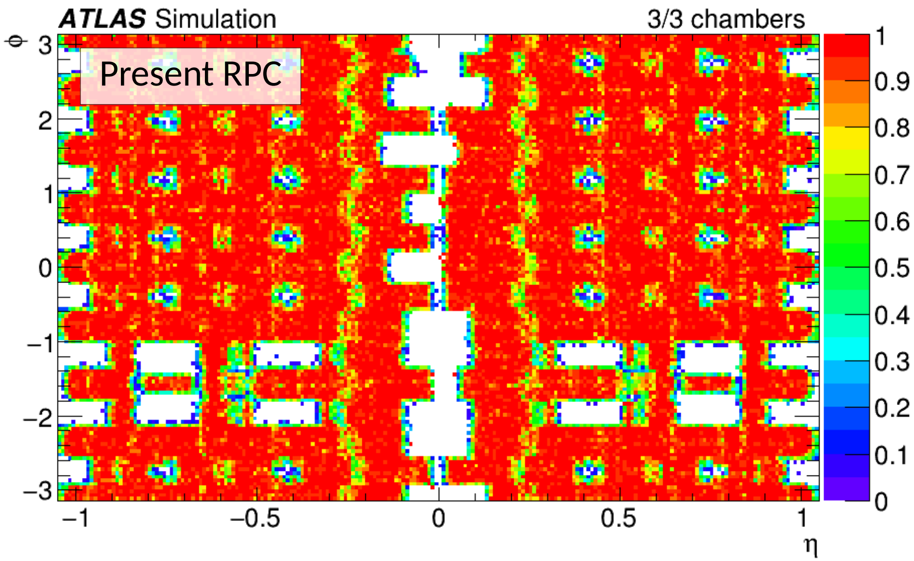


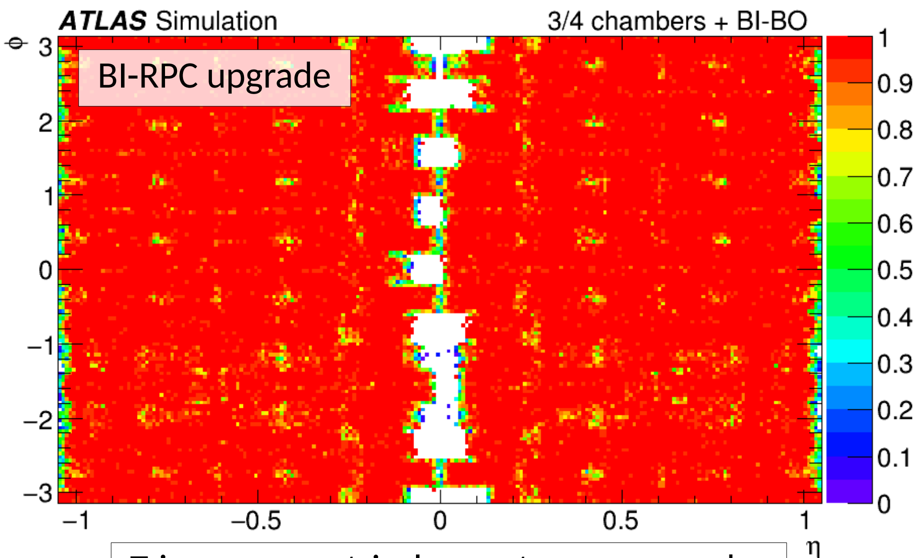
Barrel Trigger Performance

- Depending on coincidence requirements, **geometrical acceptance of trigger** increases from 78% to up to 96%
- Even for severely degraded hit efficiency in BM/BO: very good **trigger efficiency × acceptance**



Trigger efficiency × acceptance assuming hit efficiency in BM and BO degraded down to 65% (worst-case scenario)

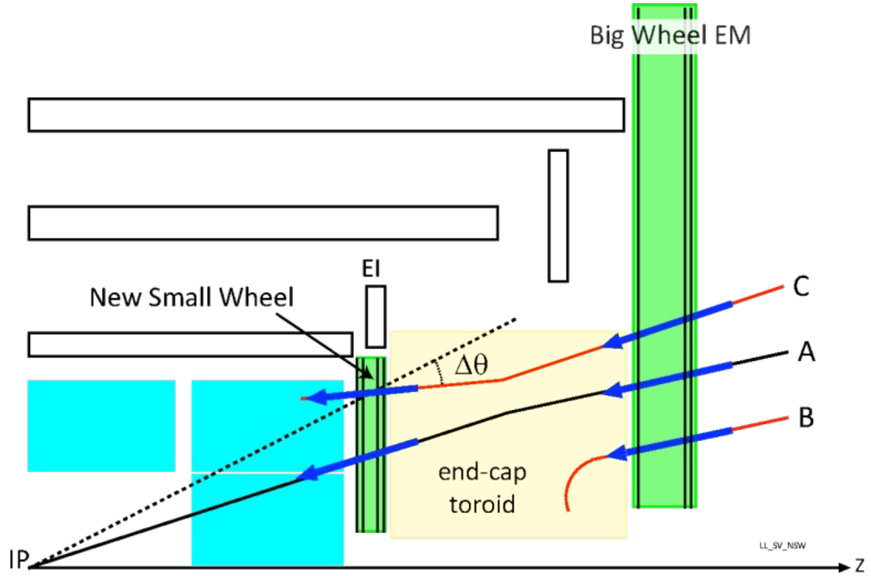


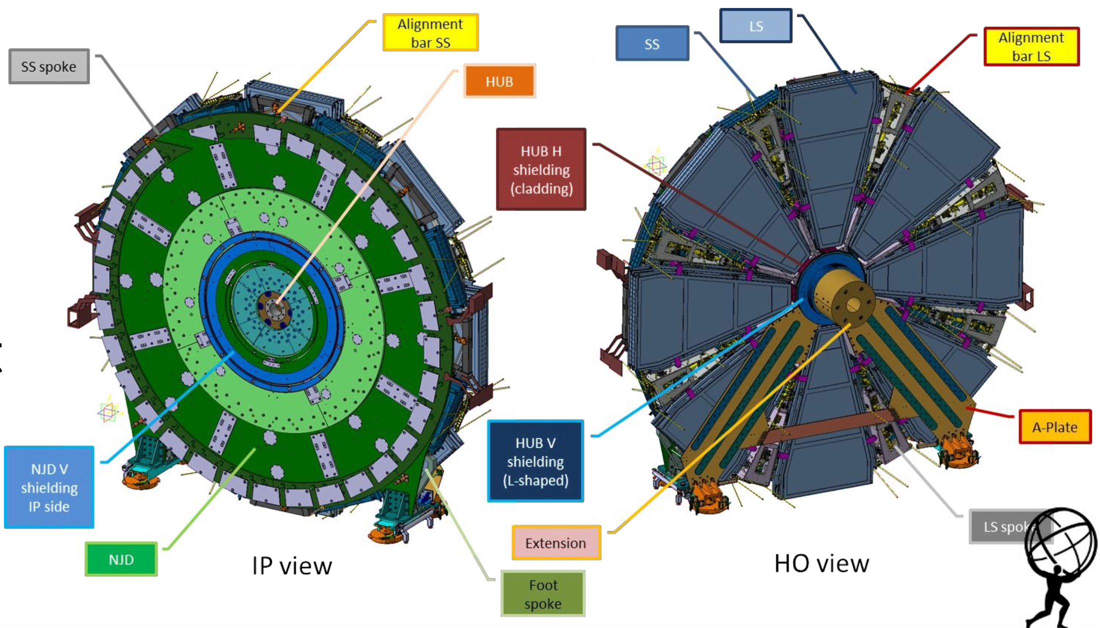


Trigger geometrical acceptance vs η and φ
Requiring hits in 3/4 of BI+BM1+BM2+BO or in BI and BO only

New Small Wheels

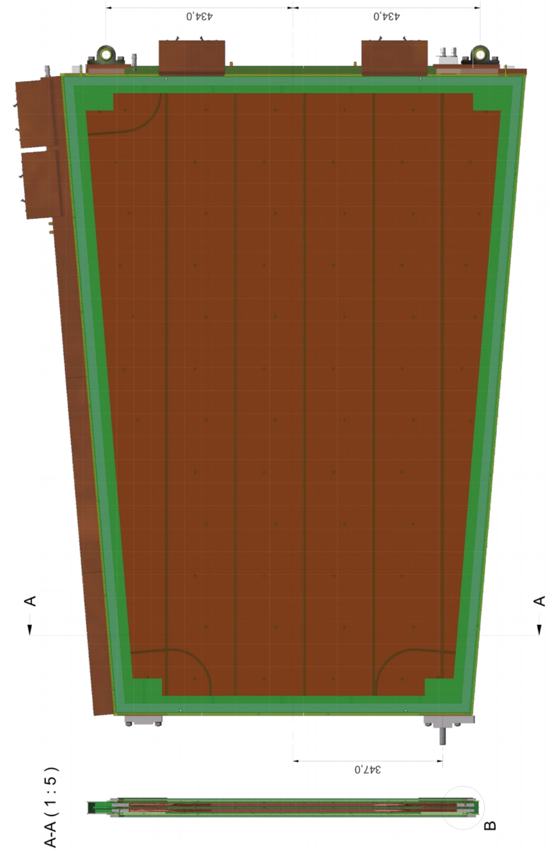
- Region of **highest rates**: endcap CSC and MDT closest to the IP (EI region, a.k.a. "Small Wheels")
- **Efficiency and resolution degrade** above $2 \times 10^{34}\ cm^{-2}\ s^{-1}$ in this region, and **90% of trigger rate** due to particles not coming from the IP
- **New Small Wheels (NSW):** replace CSC and MDT in EI by Micromegas (**MM**) and **sTGC**
- **8+8 layers**, for both **triggering** (coincidence with EM, a.k.a. "Big Wheels") and **precision measurements**, fully redundant
- Challenge: **Phase-I** project, but front-end, trigger and readout electronics **Phase-II compliant**



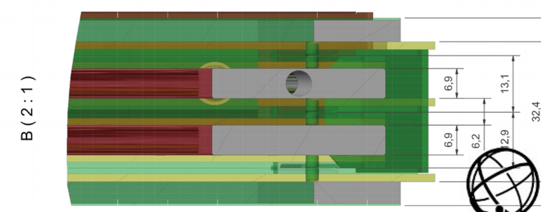


EIL4 TGC Chambers

- **EIL4 TGC chambers** at 1.0<|η|<1.3: doublet chambers, originally not foreseen to be used in trigger, but included to reduce rate of endcap triggers from non-IP tracks (same motivation as for NSW and BIS78)
- To maintain high trigger efficiency, doublets can only be used in a **1/2 coincidence**; this, and too large coincidence windows, would result at HL-LHC in **9 MHz trigger rate from cavern background**
- **Replace** doublets by triplets, with smaller coincidence windows → enable a more robust **2/3 coincidence**, much less sensitive to background

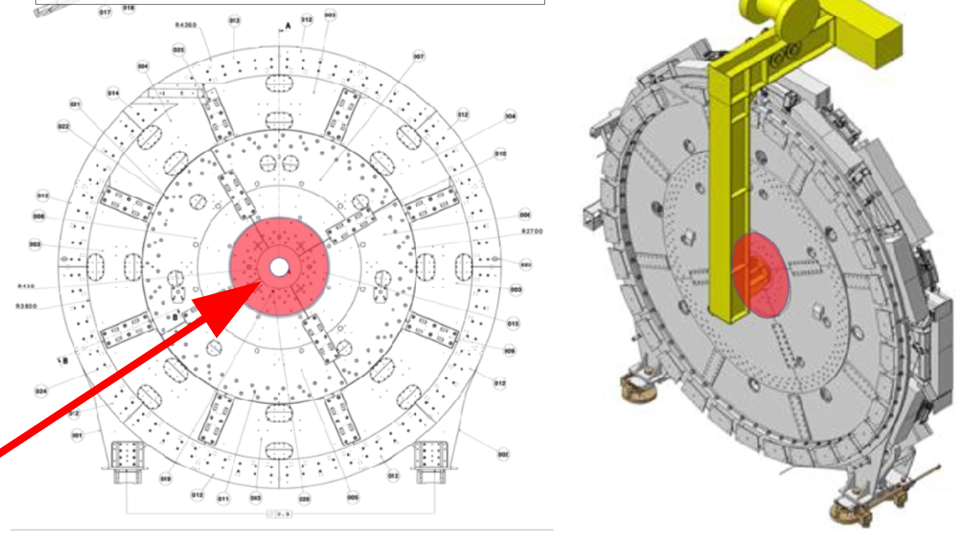


TGC triplet mechanical design

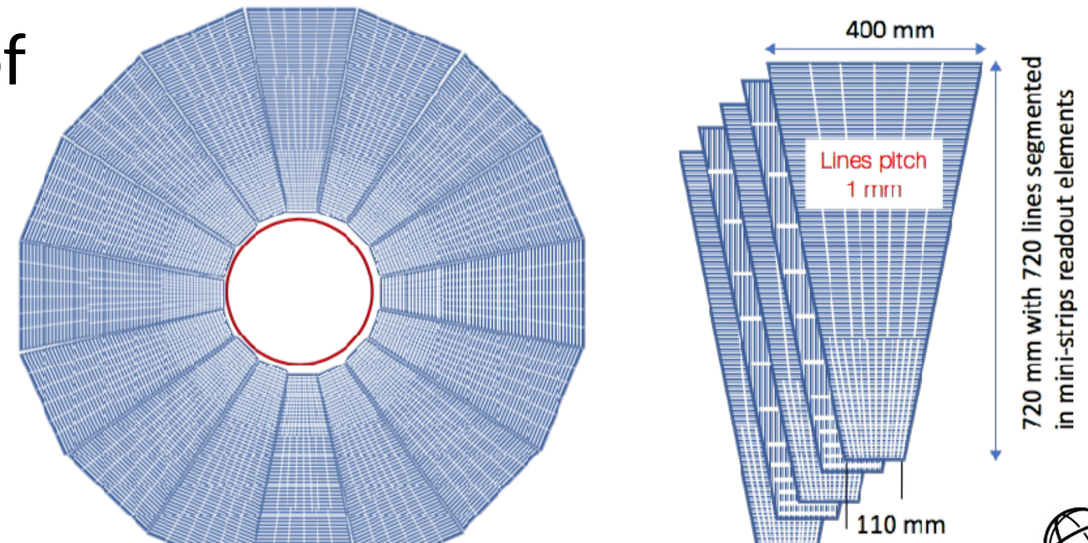


High-η Tagger (Option)

- New **Inner Tracker** (ITk) will cover up to |η|<4.0 – present muon spectrometer **coverage** ends at |η|<2.7
- Studying the option to install a **muon tagger** on innermost part of NSW shielding disk – to **identify** (tag) ITk tracks as muons (measurement of momentum solely by ITk)
- **Less advanced** than the remainder of the muon Phase-II program, R&D focusing on choice of **detector technology**



Location on NSW shielding disk



Conceptual detector layout

Front-End Electronics

- **ATLAS electronics** were **qualified for doses** corresponding to at least 1000 fb^{-1}, including large **safety factors**
- After first years of LHC operation, simulations were found to agree well with data: **updated (reduced) safety factors** compensate for most of 1000 $fb^{-1} \rightarrow$ 3000/4000 fb^{-1}
- **Replace electronics** only if no longer adequate for purpose – not for radiation considerations
- **Front-end electronics** for signal amplification, shaping, discrimination do not need modification for HL-LHC running
- Replace **digital electronics** that implements e.g. buffers of fixed size, assumptions about trigger scheme and rates, etc.

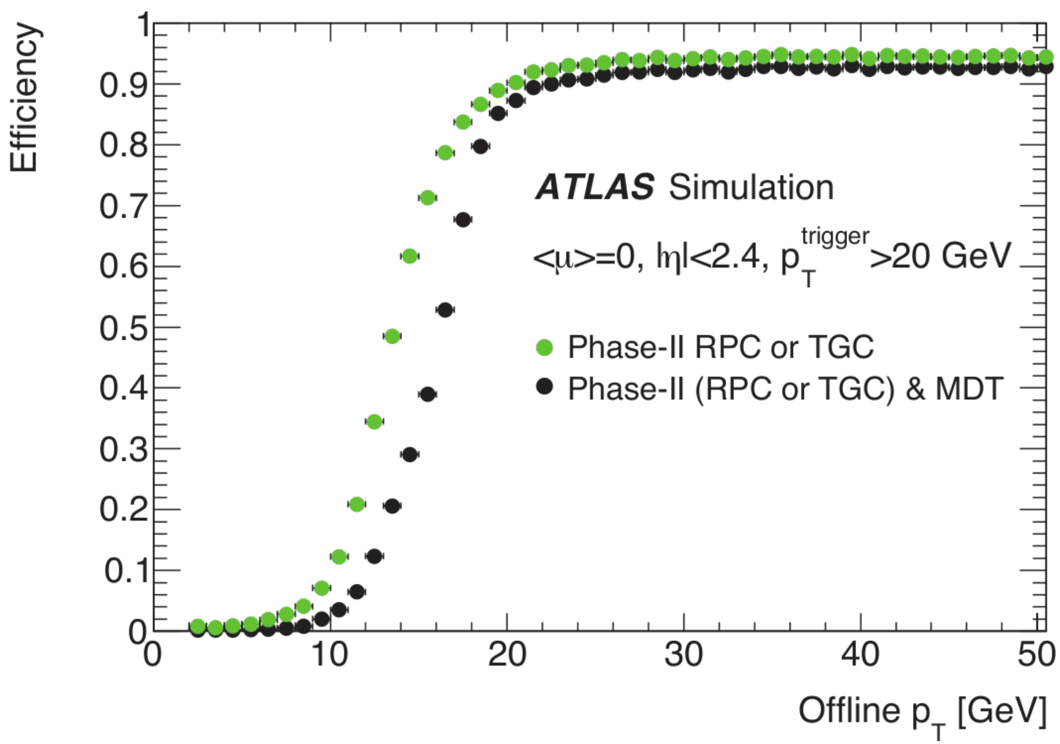
RPC and **TGC** front-end electronics **(ASD)** will remain on chambers

MDT front-end electronics **(ASD + TDC = mezzanine cards)** will be replaced

ASD would still be adequate, but hit buffers in **TDC** too small, and data transmission rates insufficient

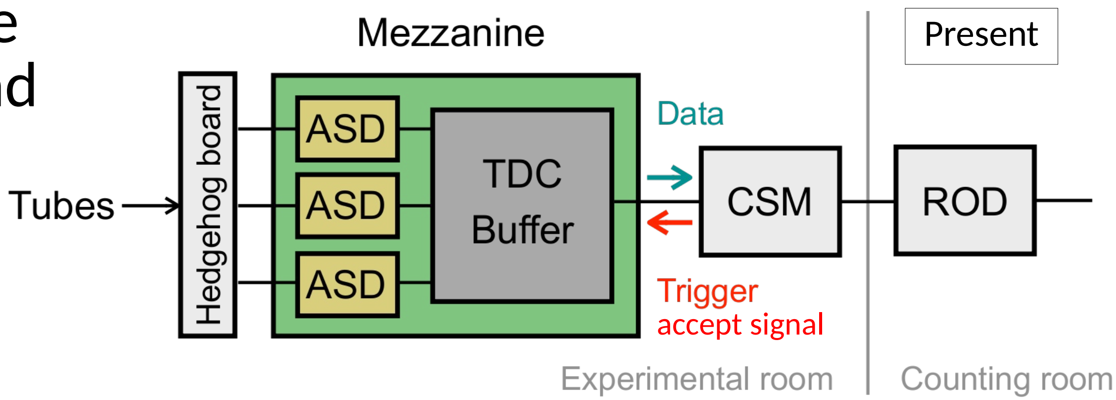
MDT Trigger

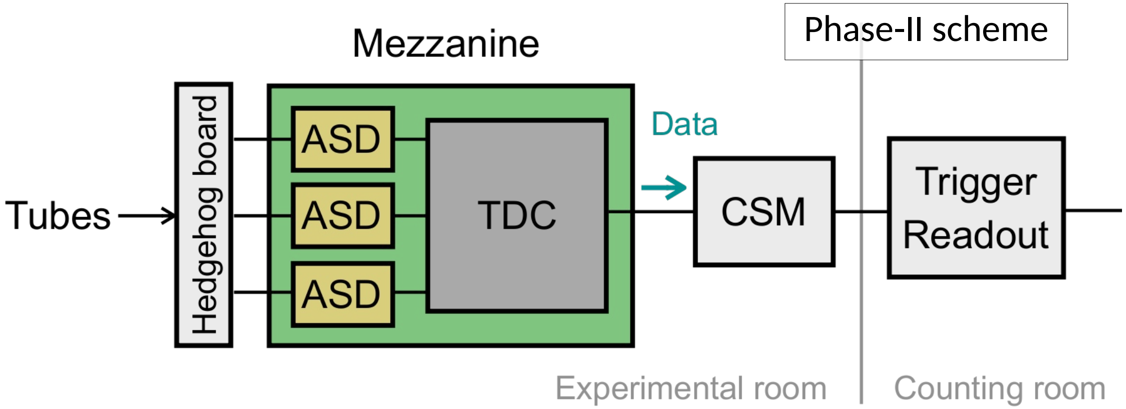
- Presently, **MDT** information used only in High-Level Trigger (HLT), not in L1
- **pT resolution** limited by position resolution and alignment of **RPC** and **TGC**
- Phase-II upgrade: use **MDT** information in L0 trigger to **sharpen the pT threshold**
- **Trigger rate** reduced by >50%
- Optionally, gain in **efficiency** by accepting **loose RPC/TGC** coincidences if confirmed by **MDT** (e.g. BI-BO)
- Challenges: computing-intensive, maximum L0 **trigger latency** → need hit information available for trigger decision **fast**



MDT Trigger and Readout

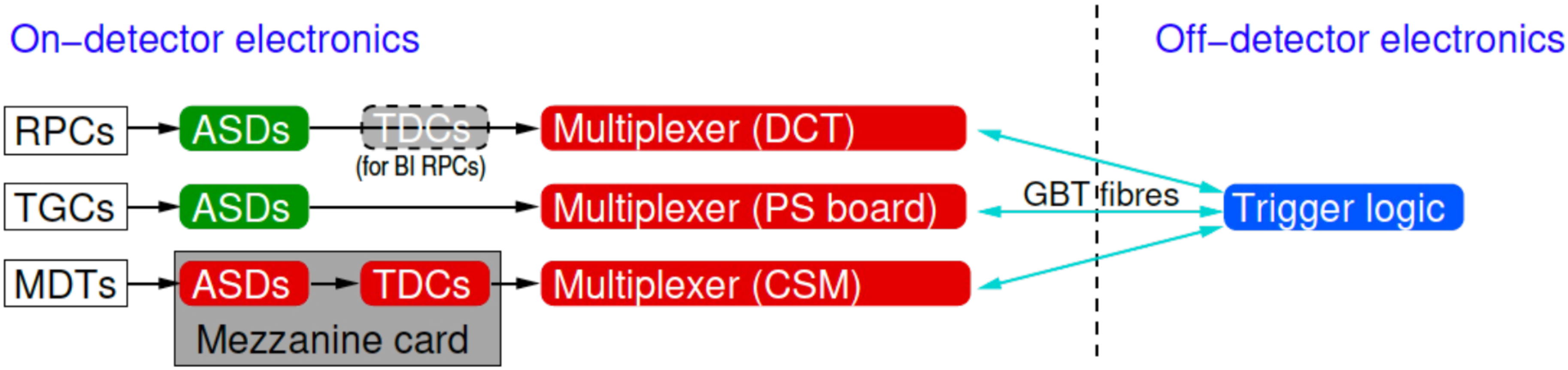
- Present **triggered MDT readout:** on L1 trigger accept signal, all hits inside a time window are retrieved from TDC buffer and sent to counting room
  - Saves **bandwidth** at low trigger rates – but not at high (Phase-II) rates
  - **Waiting** for trigger signal – costs time
  - At Phase-II trigger rates, the same hit may even be sent **multiple times**
- Replace by **trigger-less MDT readout**: send out every hit to counting room <u>immediately</u>





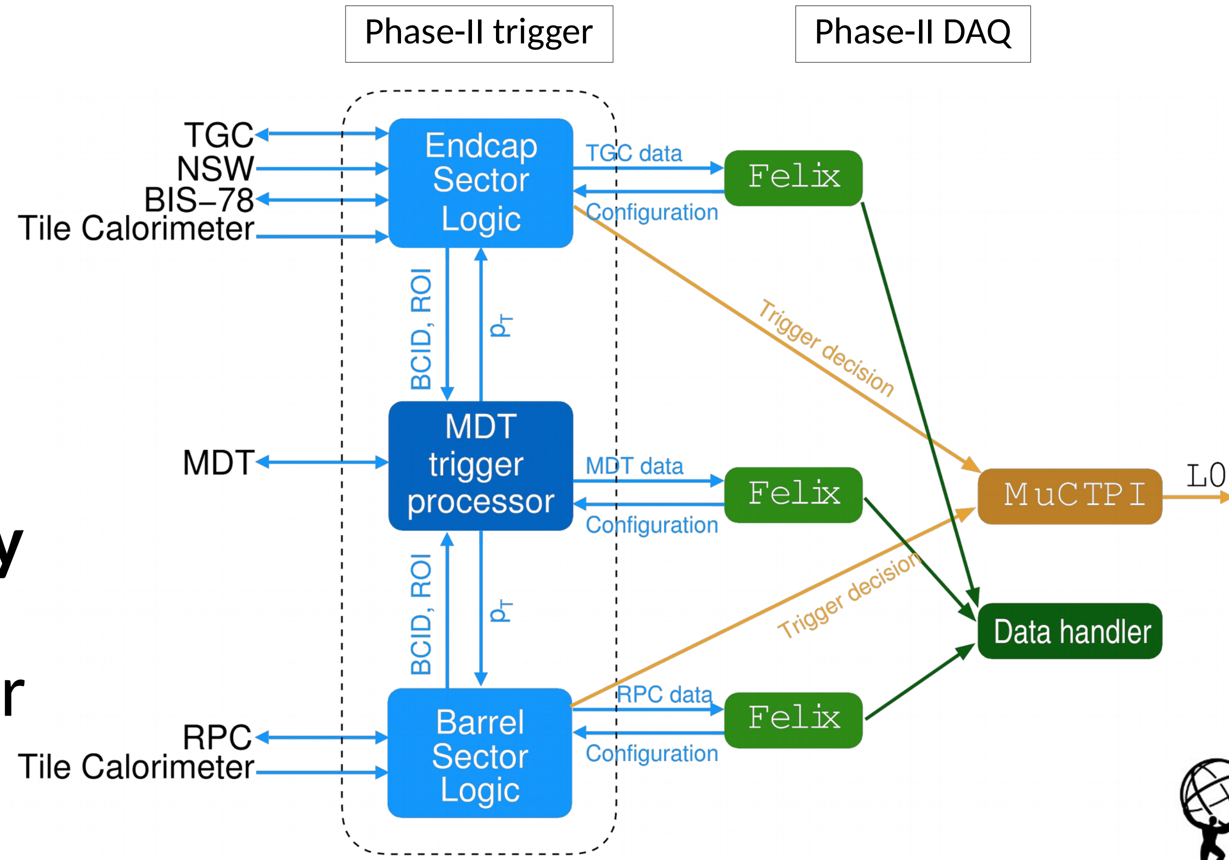
RPC/TGC Trigger & Readout Electronics

- In **present scheme**, RPC and TGC **on-detector trigger and readout electronics** implements the **L1 trigger** (coincidence matrices) and sends a trigger signal to the counting room
- In **Phase-II scheme**, send out all the hits from the detectors, make the **L0 trigger decision** in counting room
- "**Intelligent**" on-detector trigger and readout electronics replaced by "**stupid**" data multiplexers and high bandwidth



Trigger and DAQ

- Can use **commercial** (non radiation-hard) **FPGAs or CPUs** instead of hard-wired rad-hard coincidence logic → enable more **sophisticated** trigger algorithms
- MDT trigger **seeded** by RPC/TGC trigger candidates, to reduce required computing power
- On L0 trigger accept: all **hit data are already available** in counting room → direct transfer to DAQ system



Power System

- **HV/LV power distribution system** (CAEN EASY 3000 family) has been designed in 2000-05, qualified for radiation corresponding to 1500 fb^{-1} (after safety factors update)
- **Aging** + **irradiation** + **obsolescence of components** (→ no more main-tenance/repairs): very unlikely the system will survive until 2035-40
- Planning for **gradual replacement,** operating old+new components together for ~5 years (2025-30)
- Requires the new design to be as **backward-compatible** as reasonably achievable

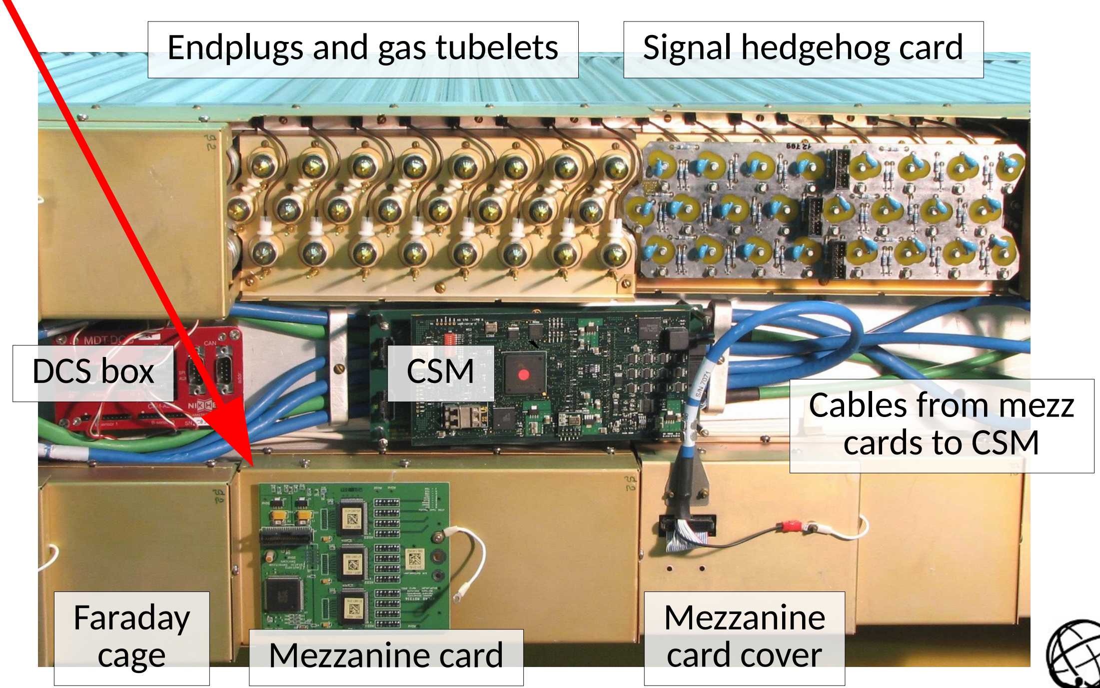
CAEN module	Function	MDT	RPC	TGC	CSC	Total
A3000NF	3-phase notch filter	11	2	2		15
A3009	12 ch. 8V/9A/45W		92			92
A3016B	6 ch. 8V/16A/90W	32				32
A3025A	4 ch. 8V/25A/150W		25			25
A3025B	4 ch. 8V/25A/150W	126	86			212
A3025D	4 ch. 8V/25A/150W			79		79
A3050D	2 ch. 25-80A/150-450W			30		30
A3100D	1 ch. 8V/100A/600W			84		84
A3485	2 ch. 3-phase 400V AC-48V DC	23	4	5	3	35
A3486	2 ch. 3-phase 400V AC-48V DC		28	30	2	60
A3512A	6 ch. 12kV/1mA		89			89
A3535A	32 ch. 3.5kV/0.5mA			134	22	156
A3540A	12 ch. 4kV/1mA	208			13	221
A3801	128 ch. ADC		58			58
A3802	128 ch. DAC		32			32
A1676A	EASY branch controller	18	23	16	2	59
EASY3000	RPC and TGC crate		88	24	4	116
EASY3000M	TGC special crate			26		26
EASY3000R	TGC special crate			12		12
EASY3000S	MDT crate	72				72
SY4527A	Mainframe	3	4	2	8	17
Total		**493**	**531**	**444**	**54**	**1522**

Inventory of the present muon power system

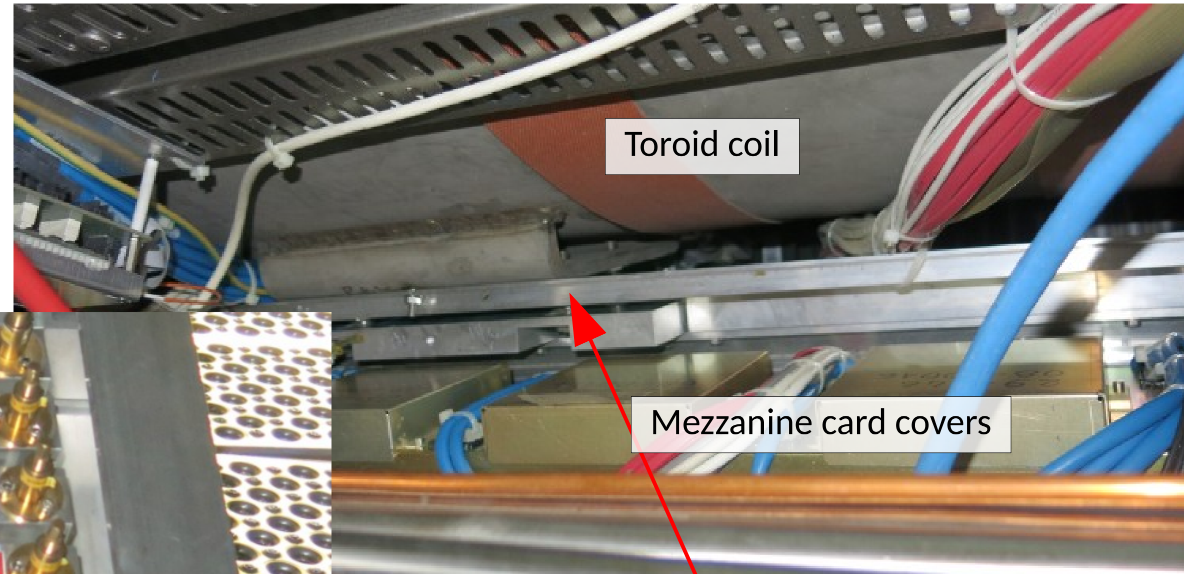
Installation

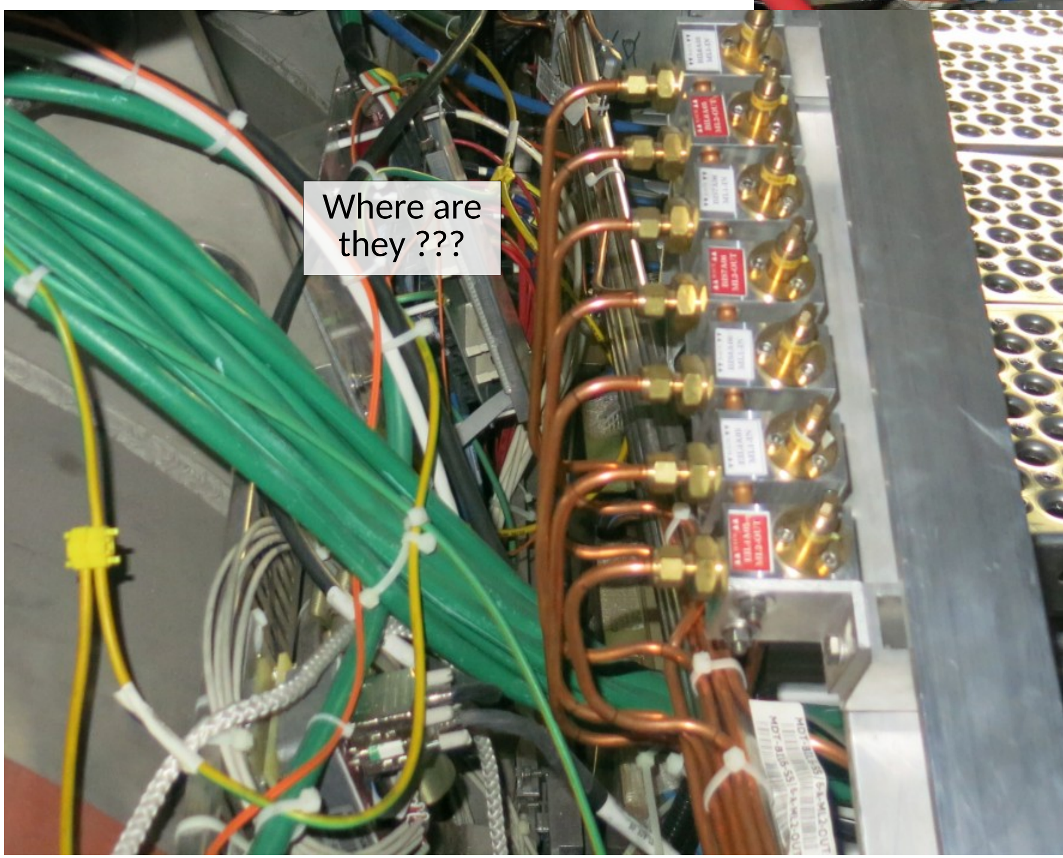
- Replacement of on-detector **trigger and readout electronics**: O(1,000) components (CSM, Pad/Splitter, PS board) for each of MDT, RPC, TGC, reasonably good **access**
- Much more difficult is replacement of **MDT mezzanine cards**: O(15,000) electronics cards
- Need 15–30 min per card, with **access** conditions ranging from challenging to extremely demanding
- Given "short" duration of LS3, most or all mezzanine cards have to be **replaced in situ**, without moving or removing chambers

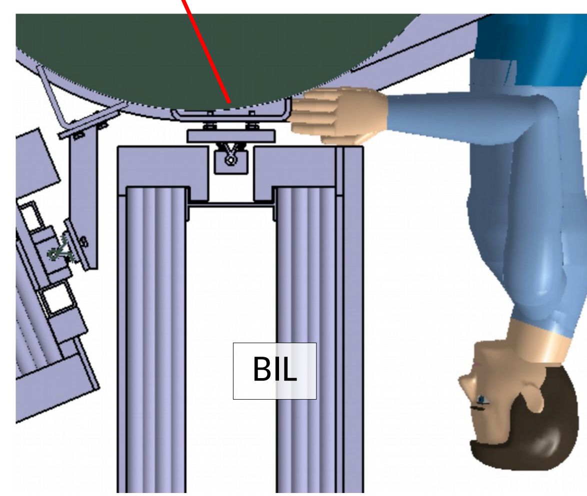
Partially disassembled MDT Chamber (view along tubes)



Installation

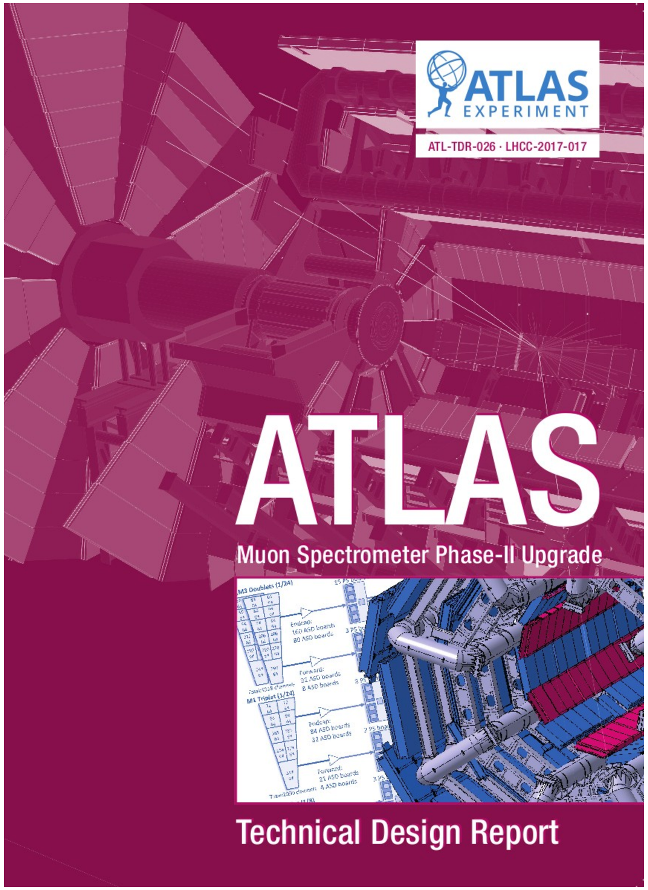






Summary

- For HL-LHC running, the **ATLAS muon system** needs to be **upgraded** in LS3
- Installation of new **RPCs,** including the **MDT in the trigger,** and replacement of some **TGCs** will improve the robustness and selectivity of the trigger
- All on- and off-detector **trigger and readout electronics** will be replaced, as well as all the MDT **mezzanine cards**
- The **power system** will be replaced
- This completes the upgrade program of the muon system that starts with the **New Small Wheels** upgrade in LS2



http://cds.cern.ch/record/2285580

Summary

- **ATLAS posters related to Muon Phase-I/II upgrades:**
  - **BIS78:**
    - Design and Construction of Integrated Small Diameter Drift Tube Chambers and Thin-Gap Resistive Plate Chambers for the Phase-I Upgrade of the ATLAS Muon Spectrometer – *H. Kroha*
  - **NSW:**
    - Small-Strip Thin Gap Chambers for the Muon Spectrometer Upgrade of the ATLAS Experiment – *R. Rojas*
    - Studies of the MicroMegas performances using INFN SM1 prototype with data recorded at the LNF cosmic ray test – *G. Mancini*
    - High Voltage Stability and Cleaning of 2 m^2 Resistive Strip Micromegas Detectors – *P. Massarotti*
    - Performance and Calibration of 2 m^2 Micromegas Detectors for the ATLAS Muon Spectrometer Upgrade – *G. Maniatis*

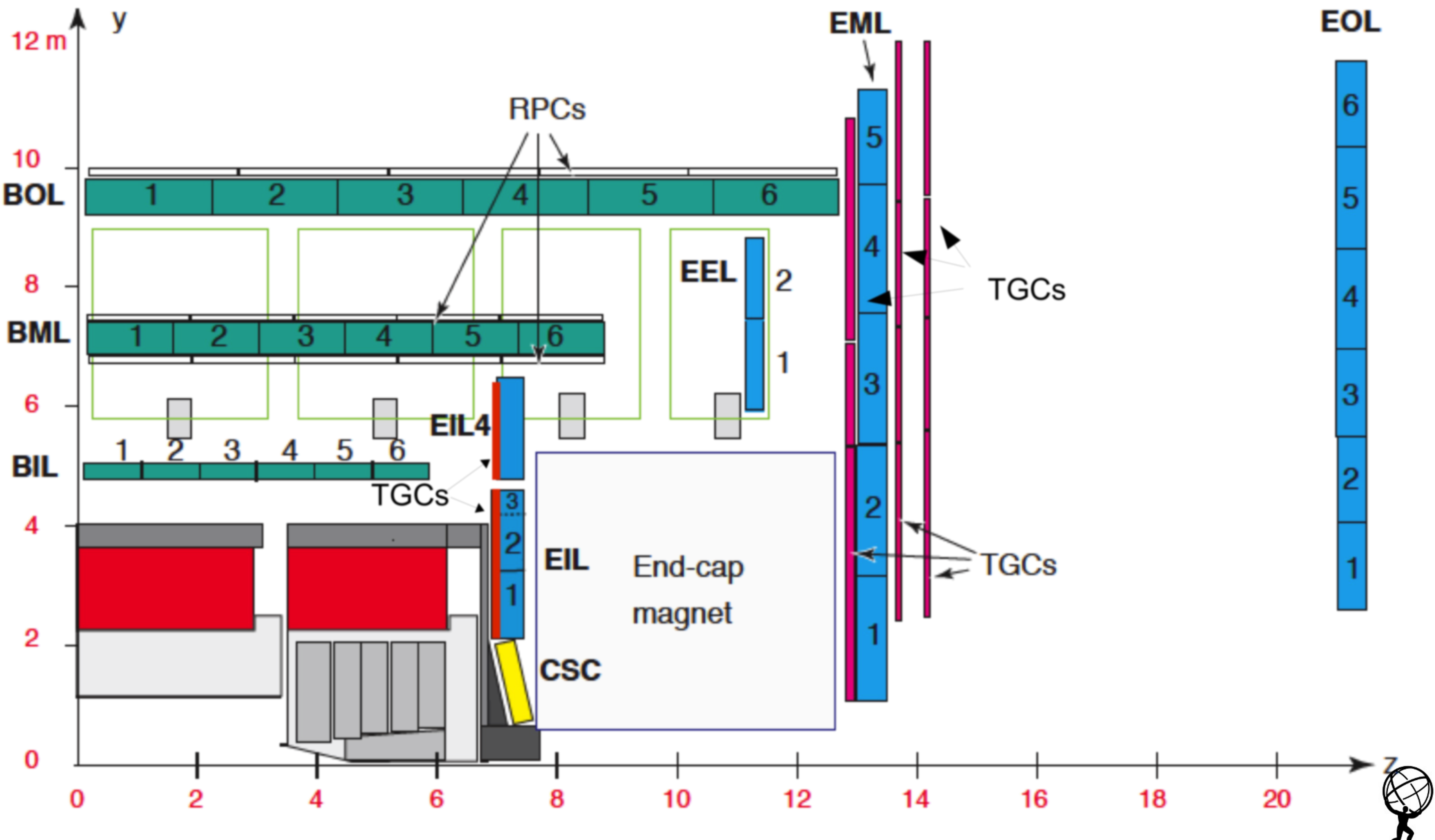
Backup

Phase-II Trigger Menu

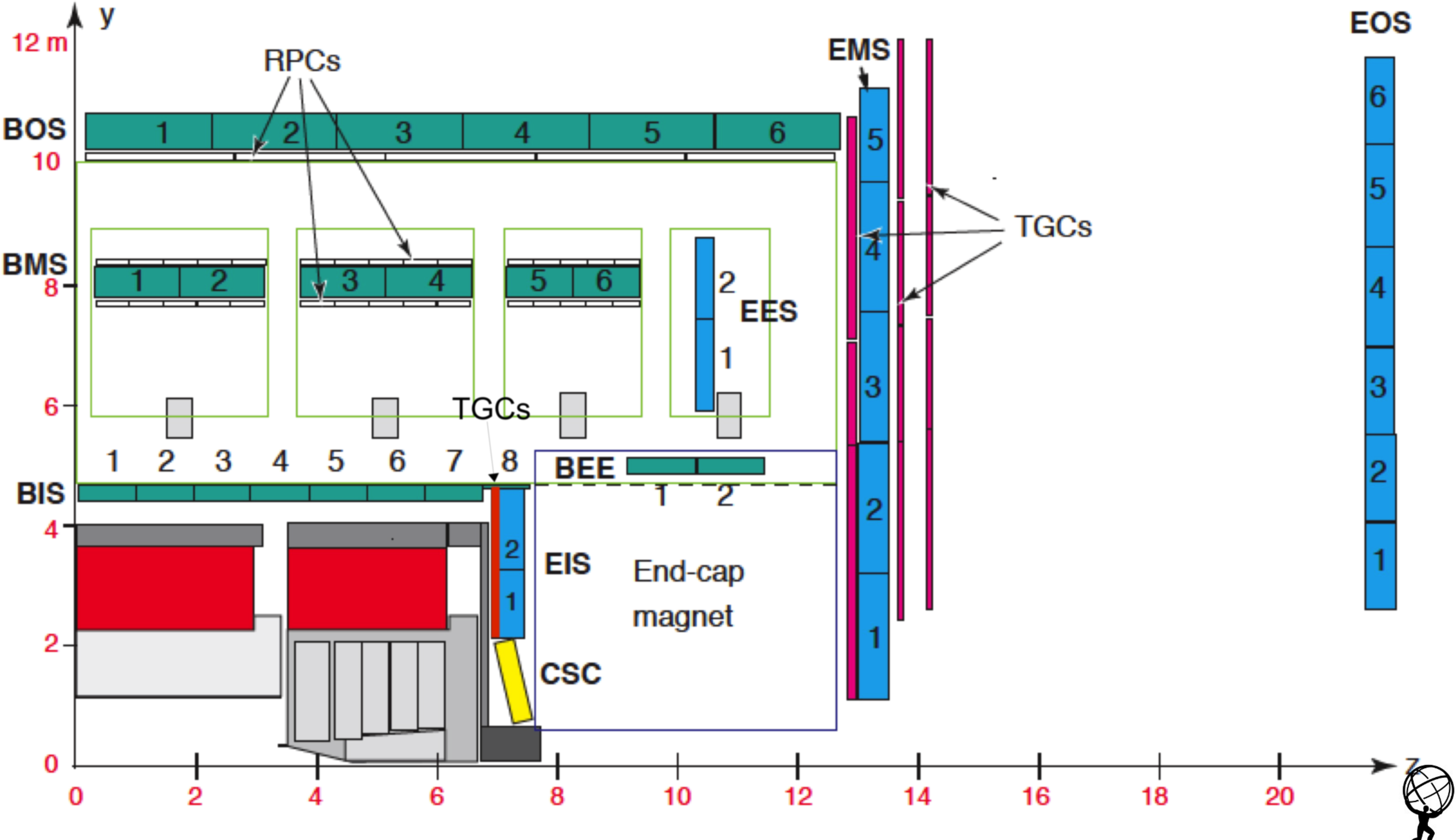
Trigger Selection	Run 1 Offline p_T Threshold [GeV]	Run 2 (2017) Offline p_T Threshold [GeV]	Planned HL-LHC Offline p_T Threshold [GeV]	L0 Rate [kHz]	After regional tracking cuts [kHz]	Event Filter Rate [kHz]
isolated single e	25	27	22	200	40	1.5
isolated single μ	25	27	20	45	45	1.5
single γ	120	145	120	5	5	0.3
forward e			35	40	8	0.2
di-γ	25	25	25,25		20	0.2
di-e	15	18	10,10	60	10	0.2
di-μ	15	15	10,10	10	2	0.2
$e-\mu$	17,6	8,25 / 18,15	10,10	45	10	0.2
single τ	100	170	150	3	3	0.35
di-τ	40,30	40,30	40,30	200	40	0.5†††
single b-jet	200	235	180	25	25	0.35†††
single jet	370	460	400			0.25
large-R jet	470	500	300	40	40	0.5
four-jet (w/ b-tags)		45† (1-tag)	65(2-tags)	100	20	0.1
four-jet	85	125	100			0.2
H_T	700	700	375	50	10	0.2†††
E_T^{miss}	150	200	210	60	5	0.4
VBF inclusive			2x75 w/ ($\Delta\eta > 2.5$ & $\Delta\phi < 2.5$)	33	5	0.5†††
B-physics††				50	10	0.5
Supporting Trigs				100	40	2
Total				1066	338	10.4

† In Run 2, the 4-jet b-tag trigger operates below the efficiency plateau of the Level-1 trigger.
†† This is a place-holder for selections to be defined.
††† Assumes additional analysis specific requires at the Event Filter level

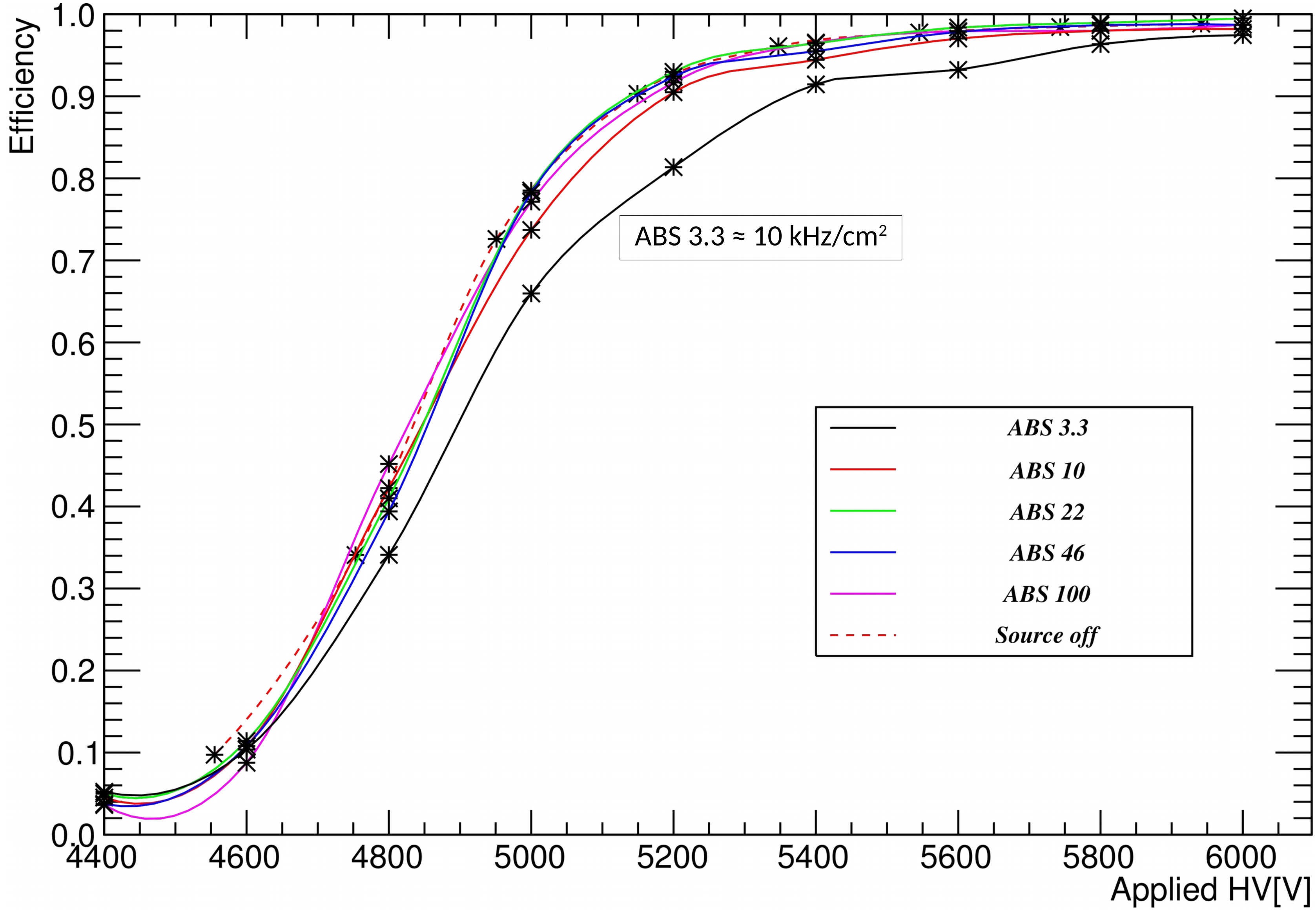
Large Sector



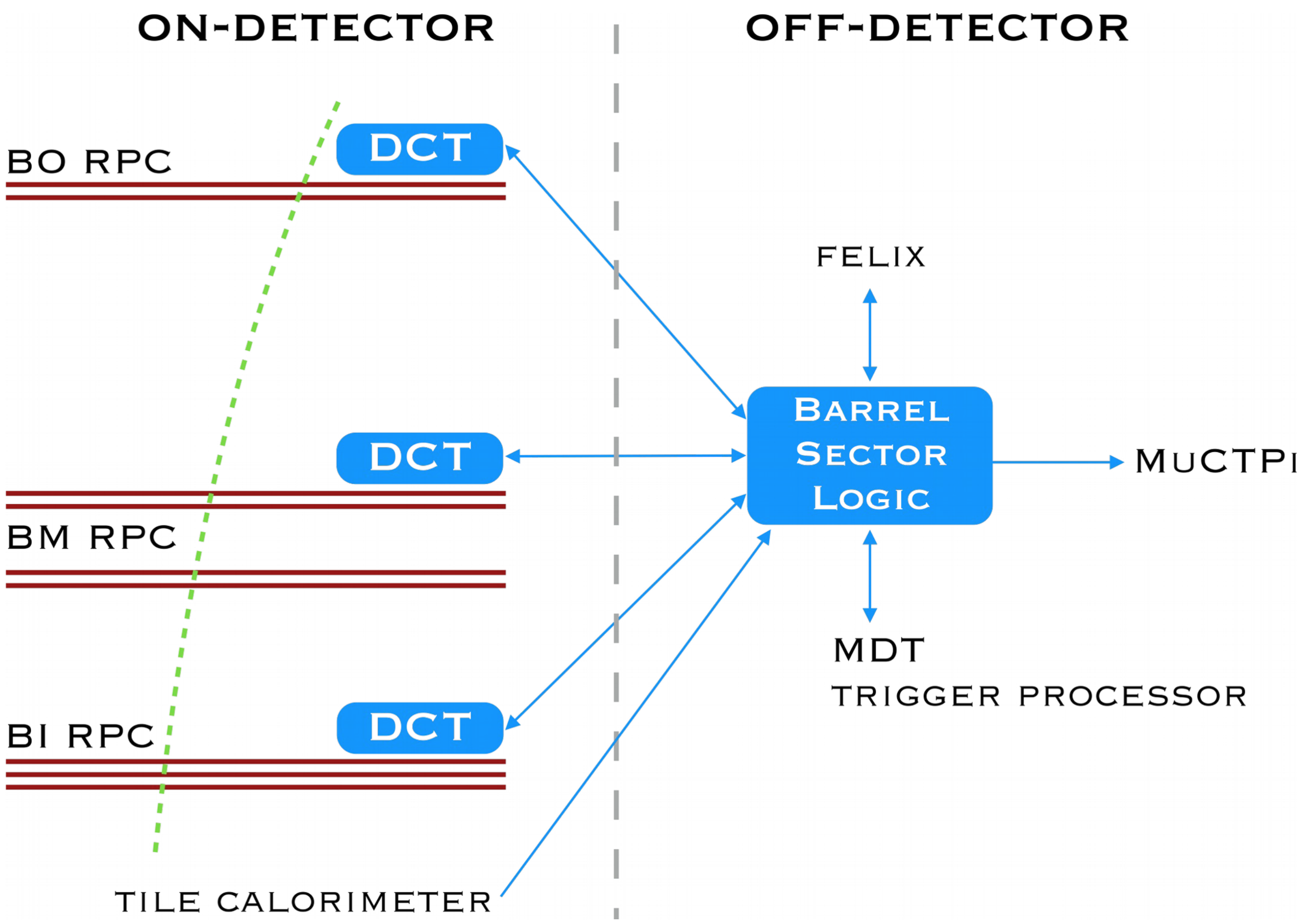
Small Sector



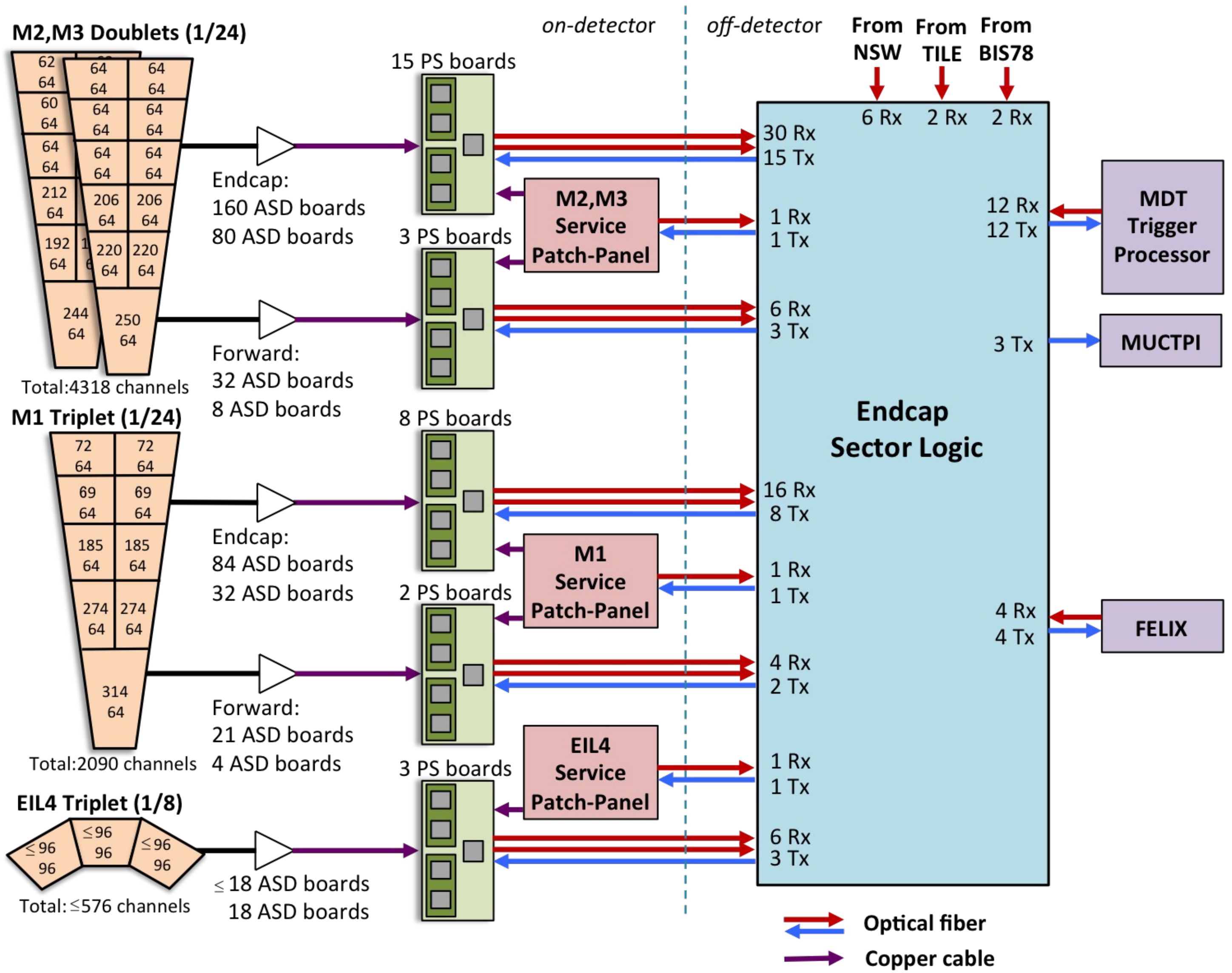
Performance of New RPC



RPC Trigger and Readout Scheme



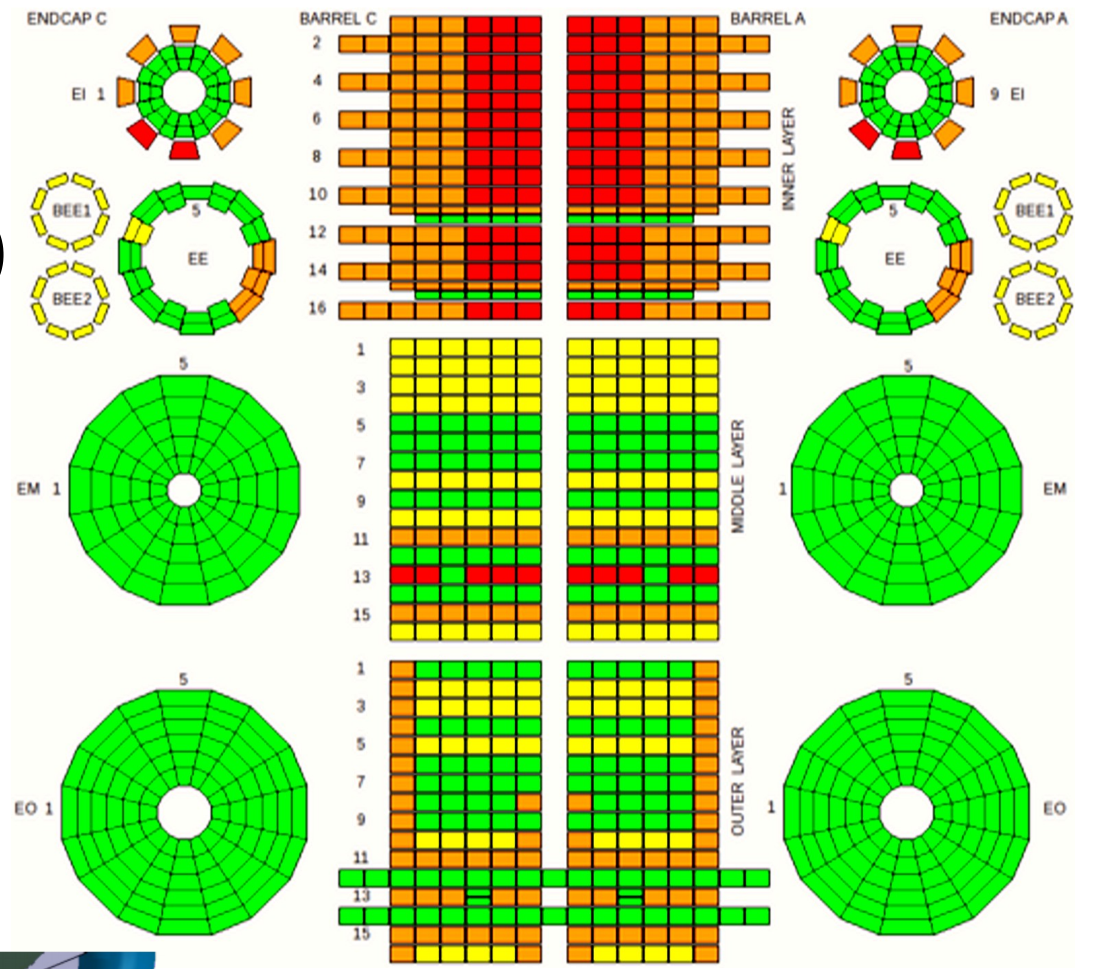
TGC Trigger and Readout Scheme

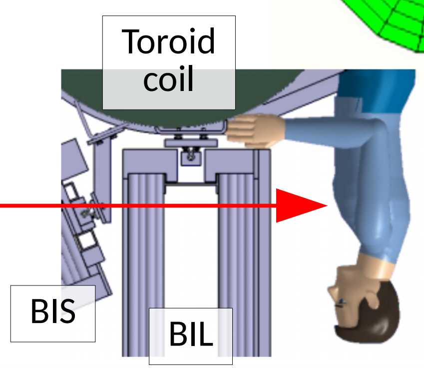


Installation

- Detailed study of **in-situ access to mezzanine cards** (without moving chambers)
- **BIL** are most problematic, developed two scenarios:
  - Temporarily remove BIL chambers to **surface**
    Many other chambers need to be disconnected and moved out of the way → risk of damage
  - **In-situ** access to BIL, moving chambers ~80 cm along rails
    Physically challenging working conditions → risk of damage

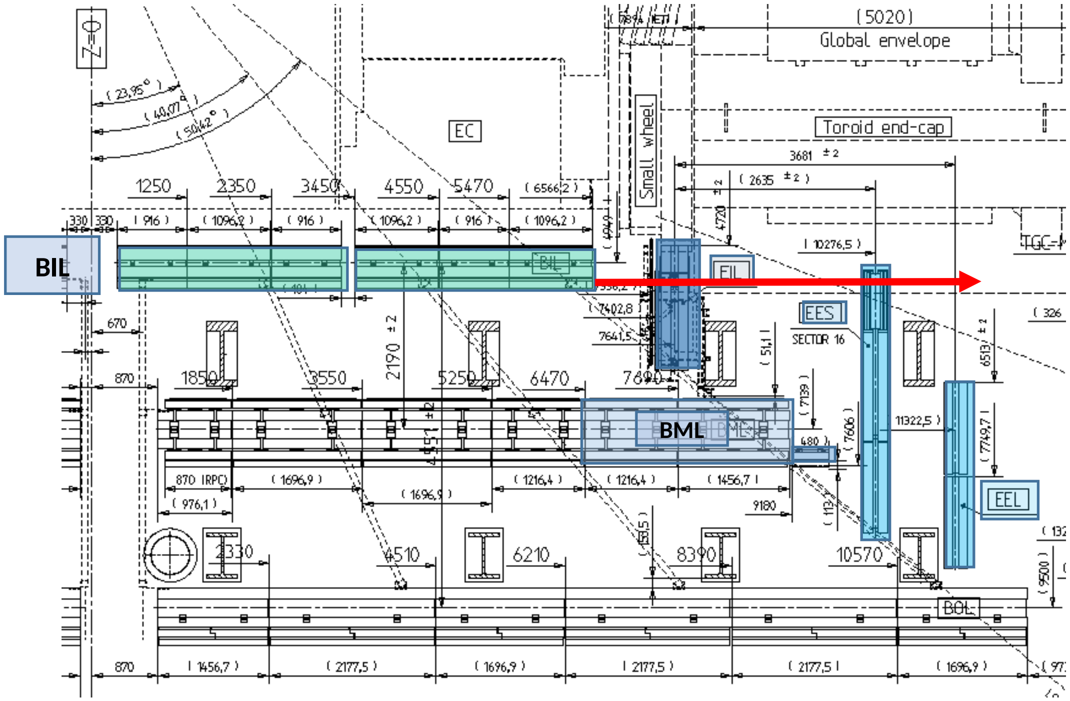
BIS: will be replaced by sMDT, are easier to move out





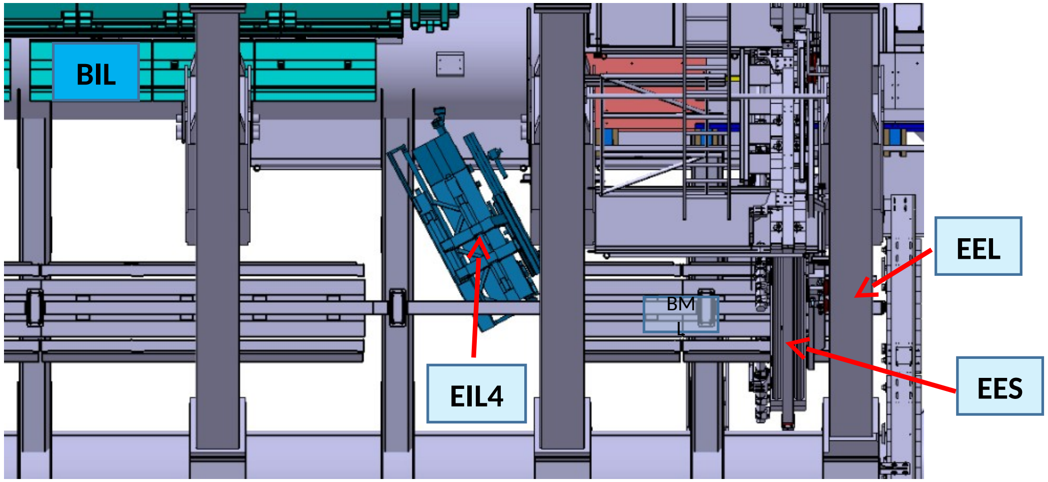
- "Easily" accessible
- Requires temporary scaffolding or platform
- Doable but needs dedicated engineering study
- No idea how to access without moving chamber

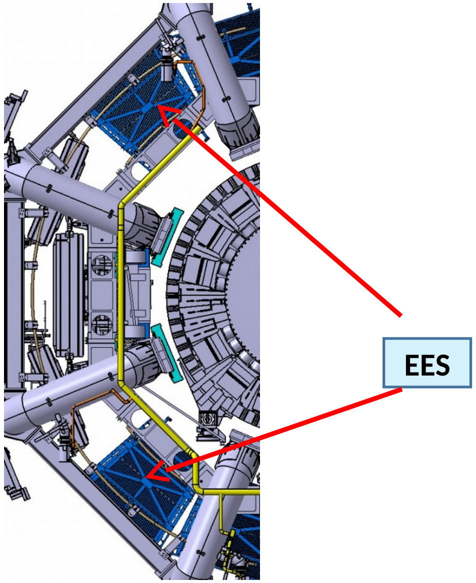
Scenario 1: Temporarily Remove BIL



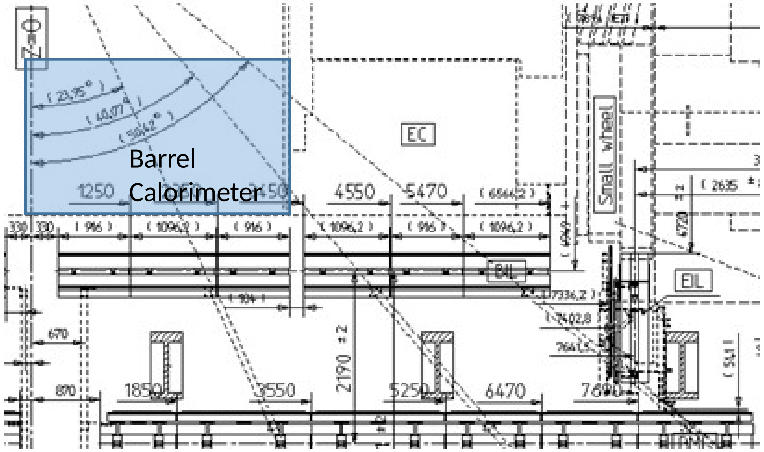
For removal of BIL chambers from the detector:

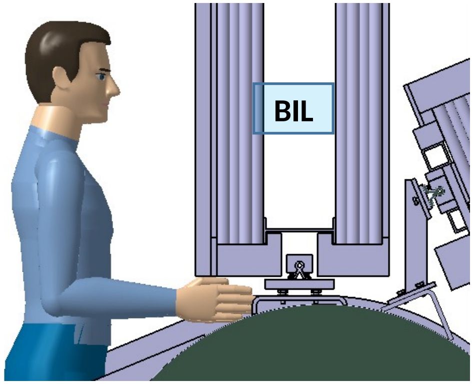
- Move EES sectors in azimuth to make space for BML
- Move BML 5,6 along beam line to make space for EIL4
- Move EIL4 radially and rotate to make space for BIL

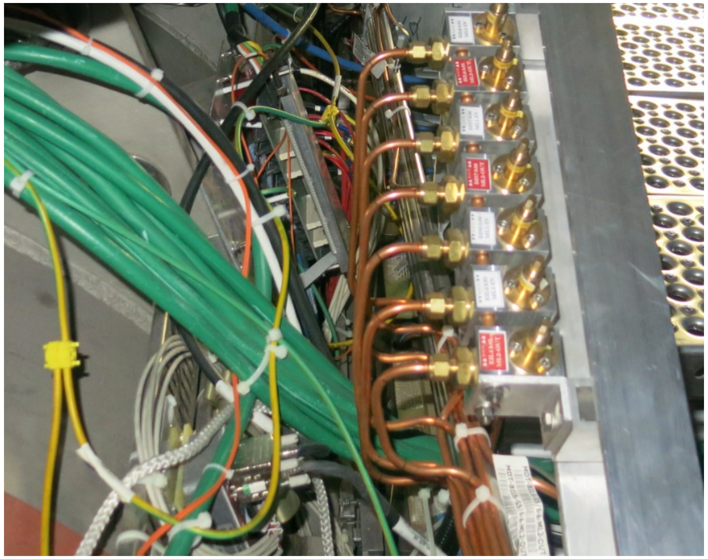




Scenario 2: In-situ Access to BIL







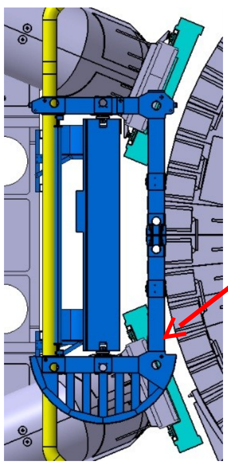
- Even if BIL remain in the detector, It is necessary to slide BILs along rails to disconnect BIS services
- To move BIL, all BIL services need to be disconnected
- Some BIL mezzanine card (covers) are at least easily visible (top right picture), others are very difficult to get to (bottom right). Need to foresee modification of platforms, removal of some services: boxes, cables, pipes

Tests have shown that in principle the space is marginally sufficient for the removal of old cards and replacement by new ones

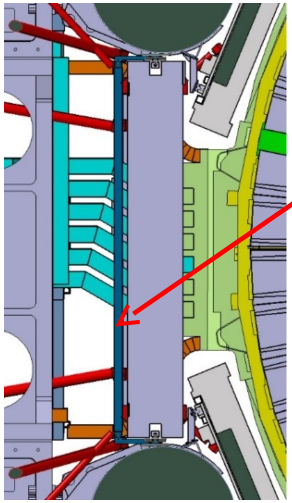
BIL RPC Installation

Scenario 1:

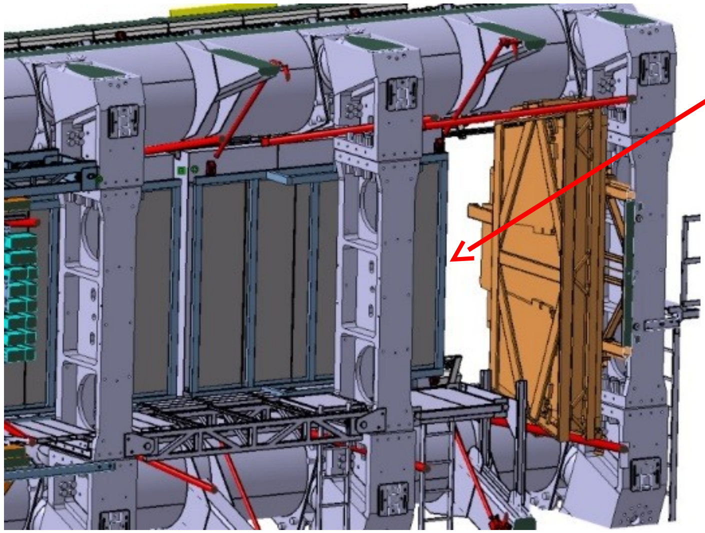
The same frame as for MDT installation can be adapted for the RPC



BIL MDT frame

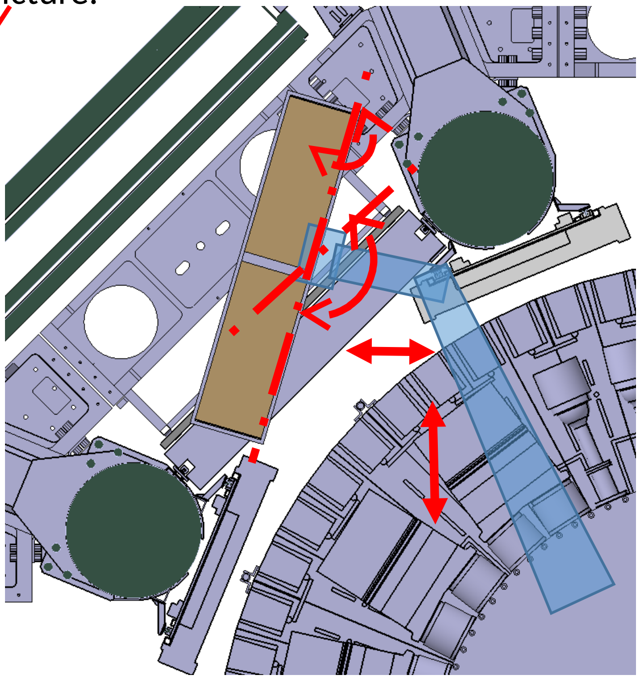


RPC



Scenario 2:

Space between EIL4 and BIL6 can be used for the insertion of the RPCs .
Procedure of manipulations is complicated, access very difficult. We need to consider special tools to be ordered/designed/produced.
One example of a similar tool shown in the picture.



Schematic view of the tool functions for the RPC installation in scenario 2.