Technologies for Future Vertex and Tracking Detectors at the Compact Linear Collider (CLIC)

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The Compact Linear Collider

- Proposed linear collider with two-beam acceleration: Achieves field gradients of ~100 MV/m
- Construction in 3 stages: 380 GeV → 3 TeV
- Physics goals: **precision SM Higgs, Top and BSM physics**
- Vertex & Tracker design driven by beam structure
  - Trains of 312 bunches, 50Hz repetition rate
  - Spacing between bunches: 0.5ns
- High bunch density leads to interactions between bunches
  - Large background from $\gamma \gamma \rightarrow$ hadrons / e+e- (beamstrahlung):
  - ~100 particles/BX within acceptance (at 3TeV)
  - Mostly in forward direction
  - Timing cuts can reduce impact
CLIC Vertex & Tracking Detectors

• All-silicon vertex & tracking detectors

• Requirements:
  • **Low mass** – 0.2% $\chi_0$ per vertex layer
  • **Low power consumption** – 50mW/cm$^{-2}$ in the vertex, air-flow cooling
  • **High single-point resolution**
    • Vertex: $\sigma_{sp} \sim 3\,\mu m$
    • Tracker: $\sigma_{sp} \sim 7\,\mu m$
  • **Precise time stamping** ~5ns

• Large area tracker (140m$^2$) with high granularity, elongated pixels (1 – 10mm)
Silicon Technologies

Hybrid

HV-CMOS

HR-CMOS

SOI

Capacitive

ELAD
Hybrid Pixel Detectors

- Traditional design of HEP silicon pixel detectors with independent parts:
  - Sensor (high-resistivity silicon with pn-junction)
  - CMOS readout chip with small feature size
  - Solder bumps as interconnect
- Allows extensive functionality on-pixel using mixed-mode CMOS circuits
- Small pixel cell sizes achievable, 25μm – 250μm
- Bump bonding
  - Cost-driving factor on detector production
  - Limiting factor for the pixel pitch
  - Limiting factor for device thickness: stability
The CLICpix2 Prototype

- Readout ASIC to meet CLIC vertex requirements
- Timepix/Medipix chip family
  - 128 x 128 pixels (3.2 x 3.2 mm² active area)
  - 65nm CMOS, 25μm x 25μm pitch
  - Per-pixel charge and arrival time measurement
- Shutter-based acquisition
- Power pulsing of the pixel matrix
- Challenge: bump bonding of sensors with 25μm pitch
- Successfully tested in lab & test beam measurements, characterization ongoing
Monolithic High-Voltage CMOS Sensors

- Evolution of Monolithic Active Pixel Sensors (MAPS)
  - Electronics and sensor on same wafer
  - Lower mass than hybrids, no bump-bonding
  - Fully integrated: amplification & readout
- Goal: Charge collection through drift instead of diffusion
  - Fast charge collection
  - Larger depleted volume, more charge collected
- Shield electronics via deep collection diode surrounding electronics
  - Allows high voltage to be applied to substrate
- Challenges:
  - Large collection diode means large input capacitance (& increased power consumption, reduced SNR)
  - Full depletion has yet to be achieved (high resistivity substrates and backside bias)
The ATLASpix Prototype (ATLAS)

- Fully integrated chip designed for ATLAS ITk upgrade
  - Under investigation in view of CLIC tracker requirements
  - AMS 180 nm HV-CMOS process, substrates with 20-1000Ωcm
  - 25 x 400 pixels, 130μm x 40μm pixel pitch
  - Charge amplifier, discriminator in pixel, charge and arrival time measurement in periphery
- Promising results from first beam tests
- Ongoing: beam tests with improved readout system to characterize timing performance

Efficiency ~99.5%
Resolution $\sigma_{SP} \sim 13\mu m$
Monolithic High-Resistivity CMOS Sensors

- Alternative to HV-CMOS
- Electronics outside charge-collection well
  - Small collection diode reduces input capacitance
  - Form depleted region by using high-resistivity substrate
- No special HV design rules for electronics necessary
- Lower bias voltage than HV-CMOS
  - Avoid electronics shielding to compete with collection diode
- Process modifications allow full lateral depletion
  - Higher backside bias possible due to isolation of electronics by depleted region
The Investigator Prototype Chip (ALICE)

- Analog prototype – digitization off-chip
- Two different TowerJazz 180nm processes
  - Different doping profiles/depletion approaches
- For 28 x 28μm² pitch: 99.3% efficiency, $\sigma_t < 5$ns, $\sigma_{SP} \sim 4$μm
- Good spatial and time resolution at very low threshold
- Future plans:
  - Design of fully integrated chip for CLIC tracker: CLICTD
  - Low resolution interesting for CLIC vertex?
Monolithic Silicon-on-Insulator Sensors

- Monolithic sensor on single wafer with high-resistivity substrate
- Separate sensor/electronics by insulation oxide layer

- Cracow SOI test chip in 200nm LAPIS SOI process, different parameters:
  >= 30μm x 30μm pitch, single-SOI & double-SOI, different r/o schemes
- First test beam results for 500 μm thickness, 30x30 μm² pitch: Efficiency > 99%, σ_{SP} ~ 2μm
- Ongoing work:
  - Analysis of prototype test-beam data
  - Production of vertex test chip CLIPS
Capacitively Coupled Detectors

- Combination of “traditional” readout chip and HV-CMOS active sensor
- Only analog part (amplification) in sensor
- Advantages:
  - Large signal from amplifier while rather simple circuitry in HV-CMOS
  - Can use full feature set of readout chip CMOS process
  - Chips can be glued, avoids bump-bonding
- Challenges:
  - Gluing requires precise alignment
  - Main influence: distance – good uniformity required
CLICpix2 + C3PD

- Two generations of active sensors (CCPDv3, C3PD) in AMS 180 nm HV-CMOS process,
  - 10-1000Ωcm substrates, 25 x 25μm² pitch
- First test beam measurements performed
  - Efficiency > 90% , $\sigma_t \sim 7$ns, $\sigma_{SP} \sim 8$μm
- Finite-element simulation of capacitive coupling
- Ongoing work:
  - Evaluation of high-resistivity sensors for larger depletion zone
  - Glue-process optimization
Enhanced Lateral Drift Detectors

- Position resolution in thin sensors limited to pitch / √12 (almost no charge sharing)
- New sensor concept: **enhance charge sharing**
  Enhanced LAteral Drift sensors (ELAD)
  - Close to theoretical optimum: linear charge sharing
- Deep implantations to alter the electric field
  - Lateral spread of charges during drift, cluster size ~2
  - Improved resolution for same pitch
- Challenges:
  - Complex production process, adds cost
  - Have to avoid low-field regions (recombination)
- Simulations ongoing: implantation process, sensor performance
- First production in 2018: test structures, strips and test sensors with Timepix3 footprint (55μm pitch)
Prototype Simulation
Simulation of Detector Prototypes: **Allpix Squared**

- Powerful simulation tools required to understand prototypes and optimize designs
- Monte Carlo simulation complementary to device modeling like TCAD
  - Account for stochastic nature of processes: high statistics samples
  - Simulate full setup (potentially multiple detectors)
- Combine tools: **Geant4 + TCAD fields + Front-end simulation**
- Provides access to main detector characteristics (resolution, efficiency…)
- Implements drift-diffusion model to model charge flow in sensor:
- Simulation of transient effects for timing under development

Drift animations of electrons/holes through a planar silicon sensor
Verification With Test Beam Data

- **CLICdp** Timepix3 Telescope + DUT: **50μm planar sensor**
- Simulate device only with few parameters taken from data
  - Dimensions, bias/depletion voltages, temperature, threshold
  - Reconstruction with same cuts & corrections
- Very good agreement between data and simulation
In a nutshell...
Summary & Outlook

- Proposed CLIC linear e+e- collider poses challenges to silicon detectors
  - ... excellent spatial and temporal resolution, minimum material
  - ... ambitious detector design concept
- Comprehensive R&D program for CLIC silicon detectors
  - Many technologies and concepts under investigation
  - Most initial requirements shown to be achievable, 3μm resolution still to be reached
- New and validated simulation tools help R&D and prototyping
- Ongoing developments:
  - New HR-CMOS chip for tracker: CLICTD
  - New SOI chip for vertex: CLIPS
  - Production and testing of a first ELAD silicon sensor
2013 - 2019 Development Phase
Development of a Project Plan for a staged CLIC implementation in line with LHC results; technical developments with industry, performance studies for accelerator parts and systems, detector technology demonstrators.

2020 - 2025 Preparation Phase
Finalisation of implementation parameters, preparation for industrial procurement, Drive Beam Facility and other system verifications, Technical Proposal of the experiment, site authorisation.

2026 - 2034 Construction Phase
Construction of the first CLIC accelerator stage compatible with implementation of further stages; construction of the experiment; hardware commissioning.

2019 - 2020 Decisions
Update of the European Strategy for Particle Physics; decision towards a next CERN project at the energy frontier (e.g. CLIC, FCC).

2025 Construction Start
Ready for construction; start of excavations.

2035 First Beams
Getting ready for data taking by the time the LHC programme reaches completion.
CLIC Accelerator Complex

CLIC layout at 3 TeV

CLIC accelerating structure

CERN-2012-007
CLIC Detector Concept

- low-mass **vertex detector** with ~25x25 μm² pixels
- **silicon tracker**
- fine-grained PFA calorimetry, 1+7.5 Λ_{i}, W-ECAL + Fe-HCAL
- 4 T **solenoid**
- return yoke with muon ID
- Complex instrumented forward region
Experimental Conditions at CLIC

- CLIC beam structure drives design
  - Spacing between bunches: 0.5 ns
  - Trains of 312 bunches, 50 Hz repetition rate
  - Transverse beam size ~nm
- Interactions between bunches
  - Large experimental background: \( \gamma \gamma \rightarrow \text{hadrons} / \text{e+e-} \) (beamstrahlung):
    ~100 particles/BX within acceptance @ 3TeV
  - Mostly in forward direction
- **Low radiation** environment
  - Factor \( 10^4 \) lower than at LHC
The CLICdp Timepix3 Telescope

• Beam telescope with 7 Timepix3 planes
  • Operated in SPS H6, typically 120 GeV pions
  • Timepix3 assemblies: 300 μm thick, 55 μm pitch
  • Resolution on DUT: spatial ~2μm, timing ~1 ns
  • High rate, capable of > $1 \times 10^6$ Tracks/spill
• x/y linear movement + rotation stage for the DUT
• 3 scintillator triggers in coincidence (for DUT)
• Motion stage for the full telescope, allows to operate parasitically to other users in the same beam line
HR-CMOS: Standard/Modified Process

Standard, in-pixel total cluster size:

Modified, in-pixel total cluster size:
Performance of Thin Planar Sensors

- Test beam studies: performance of thin sensors
  - CLIC Timepix3 telescope for reference, 2 μm resolution
  - Timepix/Timepix3 ASICs, 55 μm pitch

- High detection efficiency even for 50 μm sensor @ normal operating conditions
- Resolution limited by charge sharing / cluster size

Micron/IZM: 100 μm sensor on 100 μm Timepix

CLICdp work in progress
Caribou – Multi-chip modular DAQ system

- Variety of DAQ systems for pixel detector prototypes
  - Requirements very similar
  - Not very innovative from functional point of view
  - Repeated integration effort into (test beam) DAQ

- Solution: versatile, modular readout system
  - Collective effort for maintenance and extension
  - Support for wide range of current & future prototypes
  - Suited for laboratory and test beam measurements
Caribou – Multi-chip modular DAQ system

Xilinx ZC-706 + (optional) FMC + interface board + chip board

- Zynq System-on-Chip platform: FPGA + ARM Cortex A9 + …
  - Run Linux OS + DAQ software directly on the board
  - Access through network (1/10 Gbit ETH/SFP+)
  - SoC also contains (hardware) periphery: I2C, SPI modules, ...
- FMC cable allows to place main board in safe distance to beam
Caribou – The CaR interface board

- FMC mezzanine board
- Hosts: power supplies, ADCs, current/voltage regulators, clock generator, pulse injectors, SERDES links
- RJ45 connector to interface TLU
- SEAF connector to chip board
- Designed for re-usability: contains all functionality & all expensive components
Caribou – Application-specific chip board

- Board with minimum functionality
  - Routing between SEAF connector and front-end
  - Special buffers (LVDS-CML …)
- Low production cost, simple design
Caribou – System-on-chip layout

Periphery
- I2C
- SPI
- ETH
- SD Card
- ...

ARM Cortex A9

“peary” distribution

Custom Linux drivers
peary DAQ software

AXI4 Interface

FPGA

Registers
DMA

SerDes receivers
Custom components
...

Memory Controller

DDR RAM

DDRAM

Memory Controller

Front-end chip

application specific
Caribou – Software architecture

- kernel drivers
- system
- DAQ library
- user space

- caribouHAL
- caribouDeviceMgr
- caribouDevice
- CLICpix2
- C3PD
- ... Configuration, Logging etc.

- DAQ Client
- Lab Testing
- CLI

- caribouHAL
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- ... Configuration, Logging etc.
The Allpix Squared Framework

- Written in modern C++
- Prov. central components
  - Convenient user interface
  - Logging, configuration
  - Geometry and transformations
- Implement physics in independent modules
  - Plug & play concept
  - IO using ROOT TTrees
- Loading lib, parallelization...
Detector Models

- Different detector types available
  - Monolithic detectors
  - Hybrid detectors w/ bump bonds
- Easy configuration through model files
  - Give it a name, decide on the type
  - Set detector parameters
- Some model files already shipped with the framework, at the moment:

  ATLAS FE-I3, FE-I4, CMS PSI46/dig, Medipix3, Timepix3, CLICpix, CLICpix2, Mimosa23, Mimosa26

```python
1  type = "hybrid"
2  number_of_pixels = 256 256
3  pixel_size = 55um 55um
4  sensor_thickness = 300um
5  chip_thickness = 700um
6  # ...
7  [support]
8  thickness = 1.76mm
```
Documentation & Manuals

- Extensive User Manual ~115 pages (PDF/TeX)

- Well-documented code (Doxygen)

- Module documentation (Markdown)
Active-Edge Sensors: Guard Ring Layouts

- Different guard ring layouts implemented
  - No guard rings, floating guard rings
  - Grounded guard rings, via additional row of bump bonds
- Edge distance: distance between last n-implant and cut edge

**No Guard Rings**

**Floating Guard Ring**

**Grounded Guard Ring**

![Diagram](image)
Edge Performance

- Test beam studies of sensor performance at the edge
  - CLIC Timepix3 telescope for reference, 2μm track resolution
  - Timepix3 with active-edge sensors as DUT

- Tracks from edge folded into 2x2 pixel matrix
  - Increase statistics
  - End of pixel matrix: dashed line
  - Physical cutting edge of sensor: solid line
Active-Edge Sensor, 50μm thickness

- Without GR and with floating GR: fully efficient up to the physical sensor edge
- With grounded GR: signal/efficiency loss
Active-Edge Sensors: TCAD Simulations

- Different guard ring layouts in Synopsys Sentaurus
- 2D simulation at implant center, 50μm thick, edge distance 20μm

- Field lines end at pixel
- No charge loss expected
- Most field lines at pixel
- Small charge loss
- Some lines end on ground ring
- Significant charge loss