Frontier Detectors for Frontier Physics

14th Pisa Meeting on Advanced Detectors

May 27 – June 2 2018 ● La Biodola, Isola d'Elba (Italy)

The Belle II Vertex Detector Integration

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Solid State Detectors - Poster Session, Tuesday, 29 May 2018, 09:00 - 12:50
Christian Wessel*:*
DEPFET Pixel Detector Situated on Belle II Experiment.

Richard Thalmeier*:*
The Belle II Silicon Vertex Detector

Lorenzo Vitale
First experience with the Belle II radiation monitoring based on diamonds

Belle II

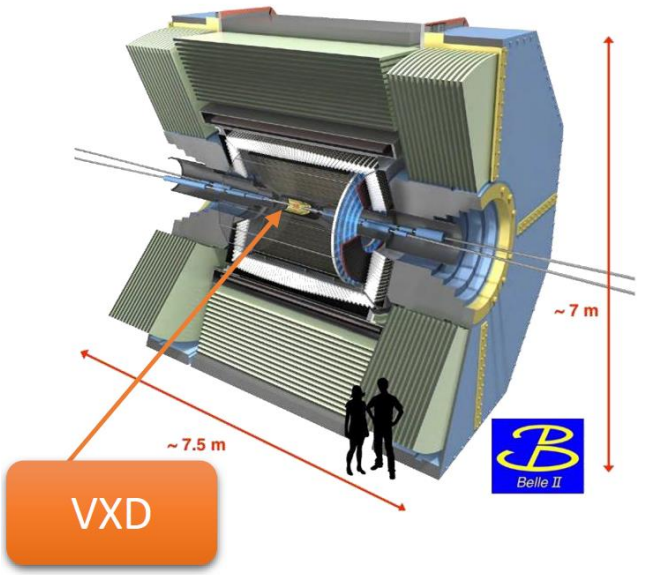
Belle II – a particle physics experiment at the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan.

SuperKEKB accelerator, an asymmetric-energy e^+e^- (4 on 7 GeV) collider with design luminosity 8×10^{35} $cm^{-2}s^{-1}$

The radiation dose expected in the inner region of the detector is around 20 kGy/yr.

The experiment requires excellent vertexing and low-p_T tracking performance.

Expected to take its first physics data with full detector in early 2019.

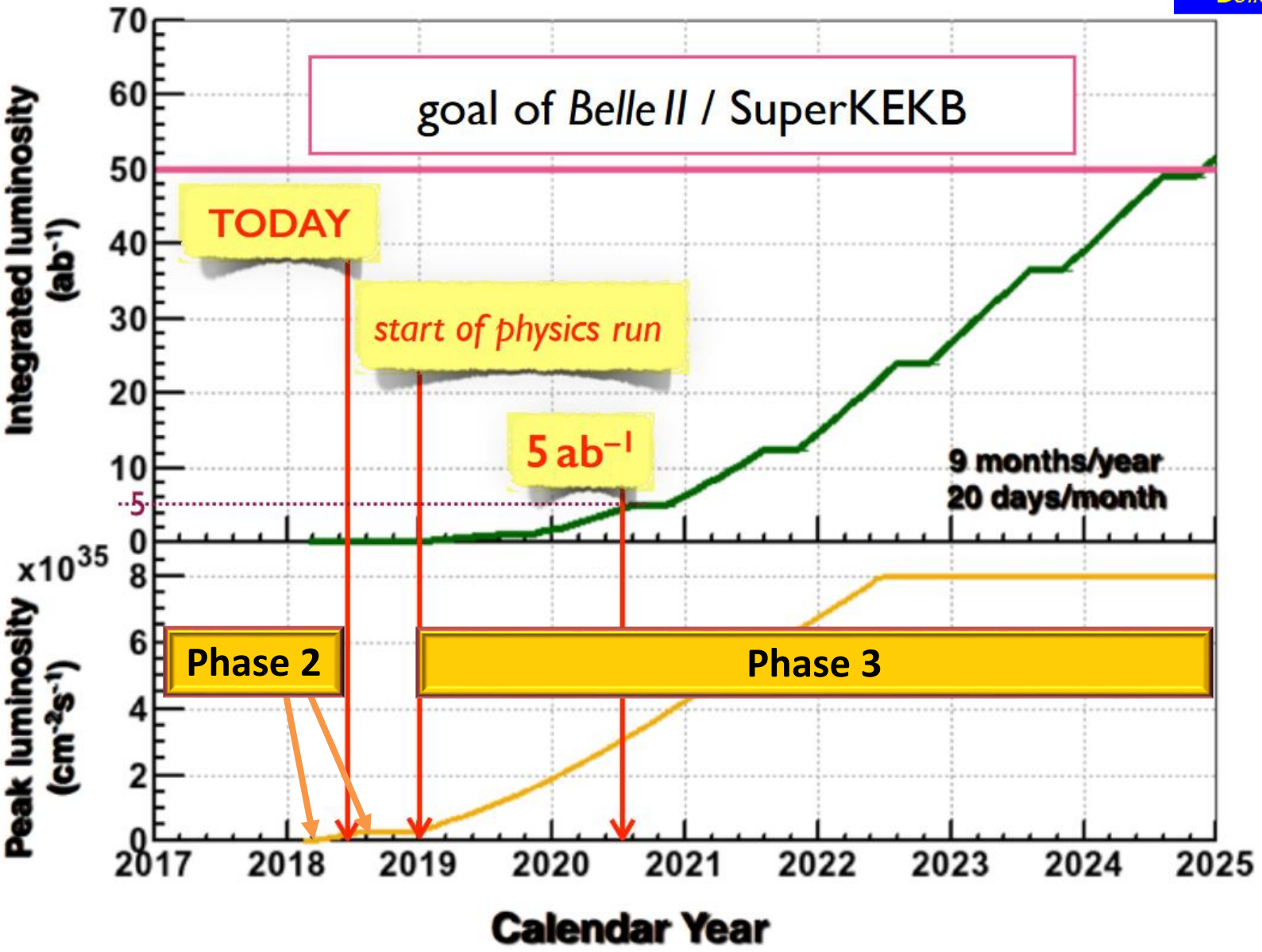


Commissioning of Belle II vertex (VXD) detector:

Phase 2: subset of the vertex detector, comprising six layers with a single ladder per layer
installation at February 2018, first collisions measurement at April 25, 2018,
end of Phase 2: mid of July, 2018
GOALS: a) commissioning of the final interaction region
b) measure beam background for safe installation of the full VXD in Phase 3
c) acquire first collisions

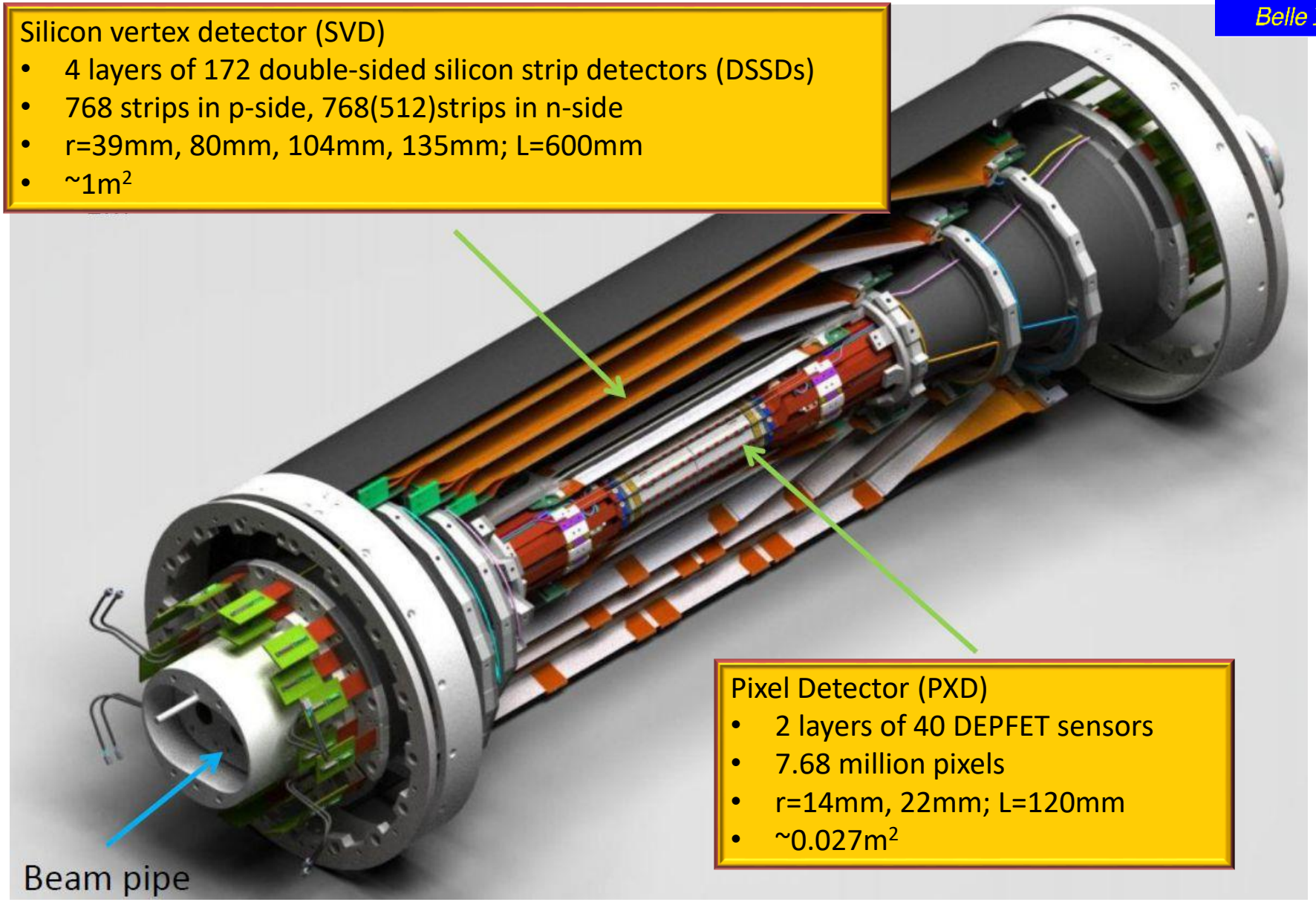
Phase 3: installation and integration of the full 6-layer VXD by the end of 2018

Belle II


goal of Belle II / SuperKEKB
TODAY
start of physics run
5 ab⁻¹
9 months/year
20 days/month
Integrated luminosity (ab⁻¹)
Peak luminosity (cm⁻²s⁻¹)
x10³⁵
Phase 2
Phase 3
Calendar Year
2017
2018
2019
2020
2021
2022
2023
2024
2025

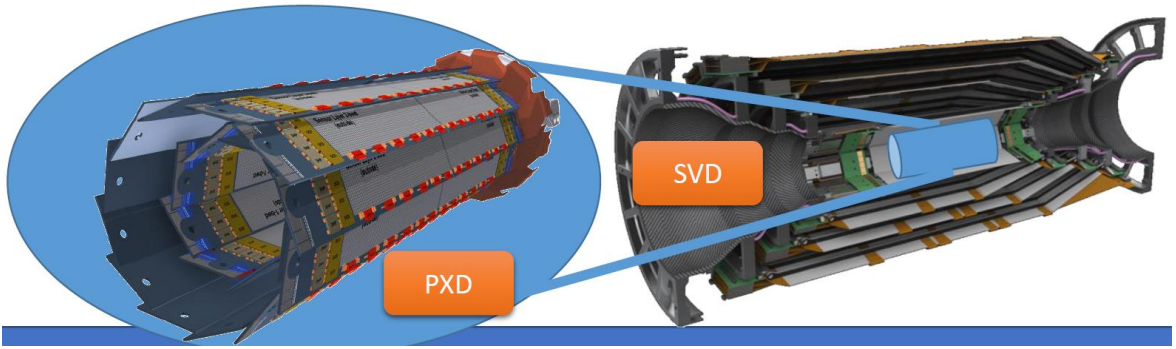
The Belle II vertex detector

Silicon vertex detector (SVD)
- 4 layers of 172 double-sided silicon strip detectors (DSSDs)
- 768 strips in p-side, 768(512)strips in n-side
- r=39mm, 80mm, 104mm, 135mm; L=600mm
- ~1m^2

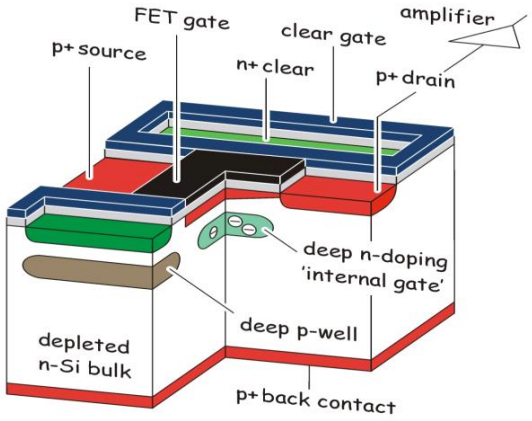


Pixel Detector (PXD)
- 2 layers of 40 DEPFET sensors
- 7.68 million pixels
- r=14mm, 22mm; L=120mm
- ~0.027m^2

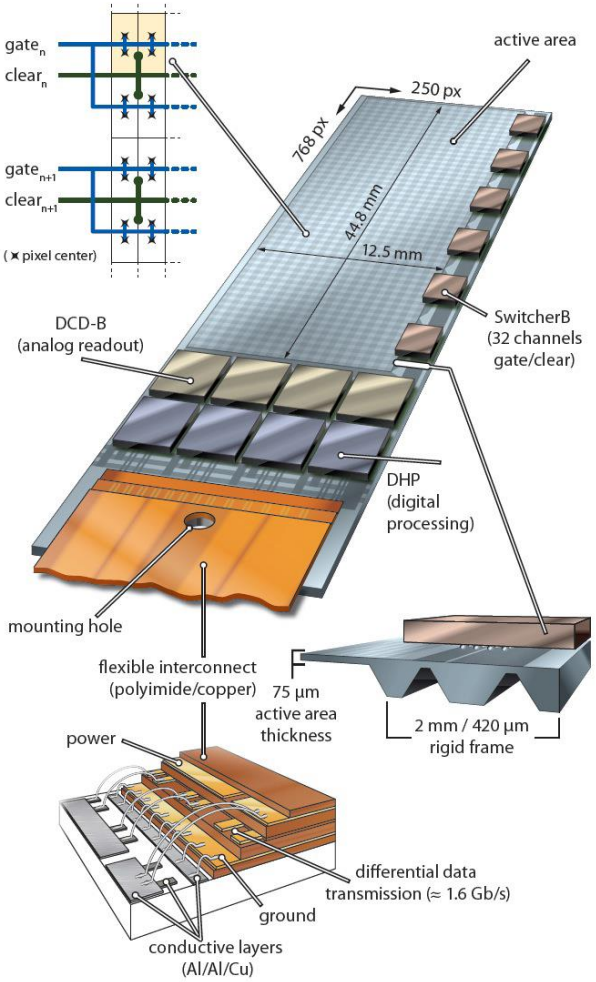
PXD – DEPFET sensor and readout



The DEPFET technology of active pixel sensors is among the frontier detector concepts for high energy physics at high luminosities.



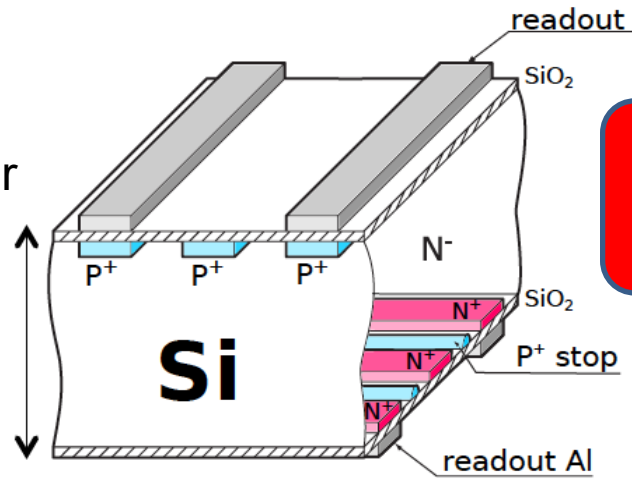
Belle II PXD produces 180 GB/s of raw data:
40 PXD half ladders with 250 × 768 pixels each and 7.6×10^6 pixels in total, expected occupancy up to 3%, trigger rate of 30 kHz.
Data volume reduced by a factor of 10.



PXD more details: Poster session Christian Wessel

SVD sensor and readout

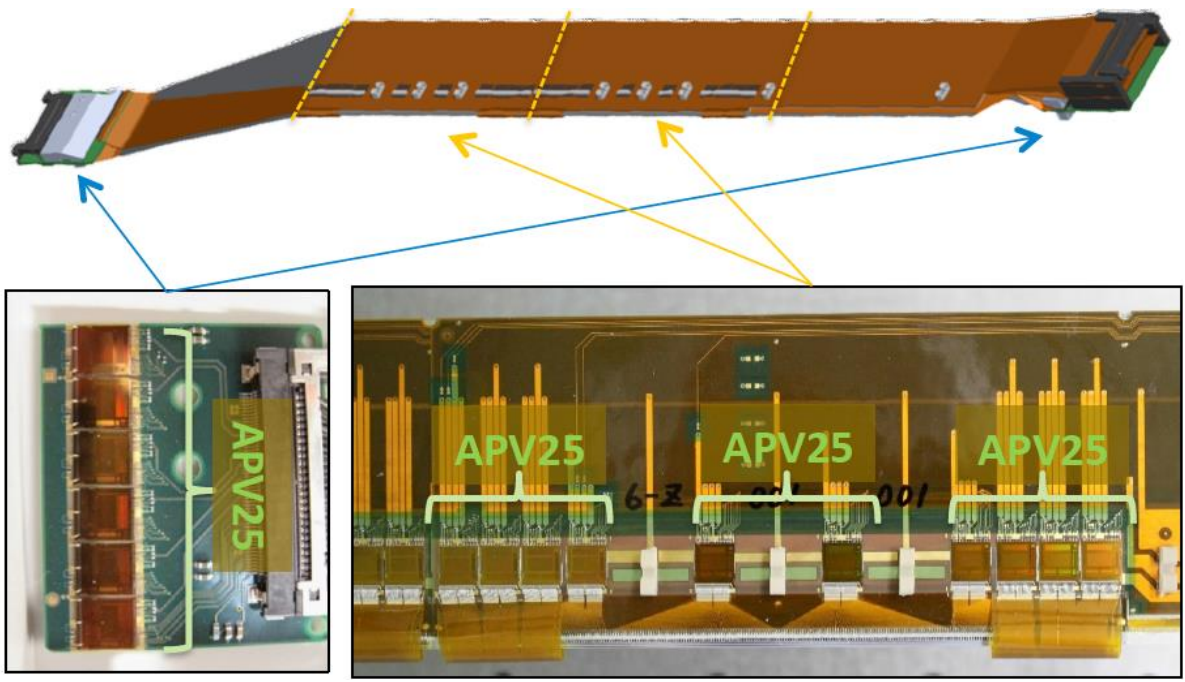
300-320 microns thick double-sided silicon microstrip detector (DSSD): p-in-n 6′ wafer



SVD more details: Poster session Richard Thalmeier

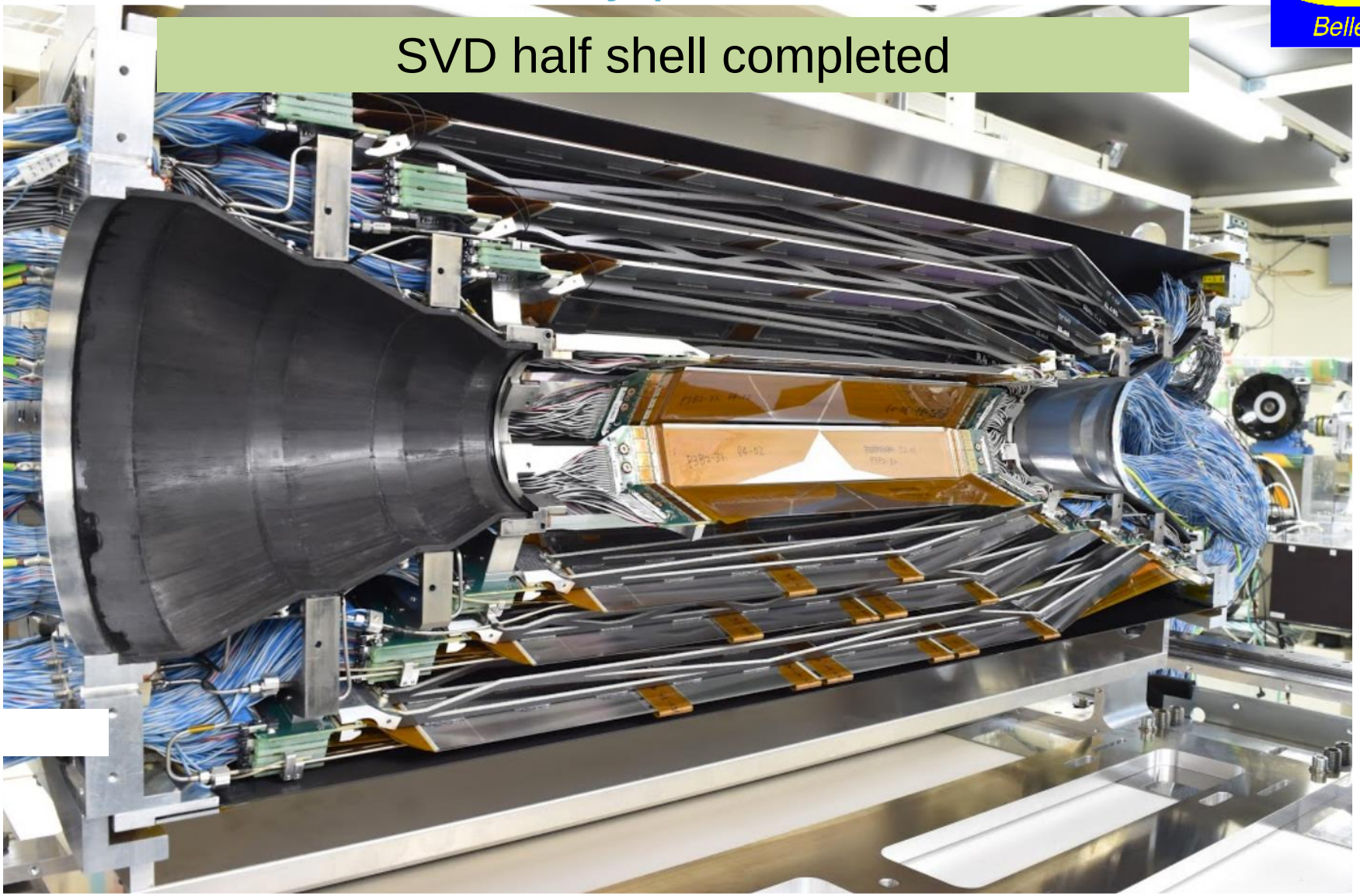
APV25 chip: originally developed for CMS.

- Shaping time: 50 ns
- # input channels: 128 per chip
- 192 cells deep analog pipeline for dead time reduction
- Thinned down to 100μm to minimize material budget
- Central DSSDs ➔ ‘Origami’ chip-on-sensor design to reduce capacitive noise



PXD – final assembly phases of Belle II

SVD – final assembly phases of Belle II



Final VXD commissioning and start of installation expected at end of October 2018

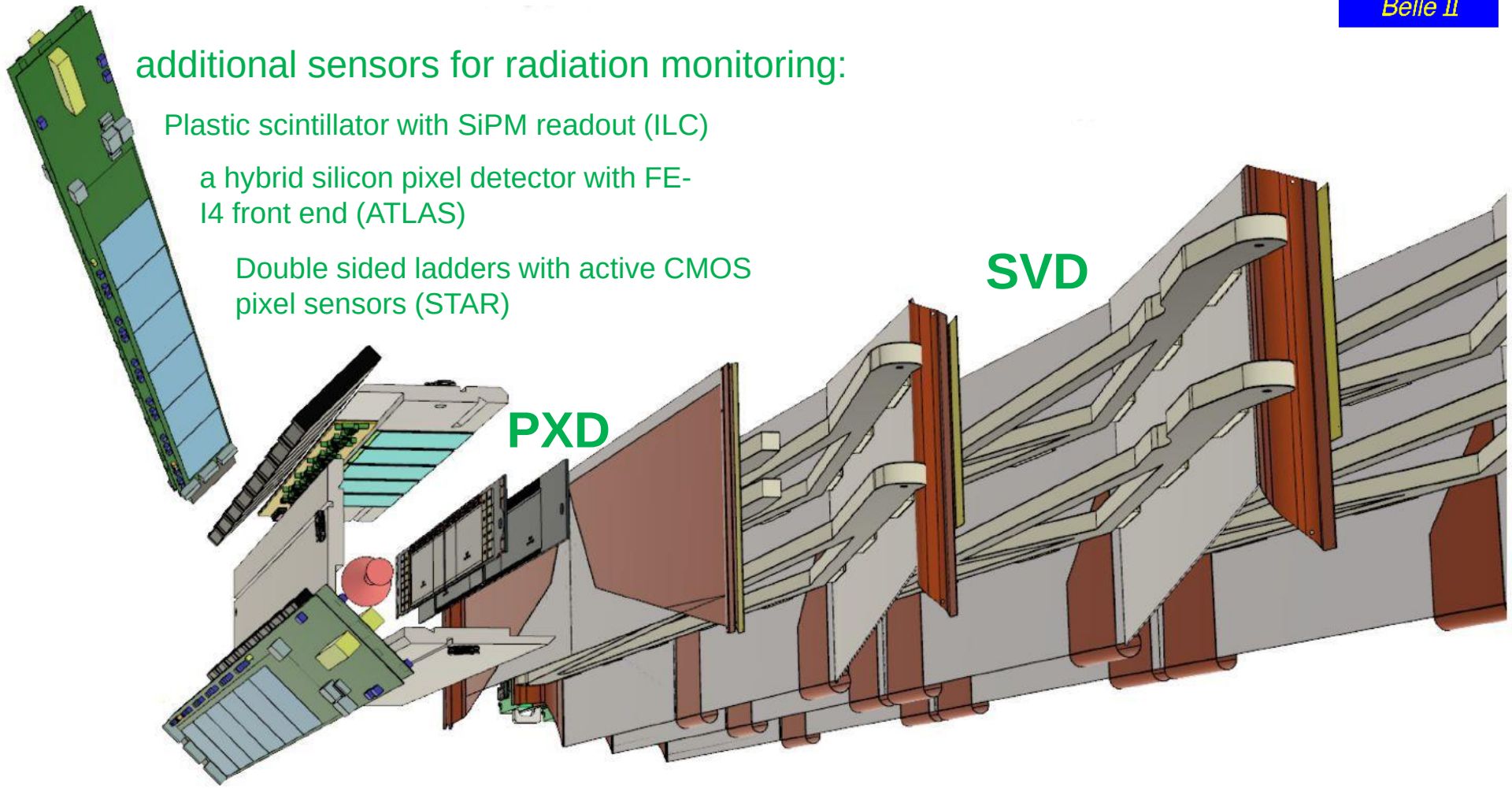
Phase 2 VXD (Feb-Jul 2018, cosmic ray + collisions)

additional sensors for radiation monitoring:

Plastic scintillator with SiPM readout (ILC)

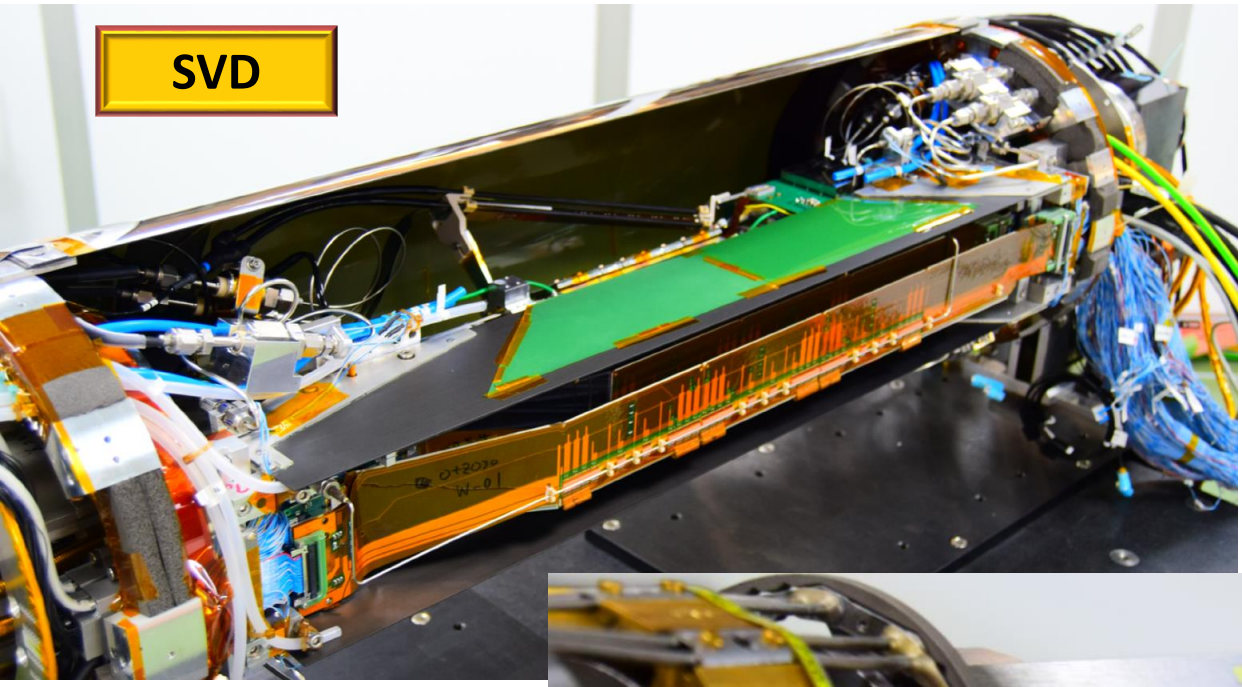
a hybrid silicon pixel detector with FE-I4 front end (ATLAS)

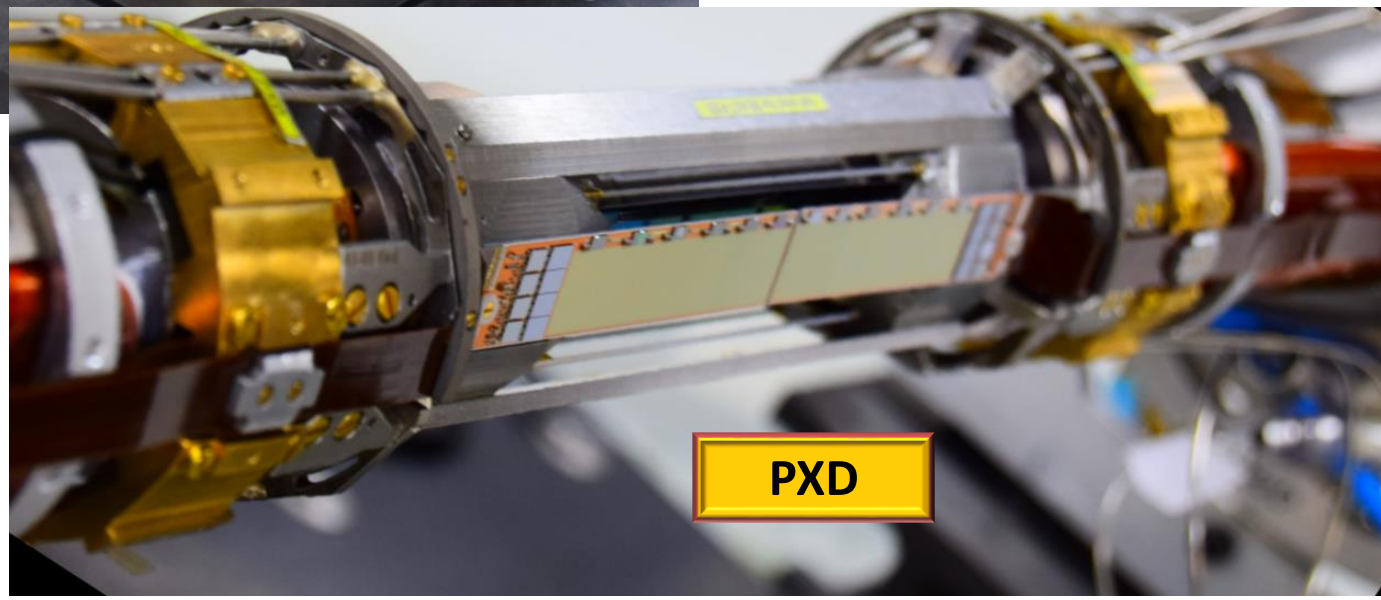
Double sided ladders with active CMOS pixel sensors (STAR)



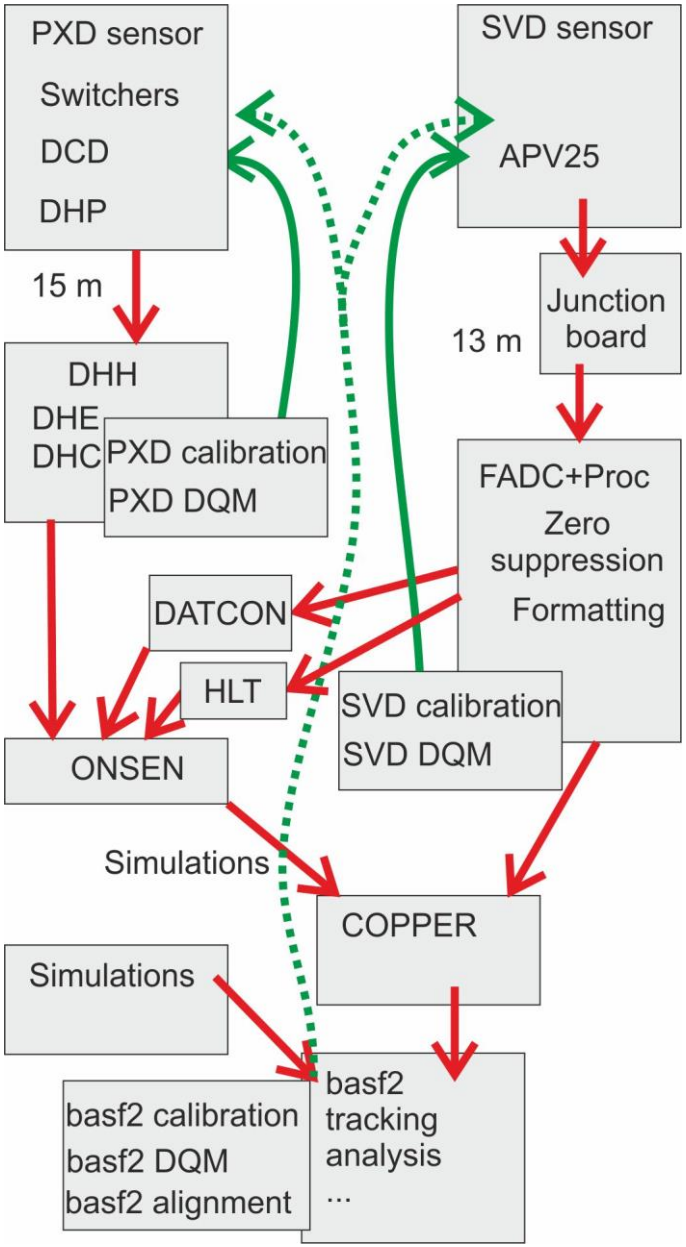
Schematic view of the Belle II Phase 2 VXD.
The six VXD layers have the geometry of the full VXD, except they comprise only a single ladder per layer in the horizontal plane for beam background and occupancy studies

Phase 2 VXD Photo:





VXD data acquisition chain



Switcher – controller of voltages and time manager

DCD – Drain Current Digitizer

DHP – Data Handling Processor, TSMC version

DHH – Data handling Hub

DHE – Data Handling Engine

DHC – Data Handling Concentrator

PXD more details: Poster session Christian Wessel

ONSEN – Online Selection Nodes real-time data-processing system

APV25 – front-end readout chip

FADC – Flash Analog-to-Digital Converter and Processing modules

DATCON – Data Acquisition Tracking Concentrator Online Node

HLT – High Level Trigger

SVD more details: Poster session Richard Thalmeier

COPPER – COmmon Pipelined Platform for Electronics Readout

DQM – Data Quality Monitor

PXD performance in Phase 2

Highlights from first data taking

Detector performance is up to design requirements and better

MPV ~6.35 ke$^-$ on 75 microns thick silicon sensor

Cluster size 2 and more dominate and give better position estimation.

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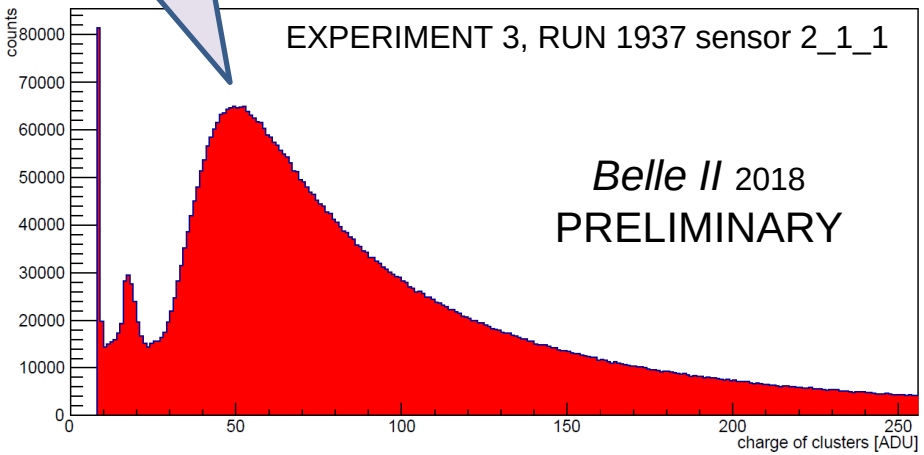
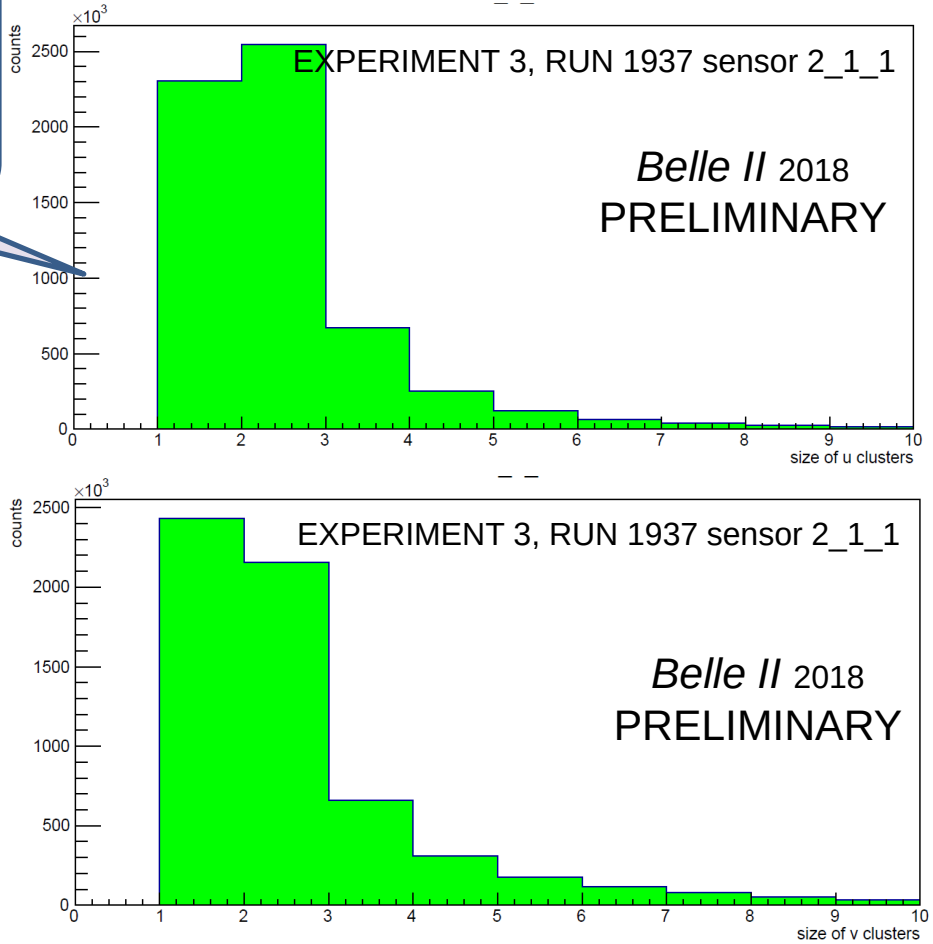


Cluster charge in ADU for all clusters
1 ADU ~ 122 e$^-$

Cluster size in u (top) and v (bottom) for all clusters



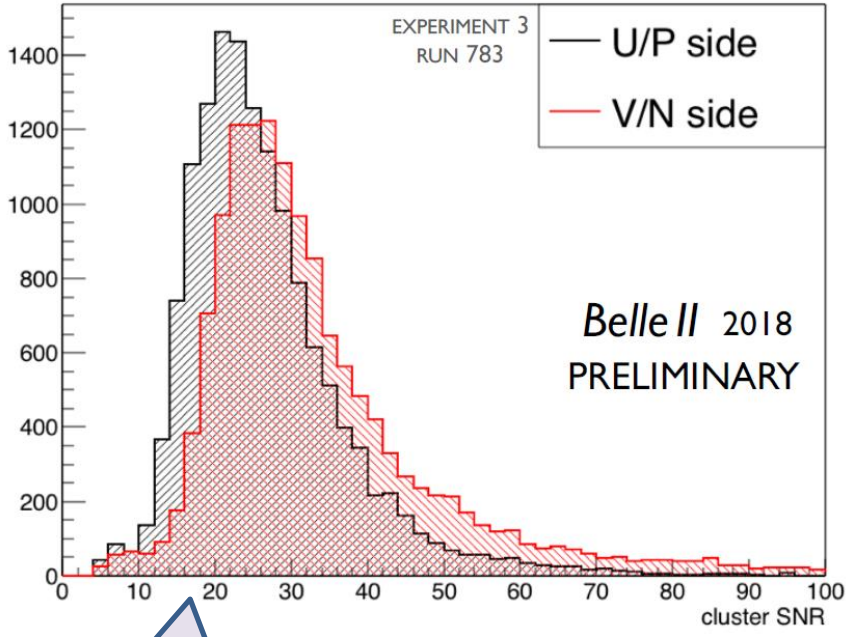
SVD performance in Phase 2

Highlights from first data taking

Detector performance is up to design requirements and better

A precise hit time determination is crucial to remove off-time hits and improve tracking performances.

tracks of different momentum and inclination matches design expectations

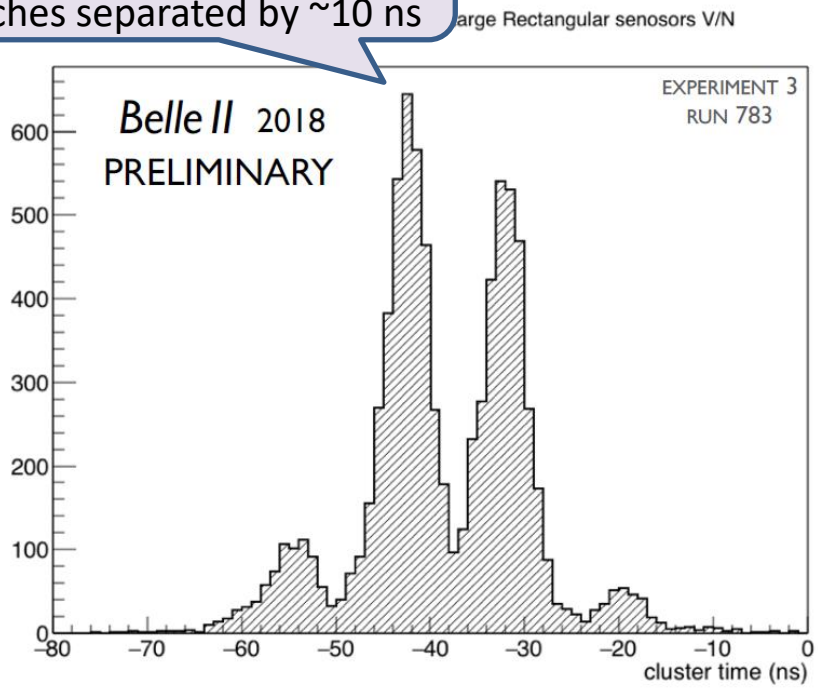


Signal-to-noise ratio 23 and higher

Cluster S/N Ratio Distribution for Clusters Related to Tracks

The filling pattern of the machine with different bunches separated by ~10 ns

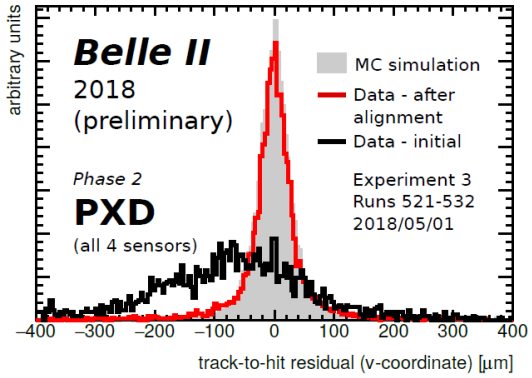
Cluster Time Distribution for Clusters Related to Tracks

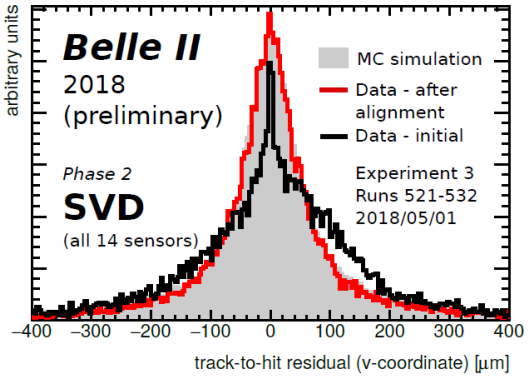


resolution of a few ns, approaching design values

VXD Alignment in Phase 2

Highlights from first data taking





In local coordinate v

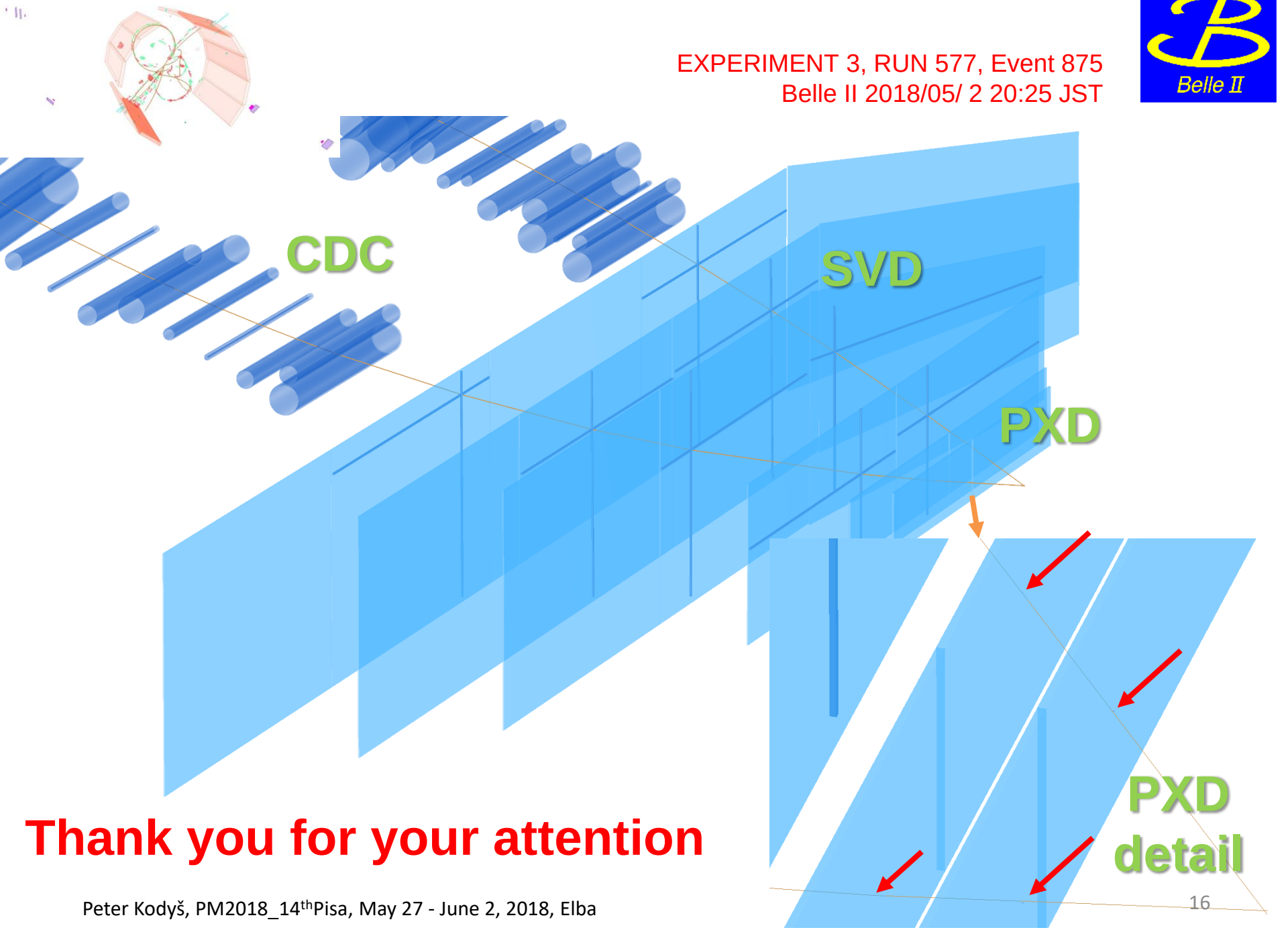
Track-to-hit residuals
sensors simulation (gray),
real data (red) and real data before alignment (black)

- The mechanical precision of installation cannot be made better than hundreds of microns, so the precise position of detector parts has to be estimated from particle tracks.
- VXD alignment employs the Millepede II algorithm and General Broken Lines track re-fit and is fully integrated in the Belle II basf2 software framework.
- Phase 2: after cosmic pre-alignment all reconstructed charged tracks with at least four VXD hits are used, 108 parameters are determined (18 sensors x 6 rigid body parameters).

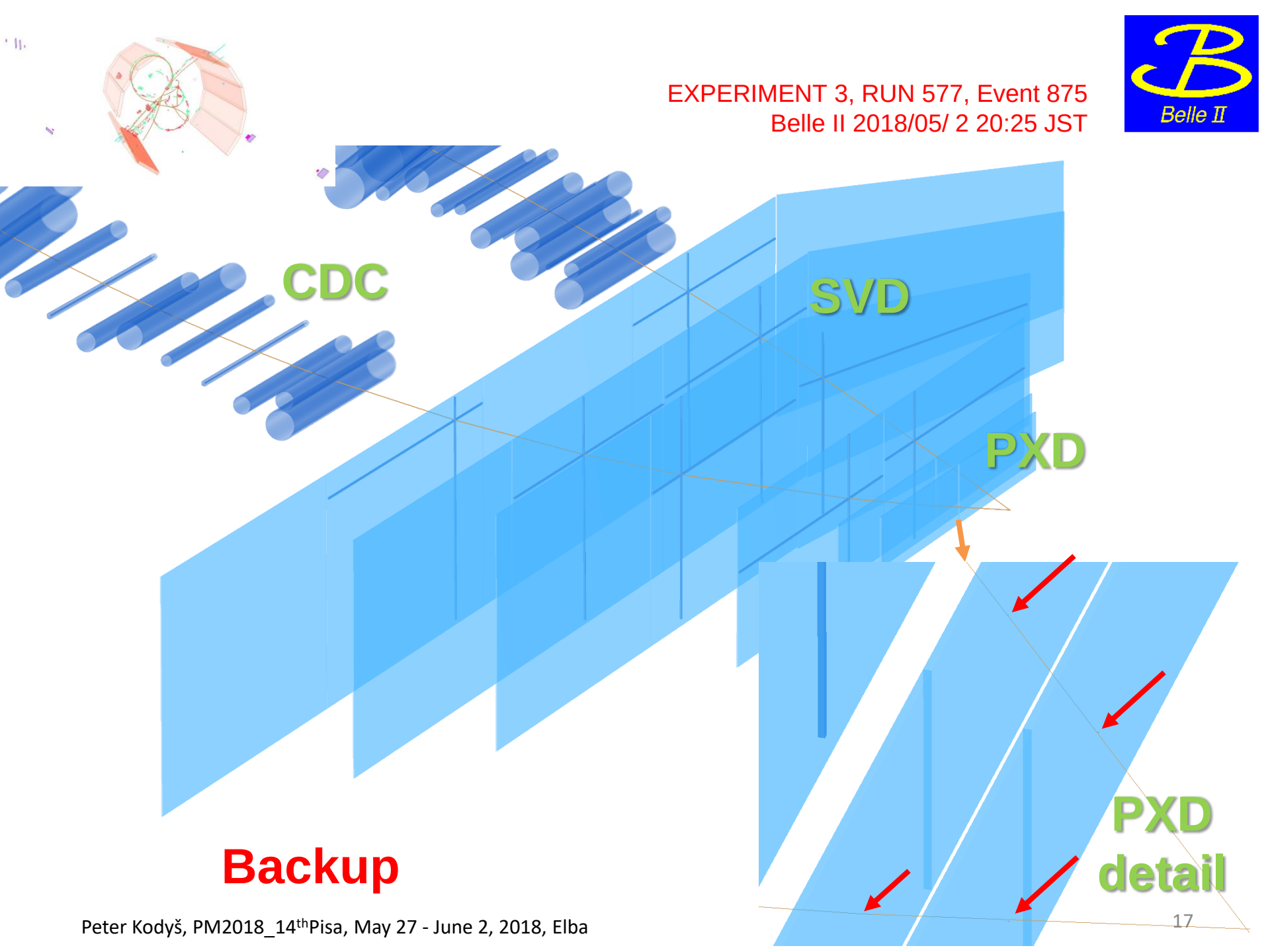
- Phase 2 VXD has a smaller number of sensors, therefore we need to use tracking from cosmic and tracking with PXD, SVD and the Central Drift Chamber (CDC) is used as a fixed reference
- The alignment integrated in the Belle II basf2 software framework is ready for work with real data.

Conclusions

- Commissioning of a subset of the vertex detector, Phase 2 VXD, comprising six layers with a single ladder per layer.
- Detector performance is up to design requirements and better.
- **First physics collisions were successfully recorded with Phase 2 Belle II detector in April 25, 2018.**
- Detectors are read out in final data chain design.
- Full data chain is well understood and realistically simulated in software
- Data quality monitors for PXD, SVD and the whole VXD are being optimized and have so far been working well.
- Alignment procedure is well integrated in the data processing chain and real data residuals are in agreement with simulations.
- Final installation and integration of the full Belle II VXD by the end of 2018 seems realistic.
- First physics data are expected early in 2019.



Thank you for your attention


EXPERIMENT 3, RUN 577, Event 875
Belle II 2018/05/ 2 20:25 JST
Belle II
CDC
SVD
PXD
PXD
detail

Backup

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The Belle II Vertex Detector Integration.

H. Aihara[q], T. Aziz[t], S. Bacher[u], S. Bahinipati[d], E. Barberio[a], Ti. Baroncelli[a], To. Baroncelli[a], A. K. Basith[e], G. Batignani[j,k], A. Bauer[b], P. K. Behera[e], V. Bertacchi[j,k], S. Bettarini[j,k], B. Bhuyan[f], T. Bilka[c], F. Bosi[k], L. Bosisio[l,m], A. Bozek[u], F. Buchsteiner[b], G. Caria[a], G. Casarosa[j,k], M. Ceccanti[k], D. Červenkov[c], T. Czank[p], N. Dash[d], M. De Nuccio[j,k], Z. Doležal[c], F. Forti[j,k], M. Friedl[b], B. Gobbo[m], J. A. M. Grimaldo[q], K. Hara[r], T. Higuchi[n], C. Irmler[b], A. Ishikawa[p], H. B. Jeon[s], C. Joo[n], M. Kaleta[u], J. Kandra[c], N. Kambara[r], K. H. Kang[s], P. Kodyš[c], T. Kohriki[r], S. Koike[C,r], I. Komarov[m], M. Kumar[g], R. Kumar[h], W. Kun[q], P. Kvasnička[c], C. La Licata[l,m], K. Lalwani[g], L. Lanceri[l,m], J. Y. Lee[t], S. C. Lee[s], J. Libby[e], T. Lueck[j,k], P. Mammini[k], A. Martini[j,k], S. N. Mayekar[i], G. B. Mohanty[i], T. Morii[n], K. R. Nakamura[r], Z. Natkaniec[u], Y. Onuki[q], W. Ostrowicz[u], A. Paladino[n], E. Paoloni[j,k], H. Park[s], K. Prasanth[i], A. Profeti[k], I. Rashevskaya[A,m], K. K. Rao[i], G. Rizzo[j,k], Resmi P. K.[e], M. Rozanska[u], D. Sahoo[i], J. Sasaki[q], N. Sato[r], S. Schultschik[b], C. Schwanda[b], J. Stypula[u], J. Suzuki[r], S. Tanaka[r], H. Tanigawa[q], G. N. Taylor[a], R. Thalmeier[b], T. Tsuboyama[r], P. Urquijo[a], L. Vitale[l,m], S. Watanuki[p], M. Watanabe[C,o], I. J. Watson[q], J. Webb[a], J. Wiechczynski[u], S. Williams[a], H. Yin[b], L. Zani[j,k],

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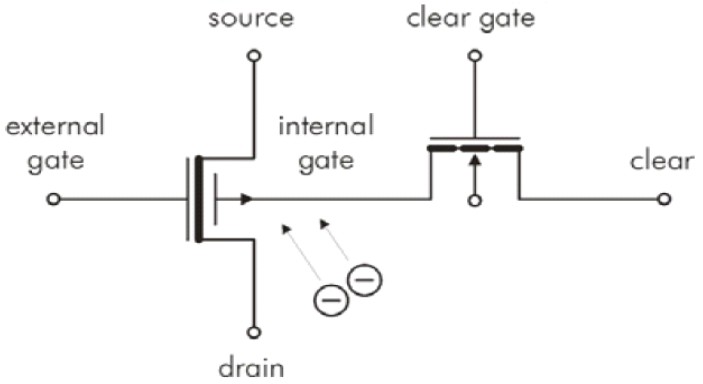
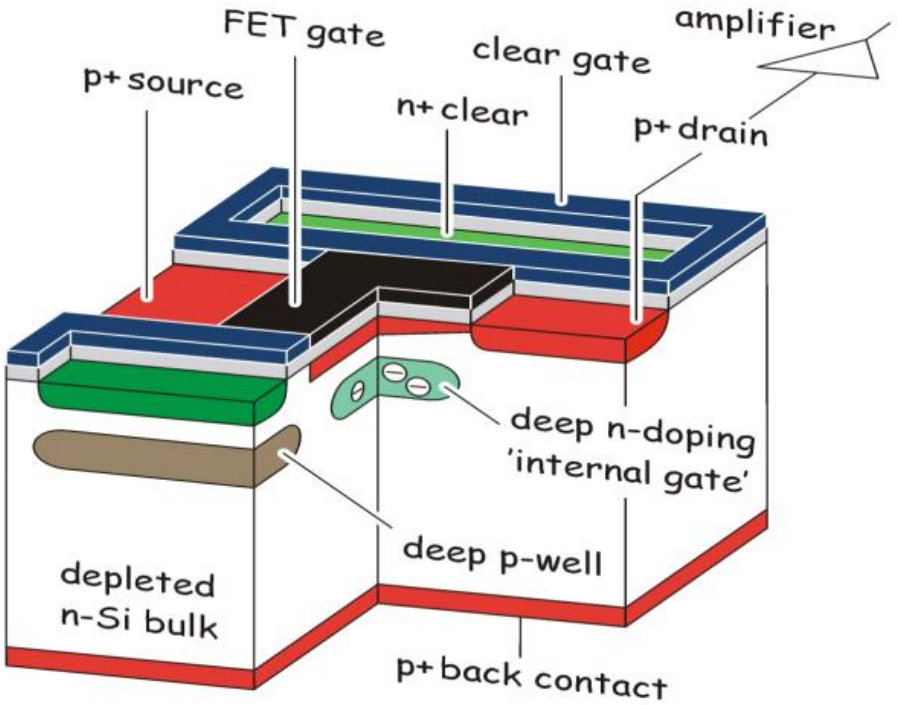
DEPFET sensors at Belle II

Spatial point resolutions below 10 μm are expected.

A unique gated data acquisition mode allows to suspend data readout for time periods with high noise occupancy; over this period, acquired charge is frozen and kept for later readout.

The front end electronics and the data acquisition schemes supporting the integration into Belle II are finalized and the two-layer pixel vertex detector (PXD) will be ready for data acquisition from its 7.6 million pixels in 2015.

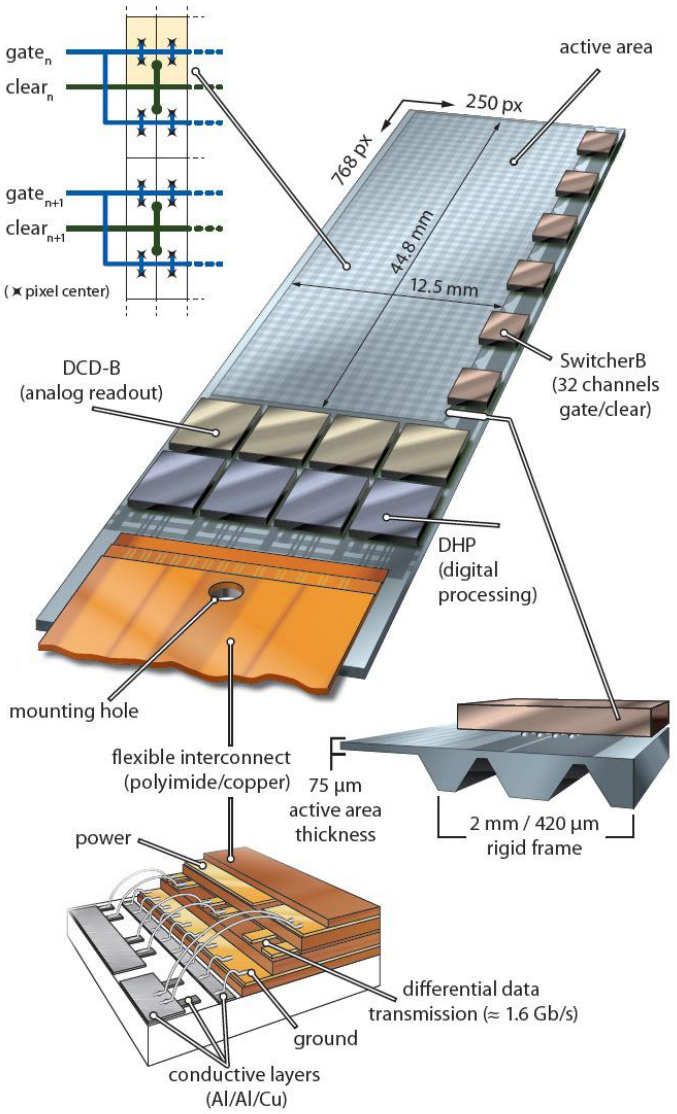




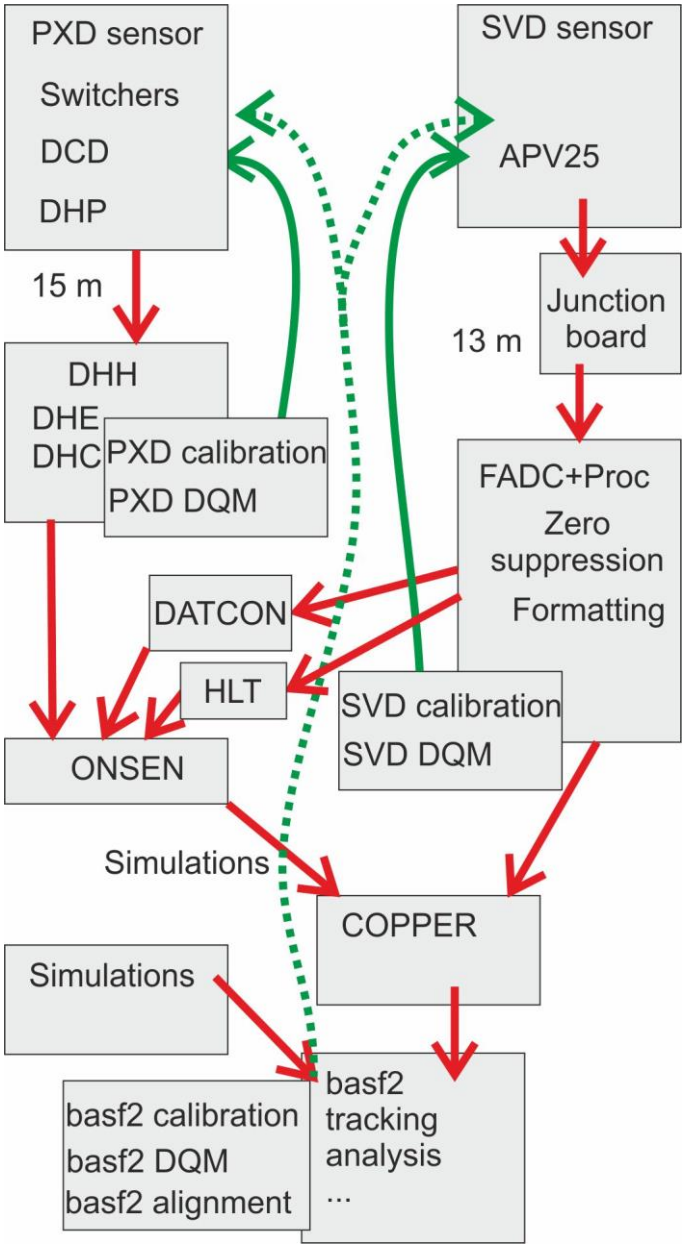
DEPFET data acquisition

Belle II PXD produces 180 GB/s of raw data:
40 PXD half ladders with 250 x 768 pixels each and 8 x 10^6 pixels in total, expected occupancy up to 3 %, trigger rate of 30 kHz.
Data volume reduced by a factor of 10.

PXD module readout: Gate and Clear Switchers organize the readout sequence, DCD (Drain Current Digitizer) are readout chips and A/D converters, DHP (Digital Handling Processor) chips provide first-stage pre-processing and data reduction (pedestals, CMN correction, zero suppression, compression algorithm). From DHP to DHH (Data Handling Hybrid) 15 m line: kapton converted to twisted-pair in a passive patch panel, DHHs via optical links to ATCA Compute Nodes, ATCA CNs reduce data based on triggers, ATCA CNs compute fast tracking using SVD data to quickly identify regions of interest in the PXD.



VXD data acquisition



- Gated Mode
- DCDs and DHPs are mounted on sensor ladders
- DHH – data acquisition, data reduction, clock, trigger and slow control commands distribution
- DHH – local data quality monitor of PXD, calibration constants
- ONSEN system filter and combine data to event builder. Possible buffering there is up to 2.5 seconds
- SVD double-sided silicon microstrip sensor readout by APV25
- Shaping time 50 ns and 6 samples per trigger
- FADC – zero suppression, data formatting
- High Level Trigger (HLT) + Data Acquisition Tracking Concentrator Online Node
- (DATCON) build event
- Create track candidates and PXD ROIs
- FADC – local SVD data quality monitor and calibrations
- COPPER board build final event and send to basf2 framework