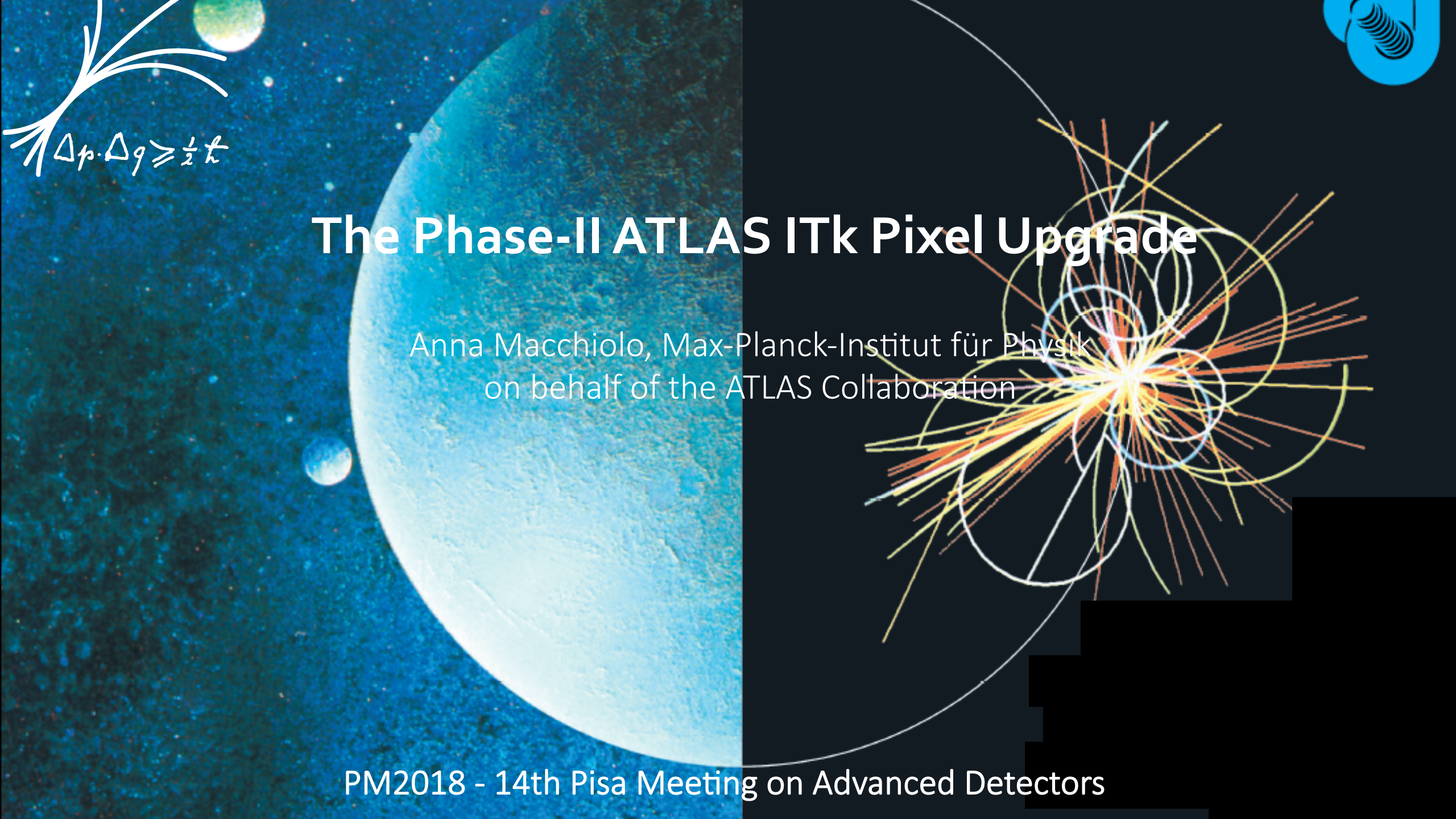
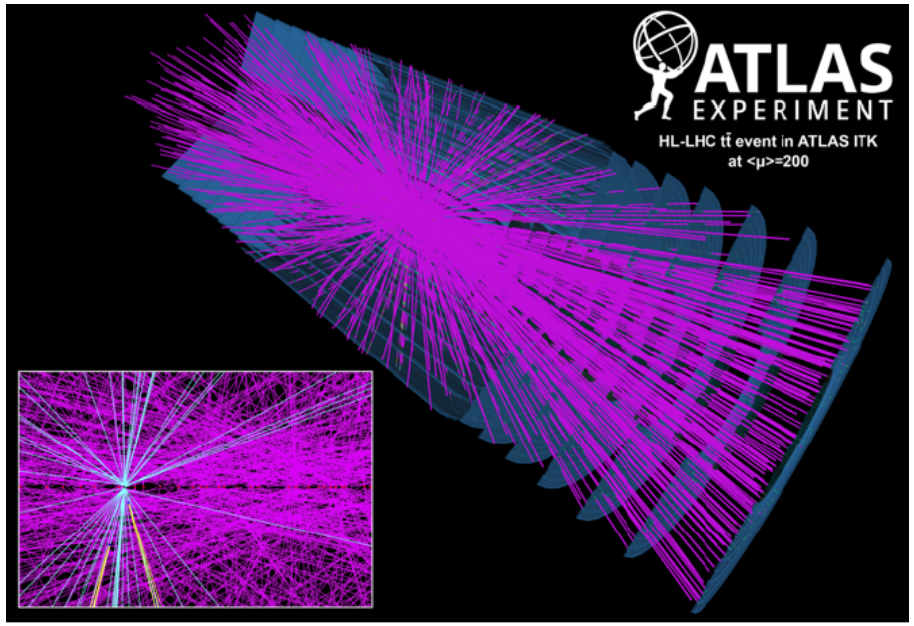


The Phase-II ATLAS ITk Pixel Upgrade

Anna Macchiolo, Max-Planck-Institut für Physik
on behalf of the ATLAS Collaboration

PM2018 - 14th Pisa Meeting on Advanced Detectors

Why a new Inner Tracker (ITk) for ATLAS?



- HL-LHC instantaneous luminosity up to 7.5×10^{34} cm^{-2} s^{-1},
- up to 200 interactions / 25 ns bunch crossing
  → Higher track density

- ID (ATLAS Inner Detector) -TRT would have 100% occupancy
- ID readout links would be saturated

A replacement of the present detector is by far not enough!

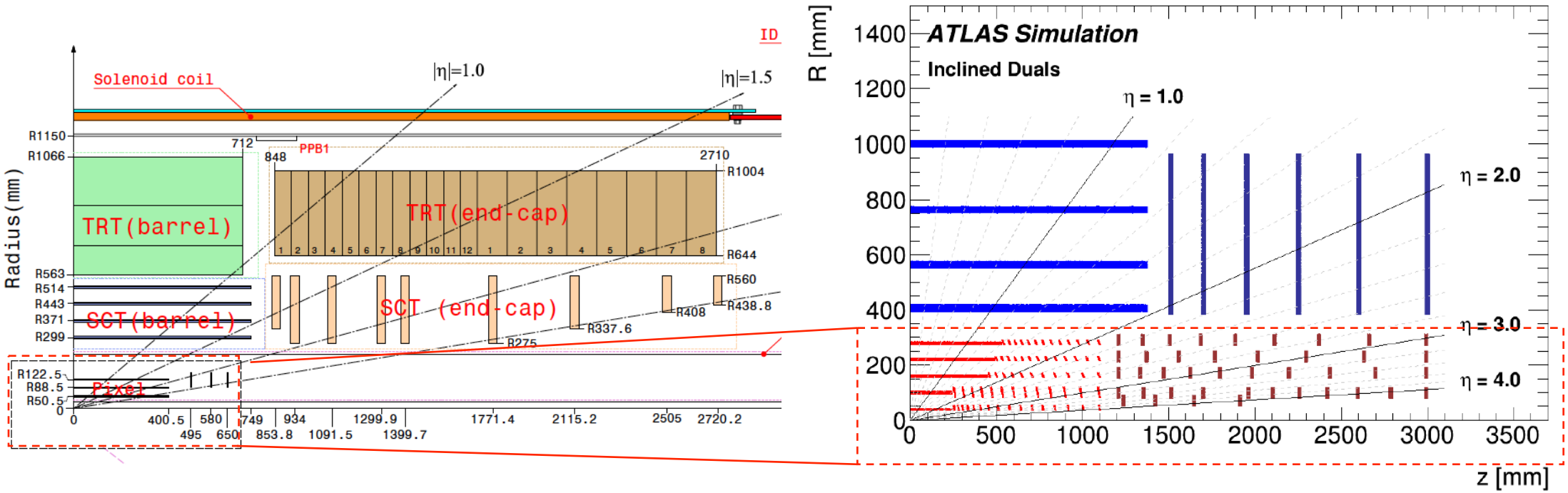
- Goal: Maintain occupancy at ≈ ‰ level (pixel), and increase spatial resolution
  - Higher granularity to keep occupancies low: 50x50 or 25x100 μm^2 pixels
  - Larger readout bandwidth capabilities

Ultimate integrated luminosity ~ 4000 fb^{-1}

Non-ionizing energy loss (NIEL) in the innermost layer: $\Phi_{eq} \approx \sim(2.5\text{-}3) \times 10^{16}$ cm^{-2}

- Replace once the two ITk innermost layers

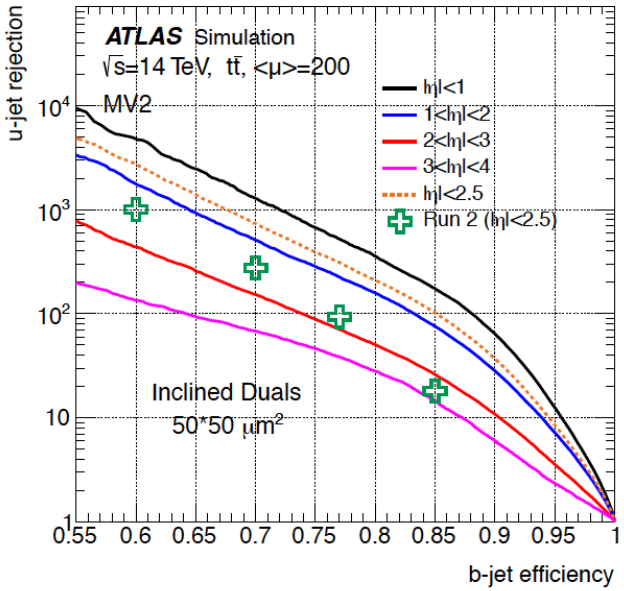
The ITk Layout

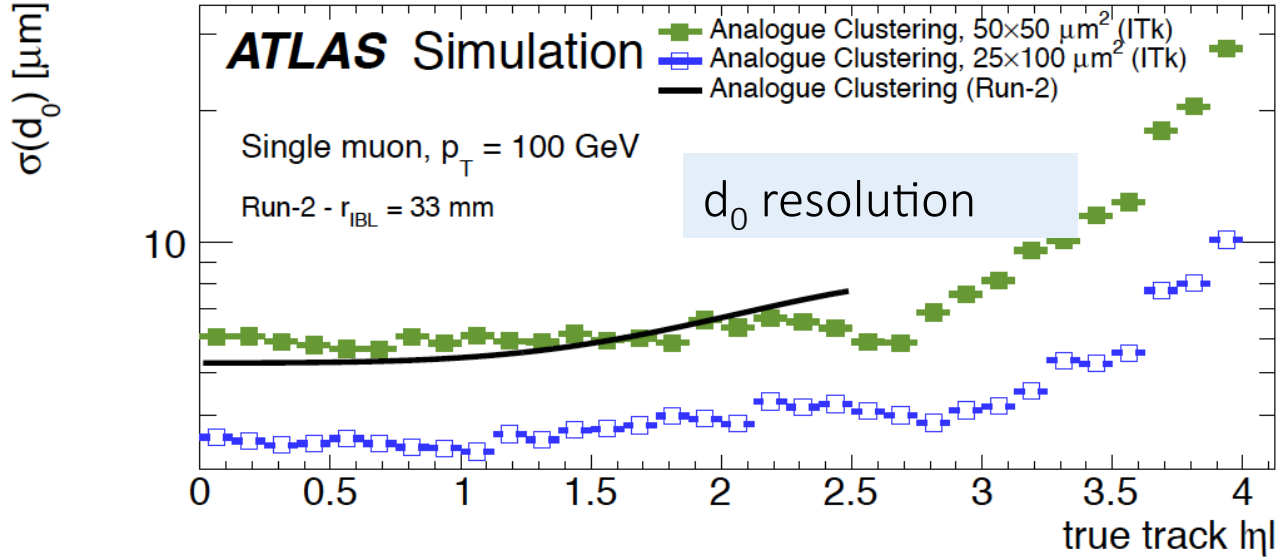


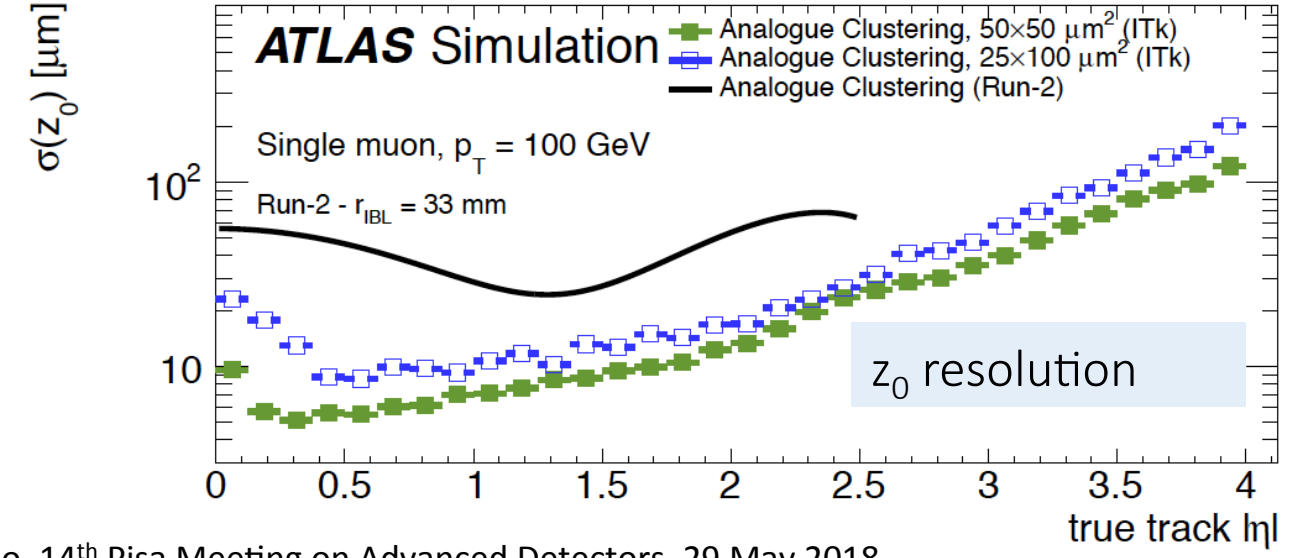
- A 5-layer pixel detector
- Coverage up to η=4
- Combined with the strip detector at least 9 points up to η=4
- Inclined layout: minimization of needed modules and more hits per layer for one track
- 10276 modules, 12.7 m^2, 5x10^9 channels

The ITk Performance

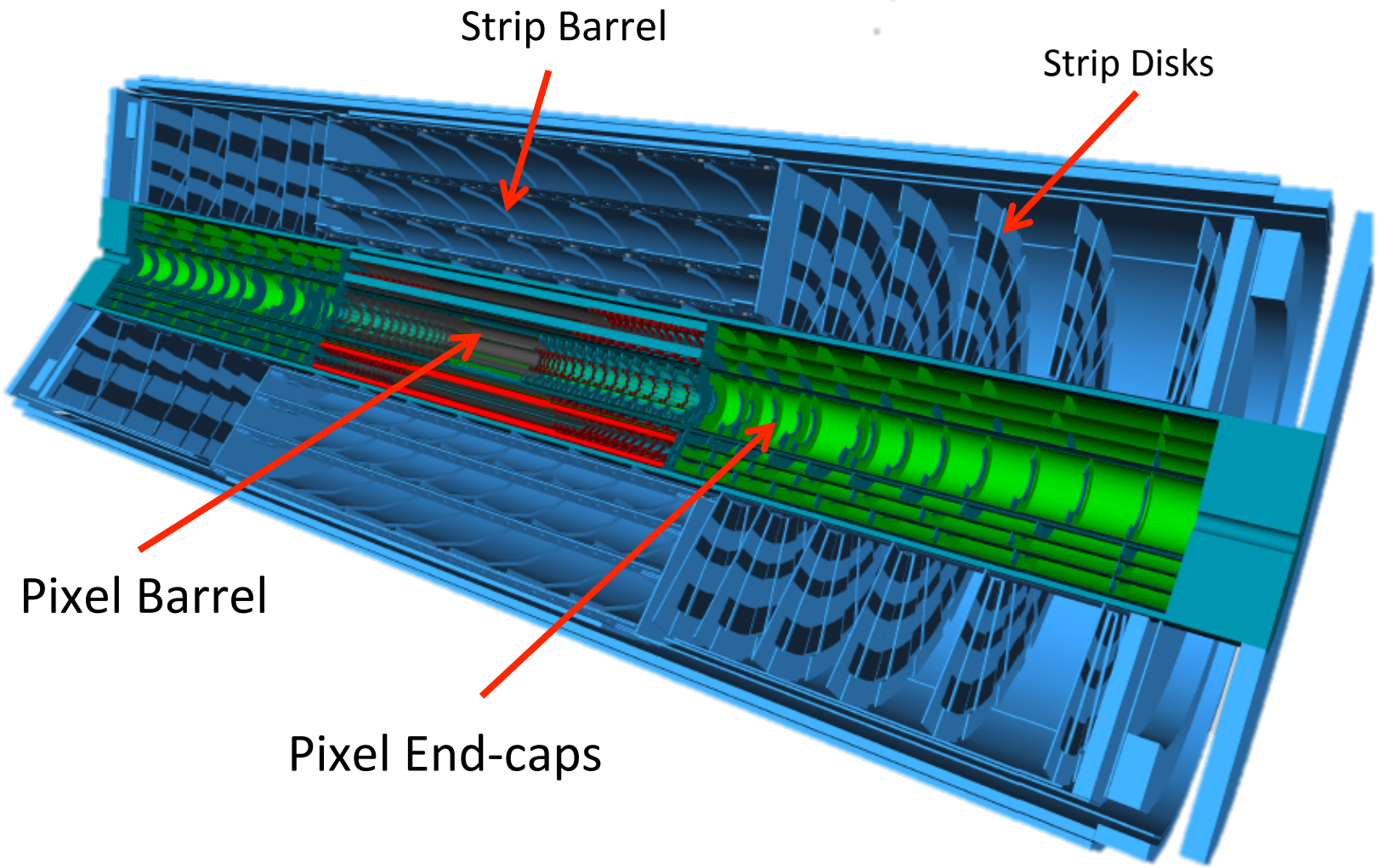
- Tracking resolution and particle identification performance comparable to or better than in Run-2, even with μ~200, for ITk Inclined layout
- Shows that our reconstruction algorithms are performing well in this challenging environment, and proper choices have been made in terms of optimal layout geometry







Pixel Mechanics



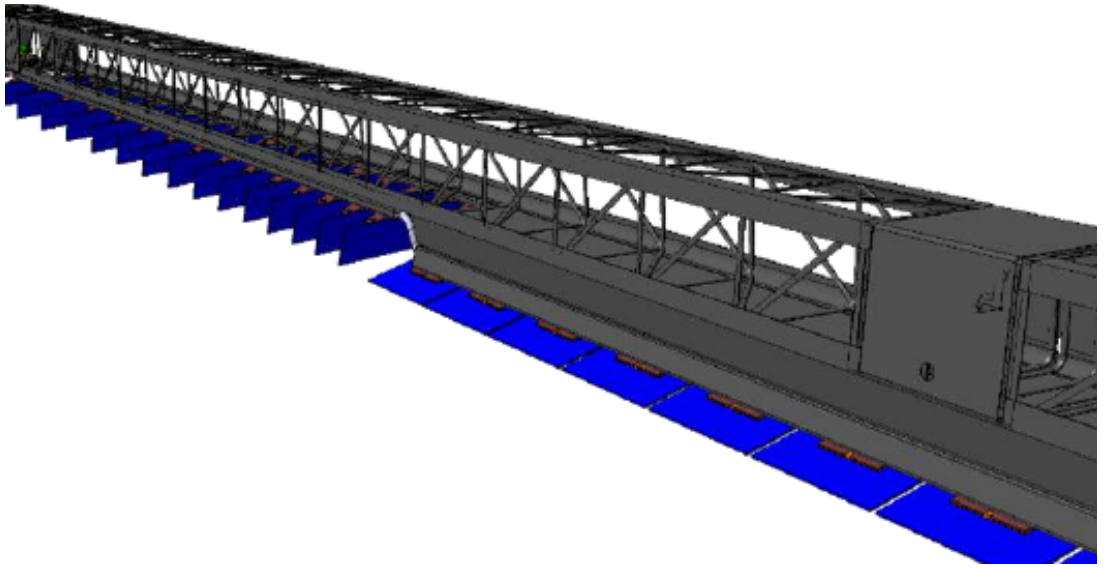
The mechanical design concept has been verified with simulations and prototypes

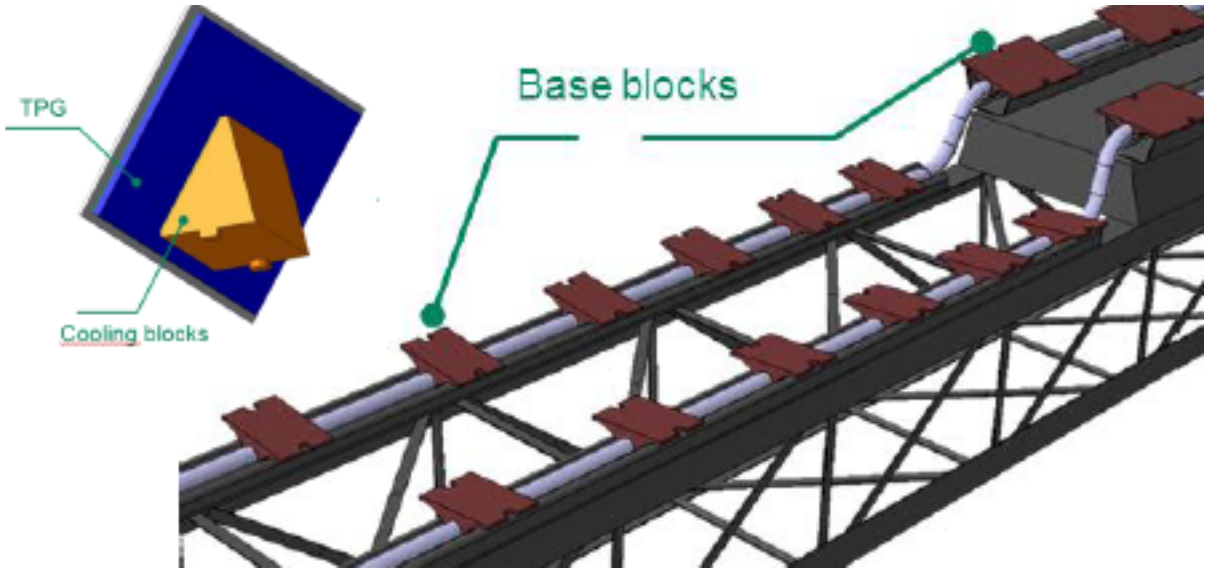
- Thermal performance proven in all sub-systems: the straight and inclined barrel sections, end-caps
- Specifications may be relaxed thanks to a possible decrease of the CO_2 saturation temperature and a decrease of the specified FE power

See L. Zwalinski, Poster Session

Local Supports - Barrel

- Design is based on the so called longeron:
  - A light filament winding structure carrying the modules on a thermal management cell
- Modules are first loaded on the cells that are then mounted on the longeron afterwards



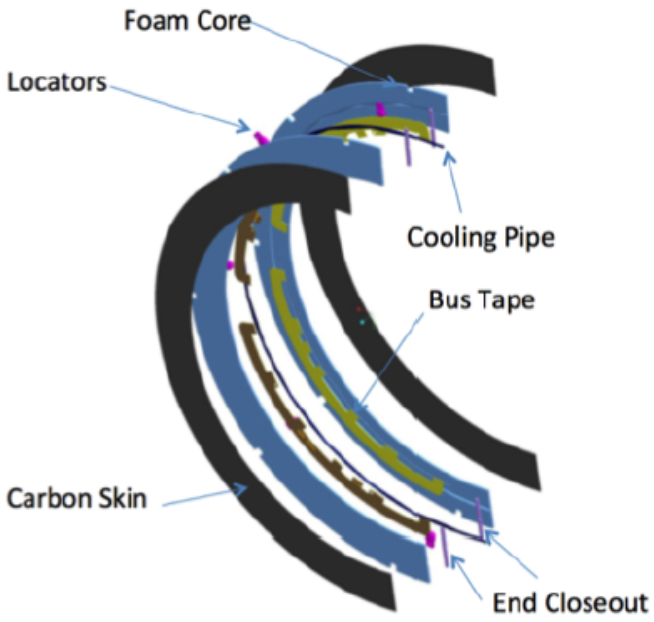


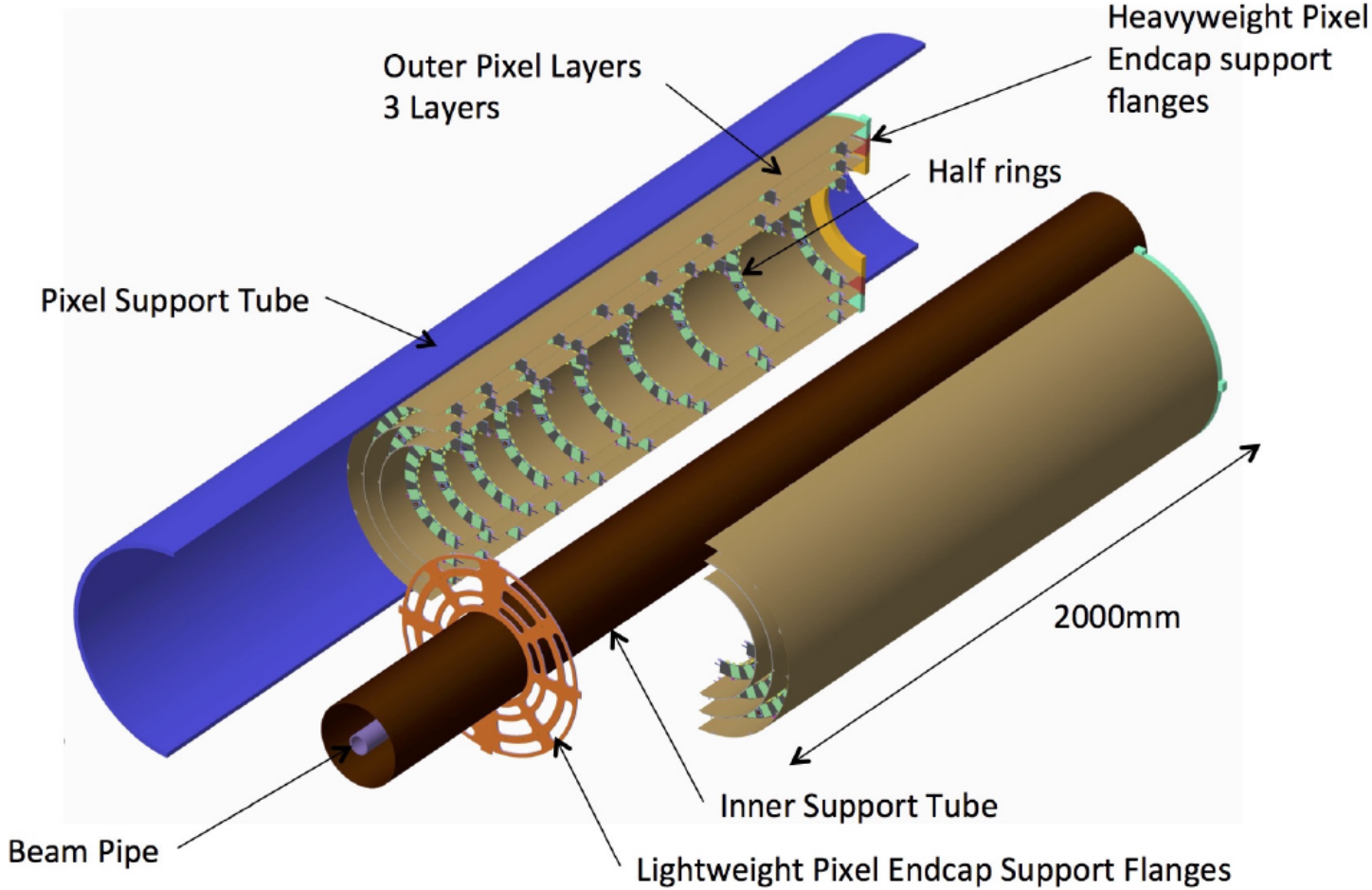
➡ Investigating the possibility of using quad modules in the inclined section to decrease the number of modules and simplify the loading procedure

Local Supports – End-caps

End-cap disks replaced by ring layers, each ring positioned to optimize coverage

Quad modules are mounted on both sides of the half rings, held in place by carbon fiber cylinders





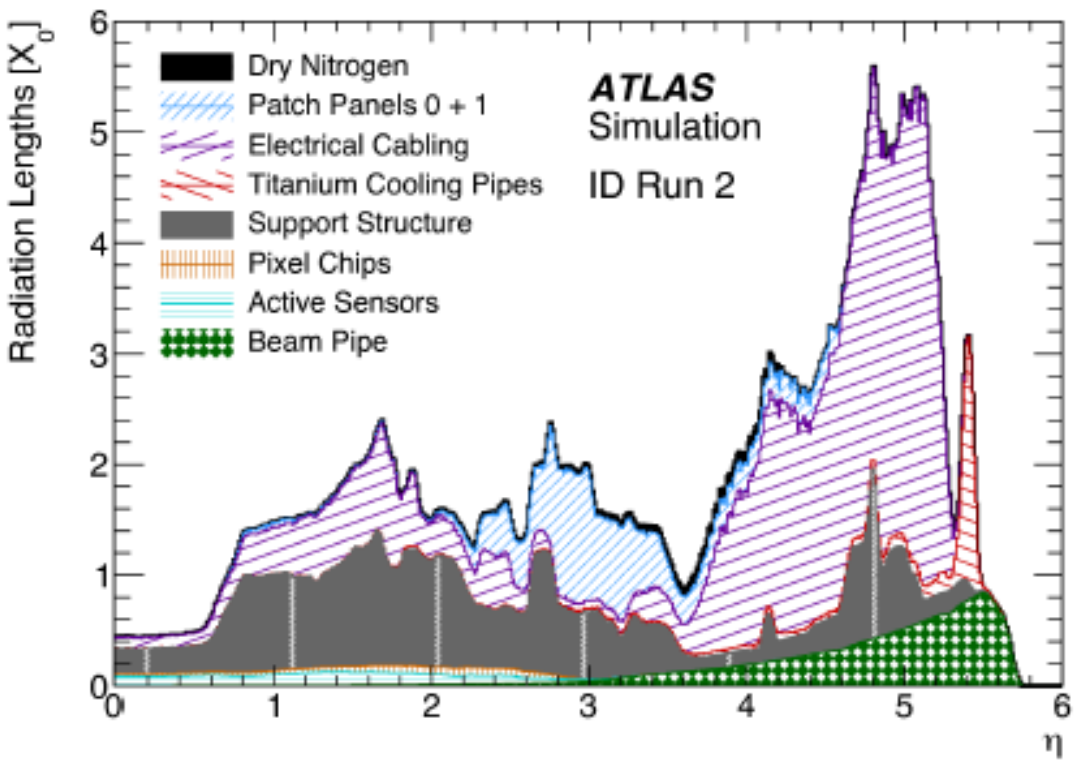
Services running inside the rings

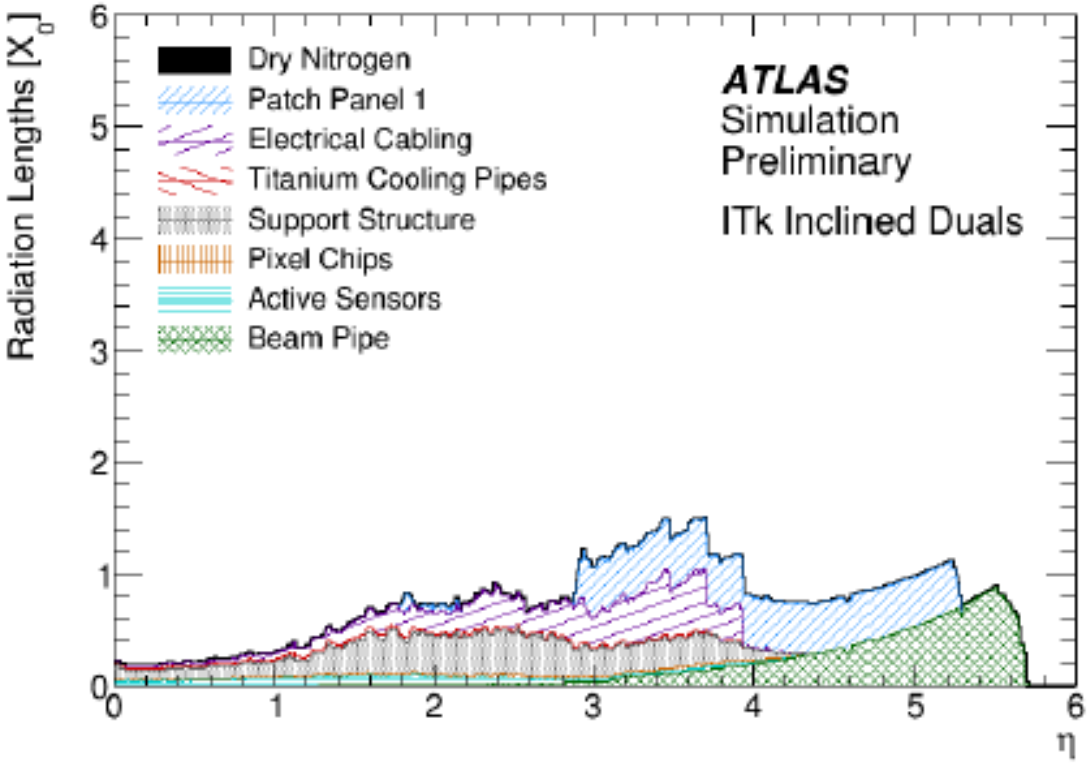
Material Budget

All the design choices (thin sensors & electronics, use of CO_2 evaporative cooling, use of serial powering, etc.) greatly reduced the material budget in the acceptance region (compared to the current Pixel detector that has one layer less) …

…and even more in the forward region up to η<5.5

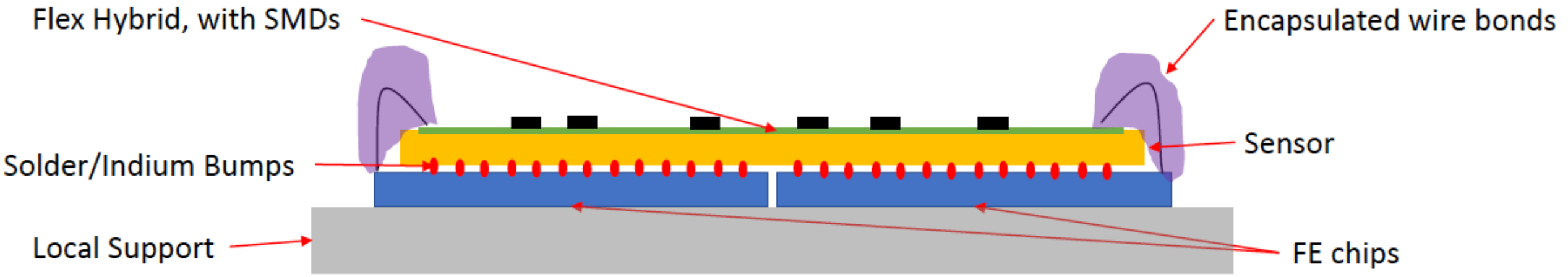
- Most of the reduction comes from cables, thanks to serial powering!





The Hybrid Module

- The module baseline is the classic hybrid module, made of a passive sensor bump-bonded to a FE chip
- Most of the ITk pixel modules are “quads”, one sensor interconnected to four FE chips



- A lot of experience has been accumulated in ATLAS with this type of detectors during LHC runs I and II

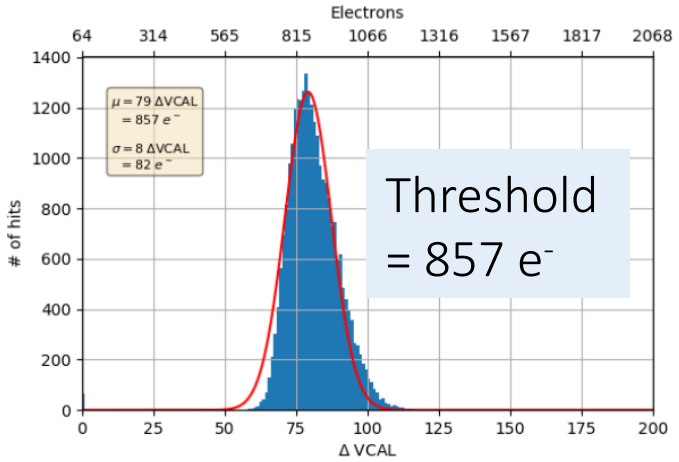
BUT …

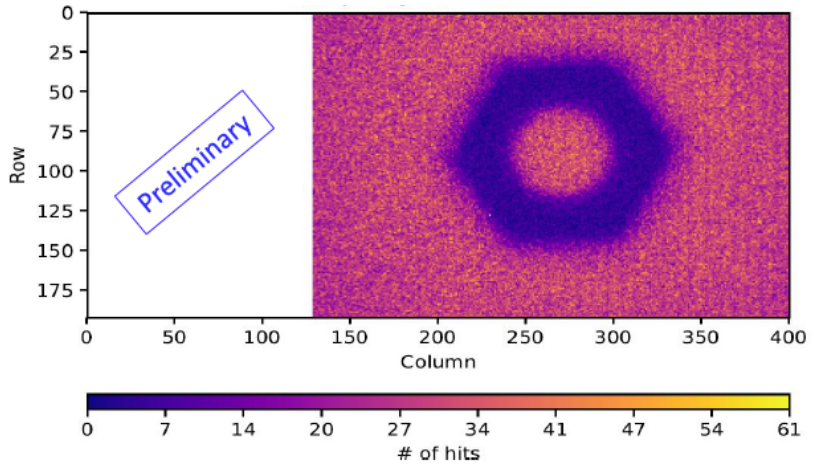
Factor 10 of increase in the number of modules →
assembly and interconnection simplification must be considered in the design phase

The ITk Pixel Readout Chip

- Based on the RD53A chip
- Increased radiation hardness using TSMC 65 nm CMOS process
  - Expected >500 Mrad
- Very encouraging preliminary results obtained with the RD53A chips and modules

  See L. Gaioni "Test results and prospects for RD53A, a large scale 65 nm CMOS chip for pixel readout at the HL-LHC" , Front-End Session





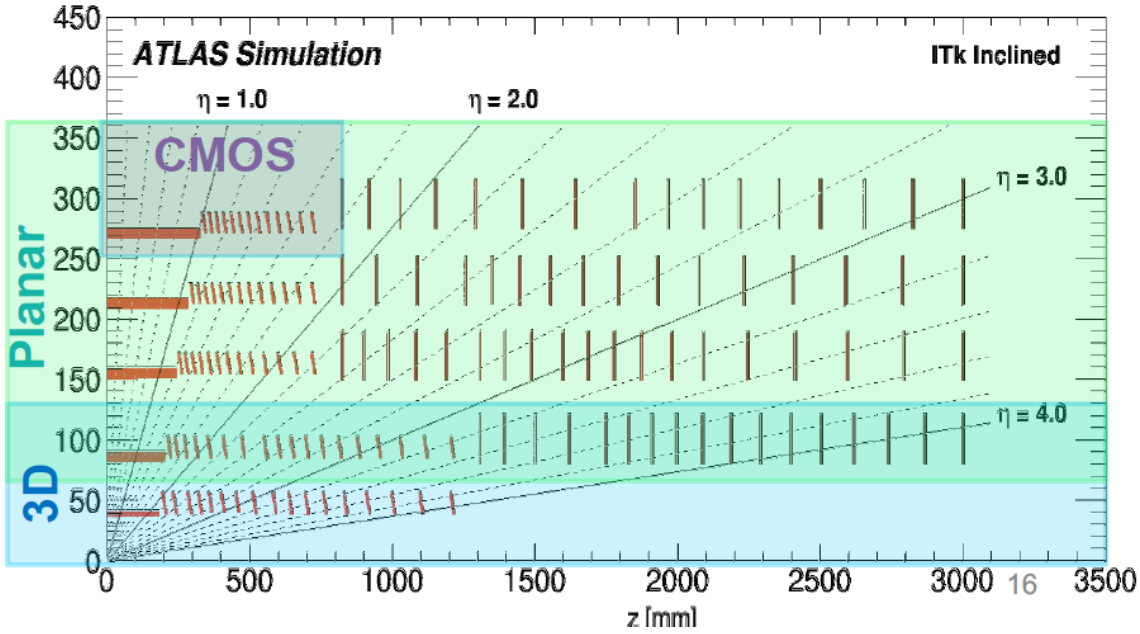
- New ITk chip prototype ready in summer 2019:
  - Expected decision on the analog flavor
  - ATLAS two level trigger support

- Data Transmission challenge:
  - FE ASIC uses 4x1.28 Gb/s links (ID now at 160 Mb/s)
  - 5.12 Gb/s used by one single FE chip in innermost layer and a full quad in the outermost layer
  - Aggregator chip is used to have to have 5.12 Gb/s in all links (~18k)

Pixel Sensors Technologies

Sensors technology must be tailored to the radiation environment

- 3D sensors in the innermost layer
  - 150 μm active thickness + up to 100 μm of support wafer
  - Single-chip sensors tiled to form double or quad modules
  - Maximum fluence in the innermost layer:
    1.3×10^{16} n_{eq}/cm^2
- Planar sensors
  - 100 μm active thickness in second layer
  - 150 μm active thickness in outermost layers
  - Two and four-chip sensors
  - Maximum fluence in the second layer:
    4×10^{15} n_{eq}/cm^2

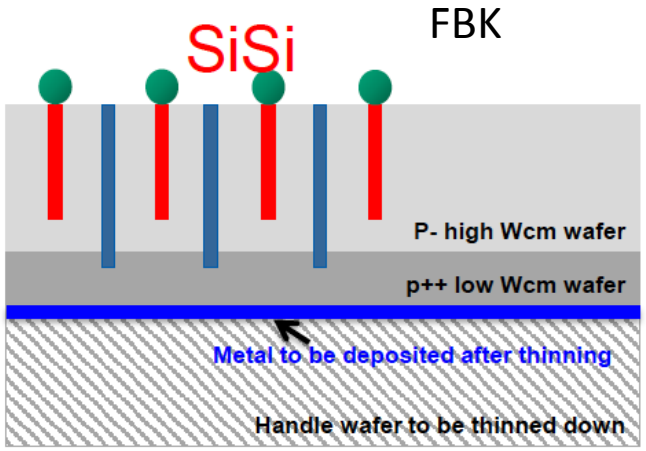


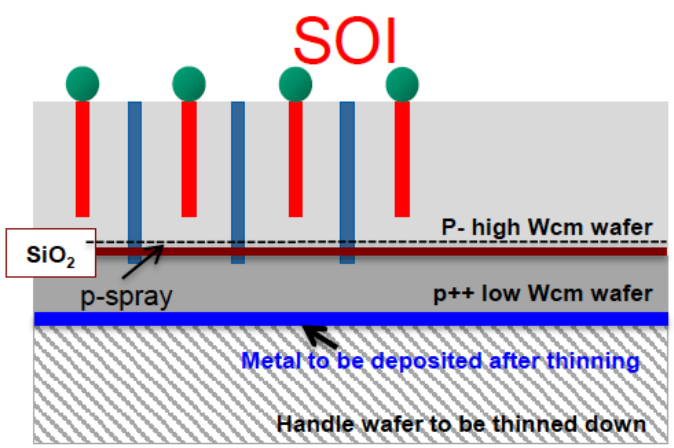
- Possible alternative for the fifth barrel layer: monolithic CMOS sensors:
  - Cost reduction with respect to hybrid modules
  - Radiation hardness up to 10^{15} n_{eq}/cm^2
  - Full size prototypes being evaluated now

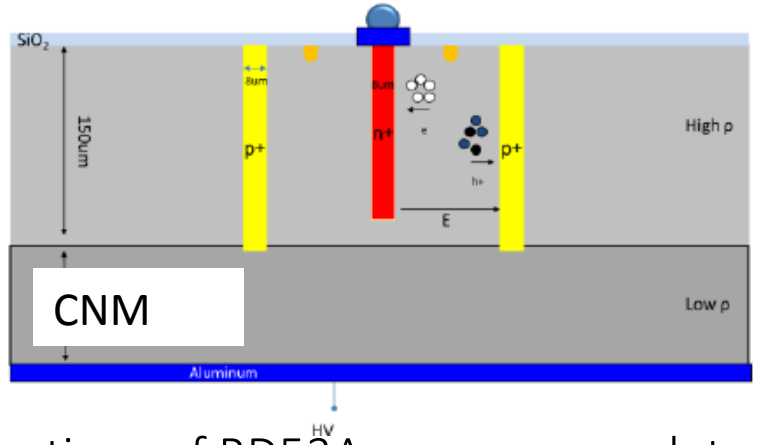
See contributions of H. Pernegger, K. Moustakas, C. Merlassino, M. Prathapan, F. Iguaz Gutierrez, F. Ehrler, R. Schimassek,

3D Sensors-Technology

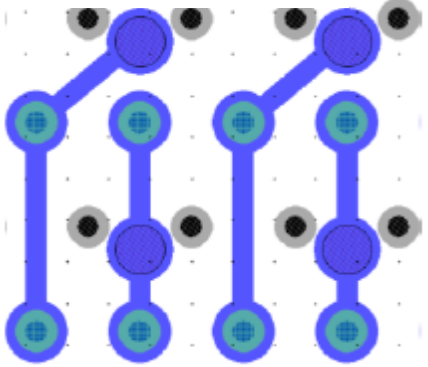
- Reduced thickness for ITk in comparison with IBL generation (230 μm thickness)
  - Support wafers needed in the production process



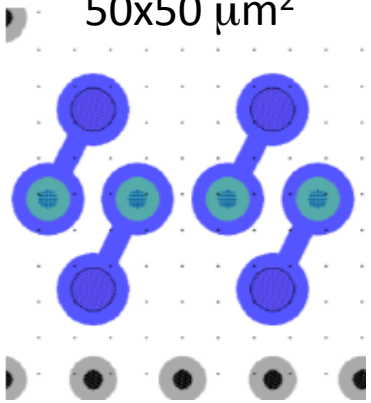




25x100 μm²



50x50 μm²



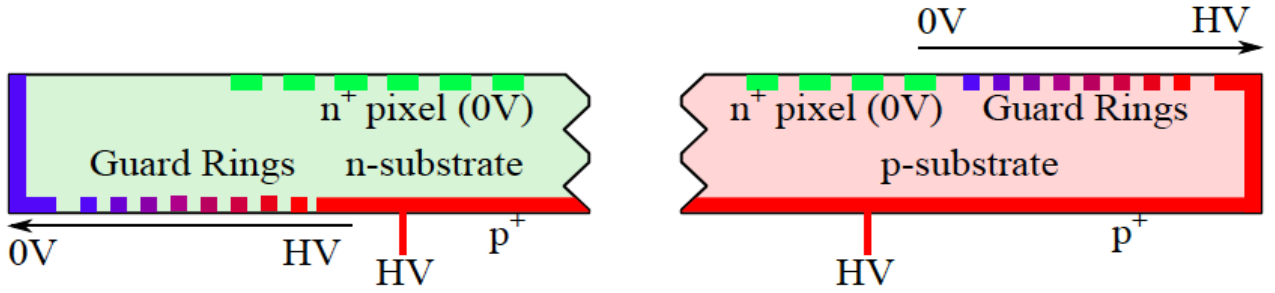
- Different productions of RD53A sensors completed or on-going at FBK, CNM and Sintef
  - 50x50 μm² or 25x100 μm²
    - 25x100 μm²: 2E could be problematic for yield and 1E for radiation hardness, to be studied with RD53A modules

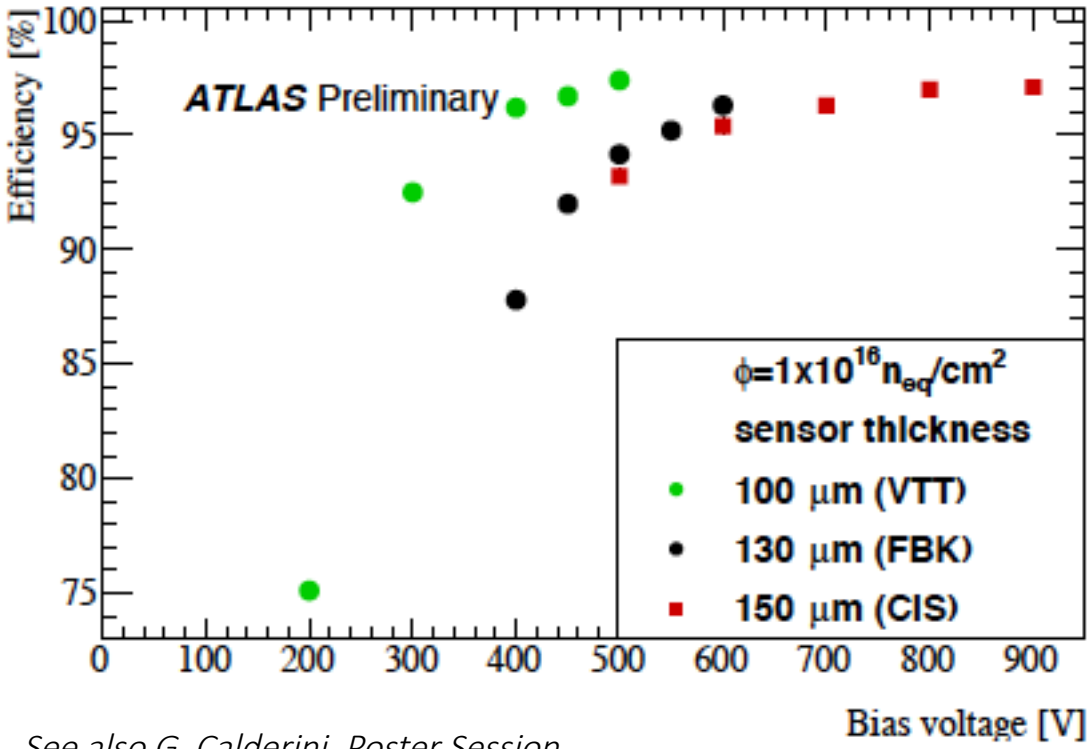
Planar Sensors

- N-in-p technology chosen for cost reduction and easier handling

- Thinner sensors reach charge and hit efficiency saturation at lower bias voltages → reduced power dissipation
  - 100 μm thin sensors baseline in the second layer
  - 150 μm thin sensors in the outermost layers

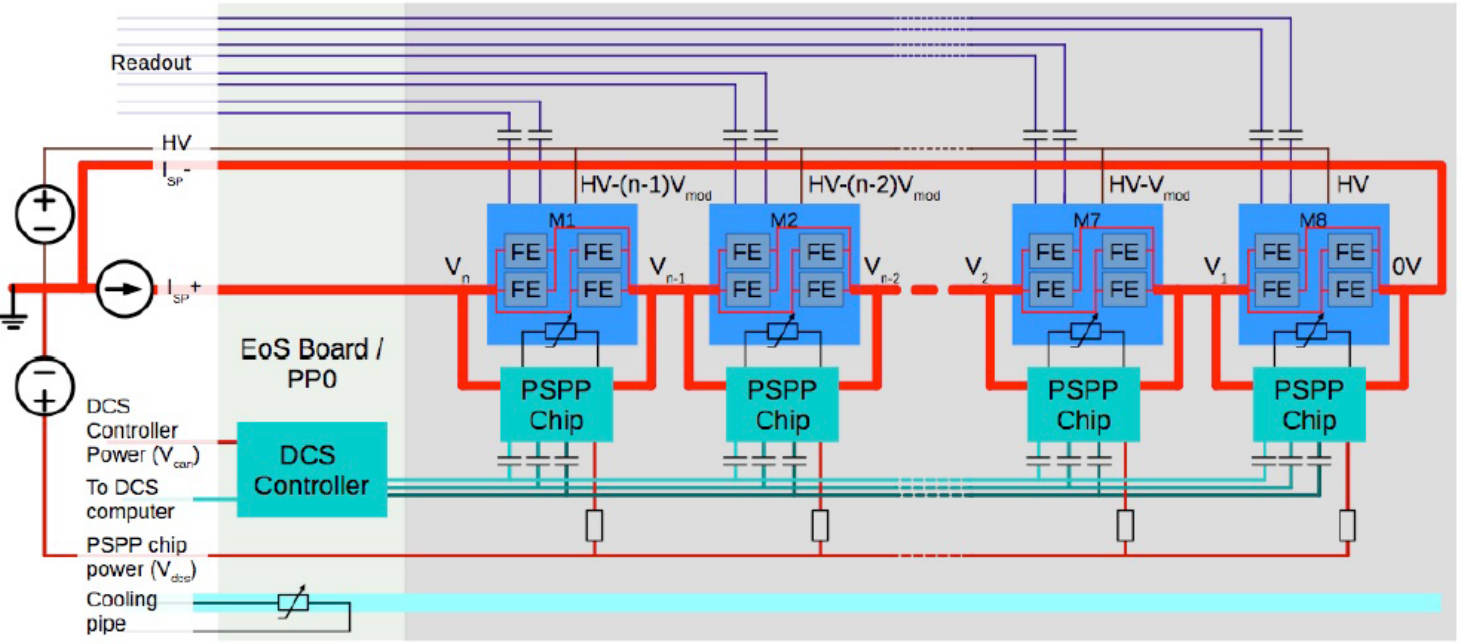
- Localized charge loss due to biasing structures after irradiation → effect has to be evaluated with the lower threshold expected with the RD53A chip

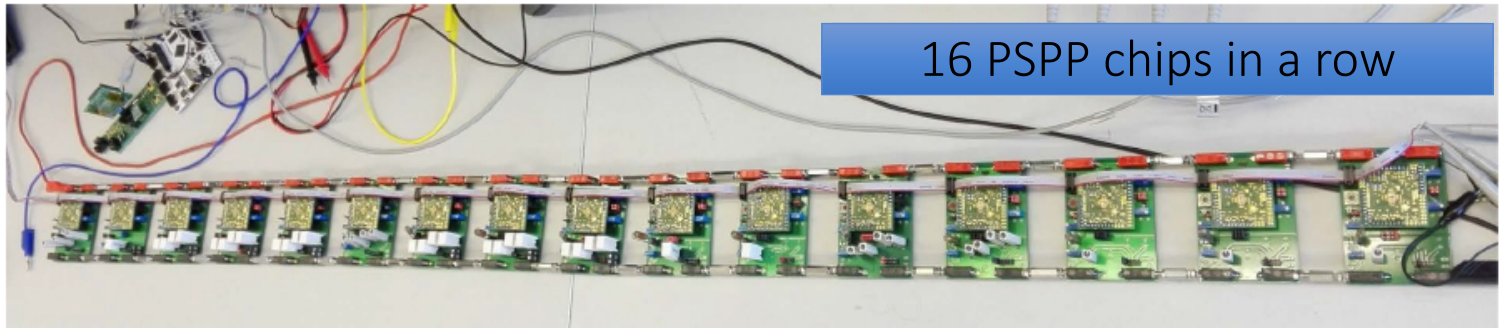




See also G. Calderini, Poster Session

Powering Scheme





Serial power to supply low voltage to modules in chain → material reduction
Enabled by special shunt circuit in RD53 chip

Parallel supplied HV, common return with LV

Protection to prevent the full chain to fail:

- PSPP chips to bypass the modules for LV protection. Up to 16 PSPP chips operated in a row → Fully functional!
- Fuses or switches to disconnect a module from HV (protection against shorts)

System Tests

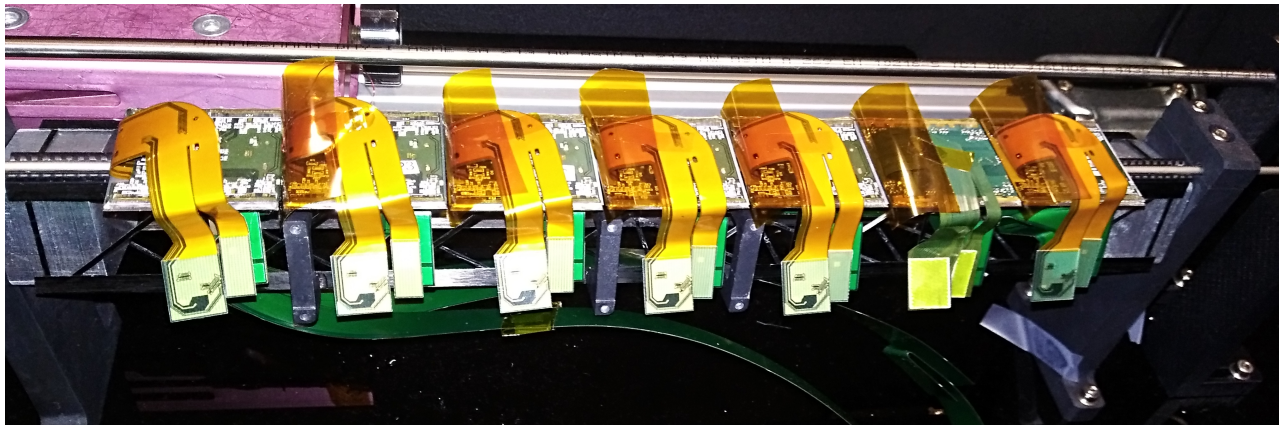
Several serial powering test setups:

- Test with up to 7 FE-I4 modules done so far.
- Tests for powering, noise introduction, cross-talk, …
- All tests show a safe operation with no distortion from noisy modules etc.

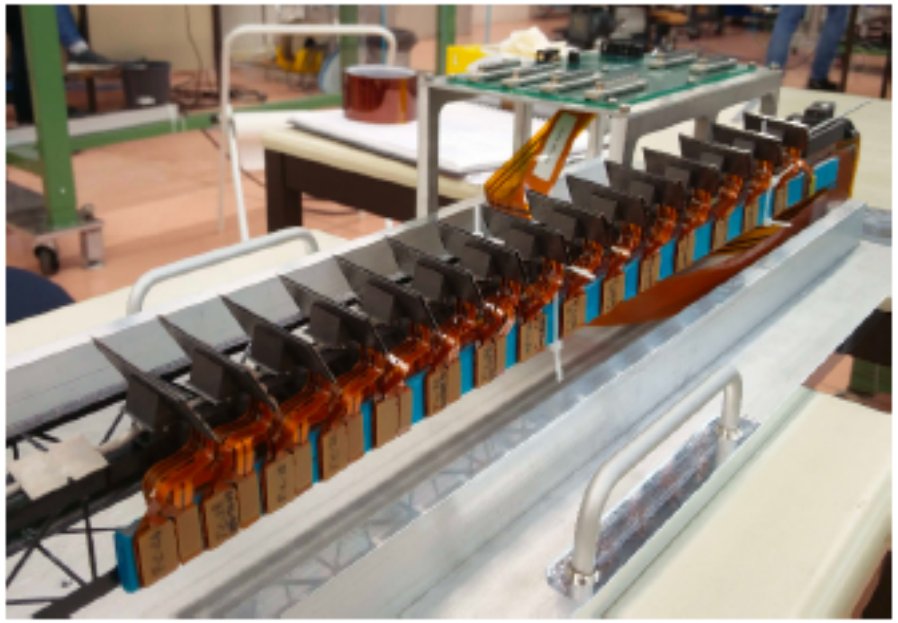
In addition prototypes for thermo-fluidic and thermal tests with CO_2 cooling

See L. Zwalinski, Poster Session

Serial powering, mechanical, loading tests planned for 2019 with RD53A quads module



Electrical prototype with 7 FE-I4 quads under test



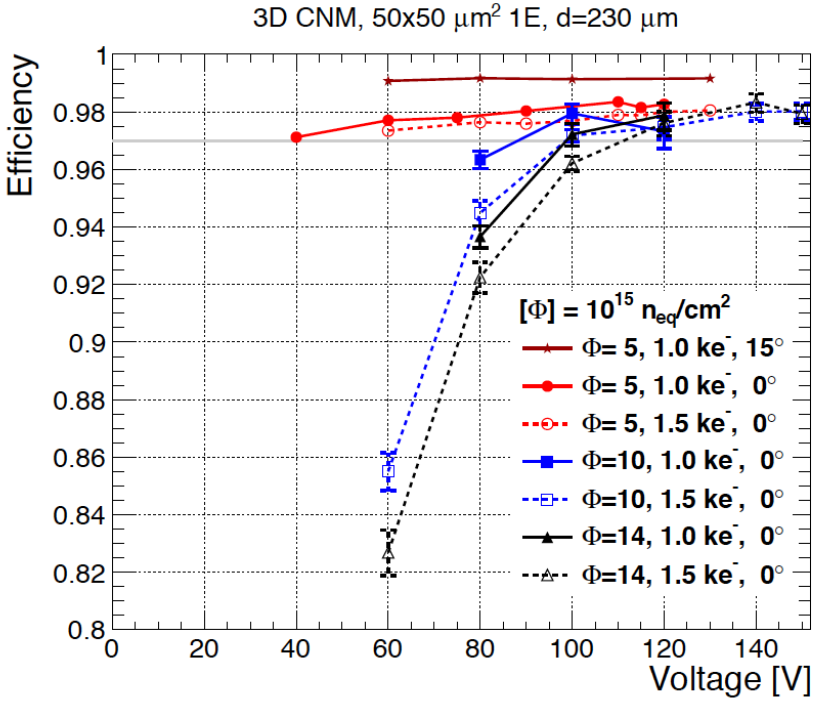
Thermal prototype with heaters: thermal figure of merit achieved

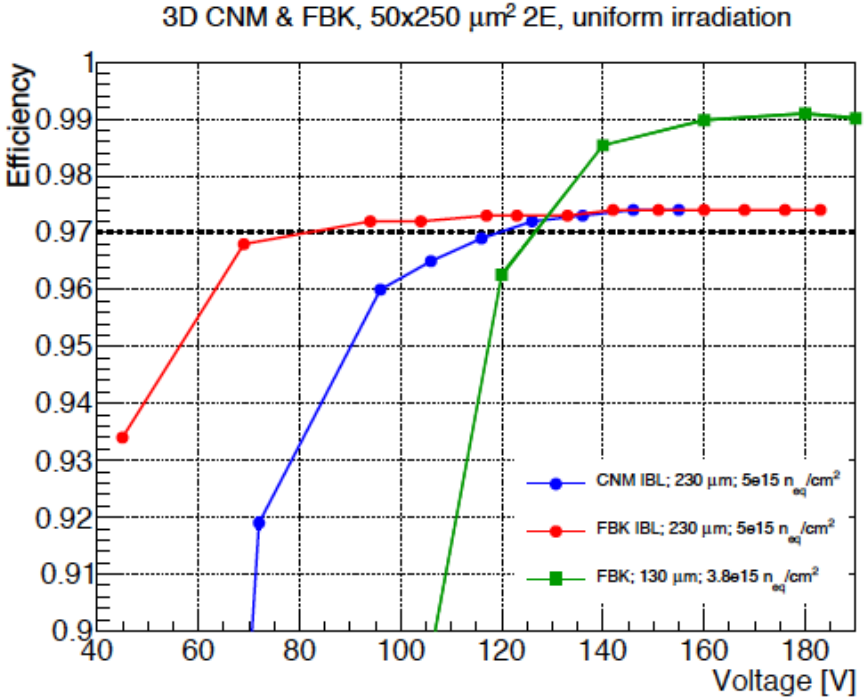
Conclusions and Outlook

- All the baseline components of the ITk pixel detectors have been defined and available in the collaboration or in the industrial environment.
  - In the module area validation with the RD53A is starting.
  - In the local support/services area, the design is getting more and more mature.
    - Thermal management under control
    - Service routing is undergoing a final optimization
- The construction schedule is tight and will require careful optimization and flexibility to react to problems.

Additional Material

3D Sensors- Test-beam Results



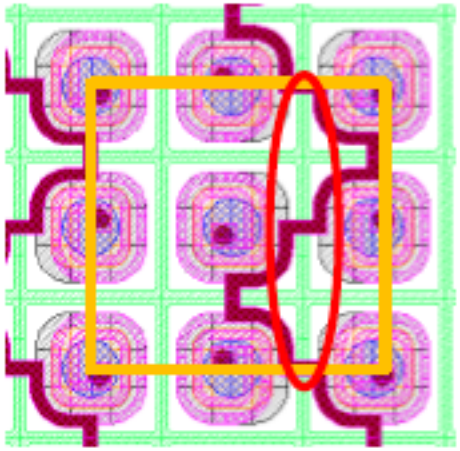


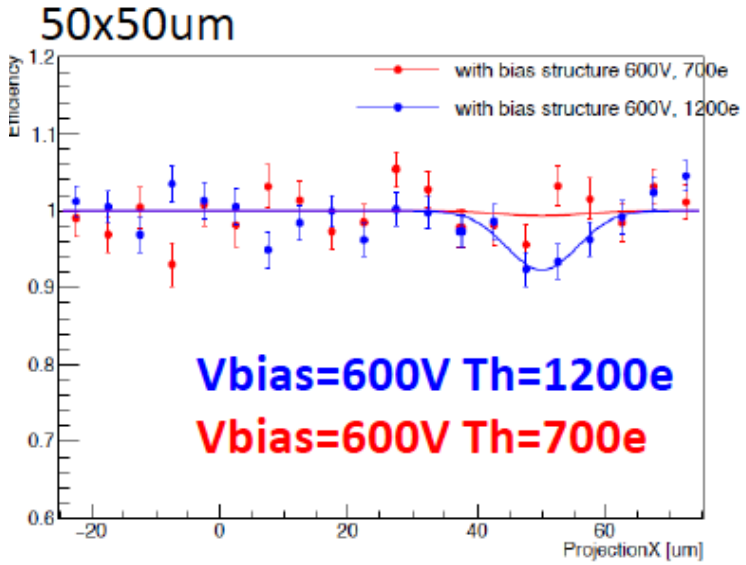
- Extreme radiation hardness
  - Hit efficiency > 97% at 100V for Φ=1.4x10^{16} n_{eq} cm^{-2}
  - Reduced electrode distance → lower operational voltage
  - Power dissipation ~ 13 mW/cm^2

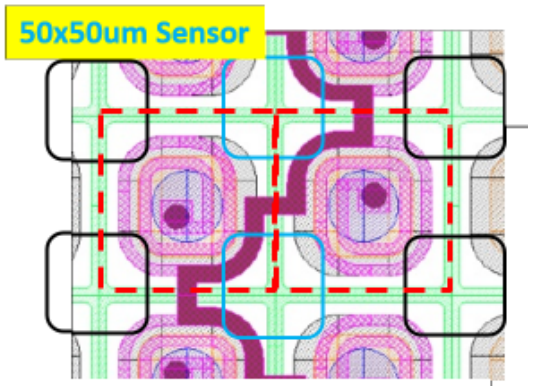
- A higher plateau efficiency reached for the thinner sample due to the smaller diameter electrode columns with respect to the IBL generation

Planar Sensors – Pixel cell Design

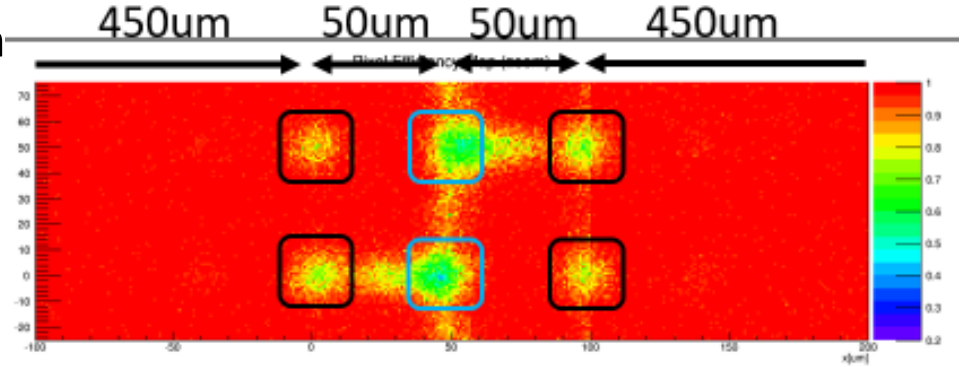
- Hit efficiency reduction after irradiation
  - Charge trapping
  - Localized charge loss due to biasing structures
    - Punch-through
    - Poly-silicon resistors
  - Particularly affecting small pixel cells
- Effect has to be evaluated with the lower threshold expected with the RD53A chip







- Φ=3x10^{15} n_{eq} cm^{-2}
- Poly-silicon resistor
- Modified FE-I4 compatible sensor
- Threshold= 2500 e
- Hit efficiency in 50x50 μm^2 cell =93.87%



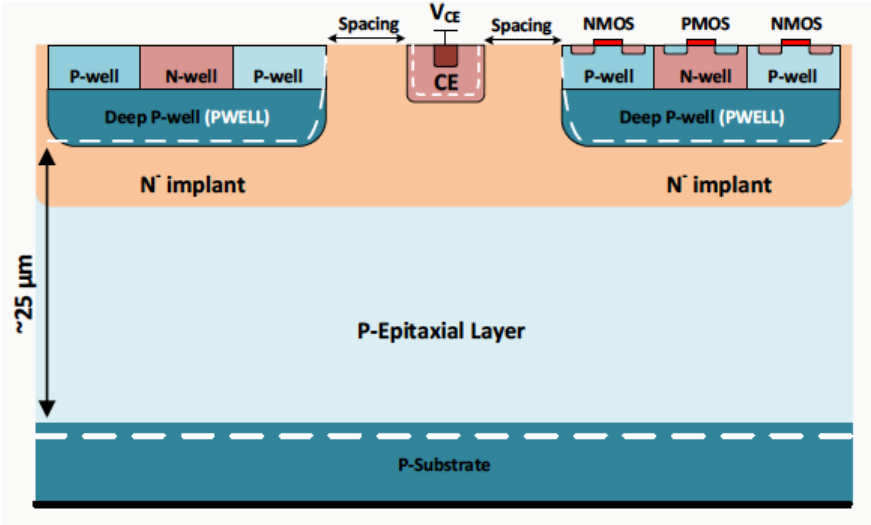
- Encouraging results with the FE65-P2 demonstrator chip
  - Threshold 700 e

DMAPS Developments

- Requirement for application in ATLAS ITk:
  - Fast charge collection to avoid trapping after irradiation and be 25 ns in-time efficient
  - Large depletion region for higher signals
- Higher rate capability

- DMAPS: Depletion is key for fast signal response and radiation hardness - Enabling technologies: High voltage process and high resistive wafers

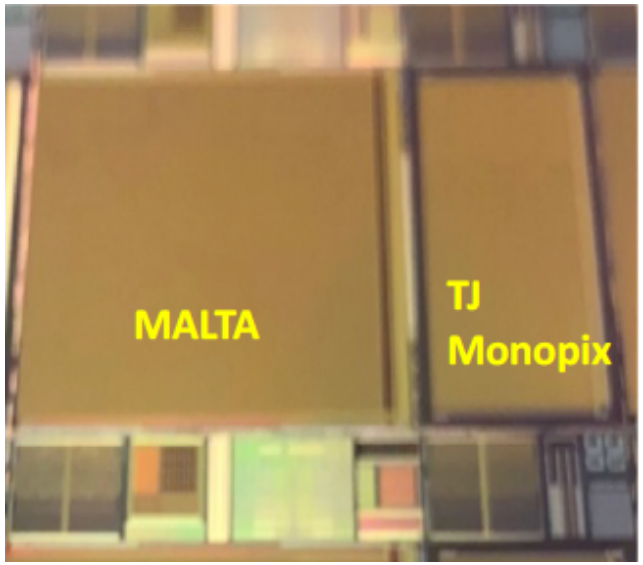
• High granularity, Low material budget and power, Large area at reduced cost with respect to hybrid modules



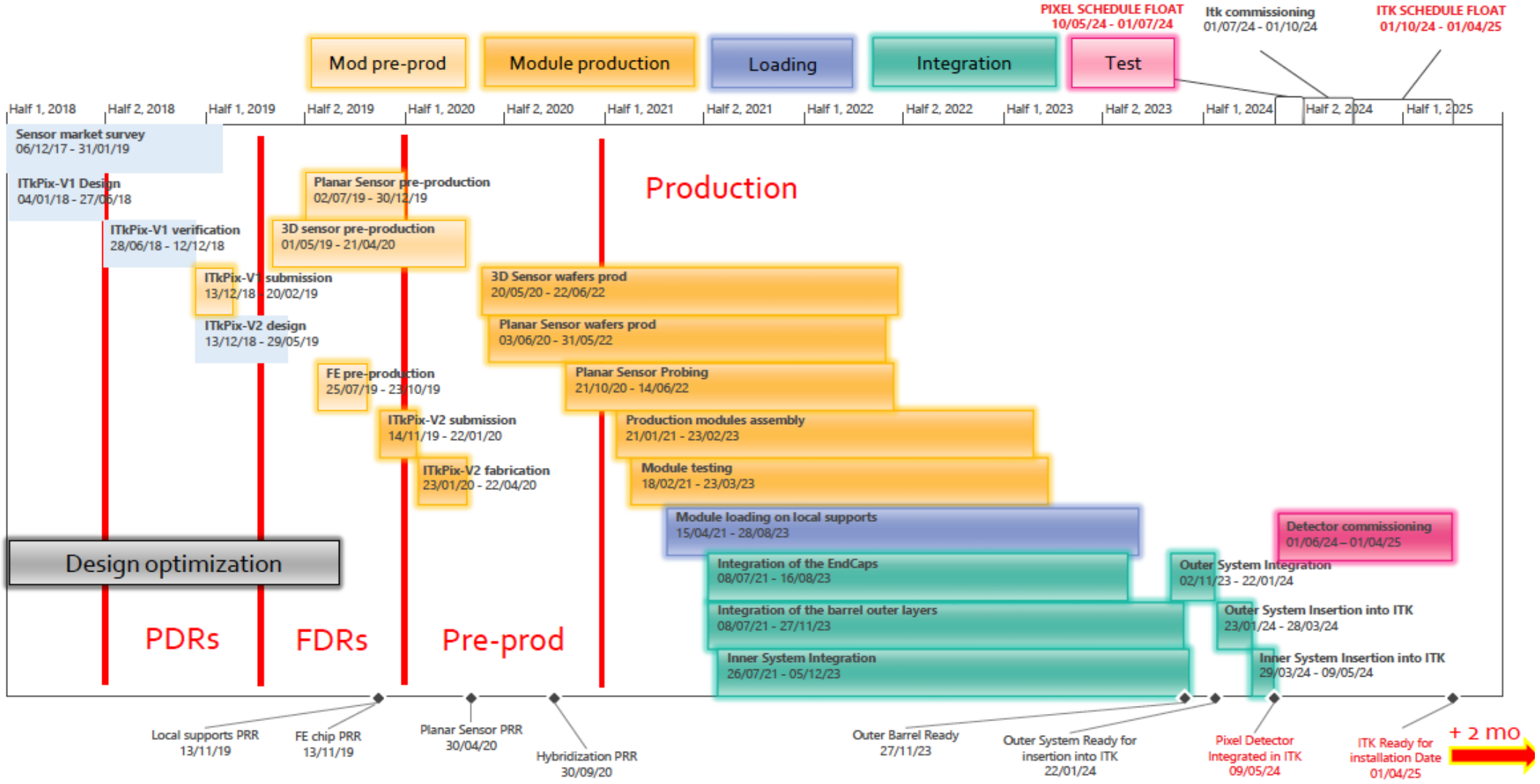
See contributions of H. Pernegger, K. Moustakas, C. Merlassino

Particularly interesting is the novel modified TJ-180 process:

- Full depletion radiation tolerant to bulk damage
- Small n-well collection electrode
- Small sensor capacitance → low noise and power
- Full size prototypes being evaluated as a possible technology for the barrel L4 in ITk



Schedule


PIXEL SCHEDULE FLOAT
10/05/24 - 01/07/24
Itk commissioning
01/07/24 - 01/10/24
ITK SCHEDULE FLOAT
01/10/24 - 01/04/25
Mod pre-prod
Module production
Loading
Integration
Test
Half 1, 2018
Half 2, 2018
Half 1, 2019
Half 2, 2019
Half 1, 2020
Half 2, 2020
Half 1, 2021
Half 2, 2021
Half 1, 2022
Half 2, 2022
Half 1, 2023
Half 2, 2023
Half 1, 2024
Half 2, 2024
Half 1, 2025
Sensor market survey
06/12/17 - 31/01/19
ITkPix-V1 Design
04/01/18 - 27/06/18
ITkPix-V1 verification
28/06/18 - 12/12/18
ITkPix-V1 submission
13/12/18 - 20/02/19
ITkPix-V2 design
13/12/18 - 29/05/19
Planar Sensor pre-production
02/07/19 - 30/12/19
3D sensor pre-production
01/05/19 - 21/04/20
FE pre-production
25/07/19 - 23/10/19
ITkPix-V2 submission
14/11/19 - 22/01/20
ITkPix-V2 fabrication
23/01/20 - 22/04/20
Production
3D Sensor wafers prod
20/05/20 - 22/06/22
Planar Sensor wafers prod
03/06/20 - 31/05/22
Planar Sensor Probing
21/10/20 - 14/06/22
Production modules assembly
21/01/21 - 23/02/23
Module testing
18/02/21 - 23/03/23
Module loading on local supports
15/04/21 - 28/08/23
Integration of the EndCaps
08/07/21 - 16/08/23
Integration of the barrel outer layers
08/07/21 - 27/11/23
Inner System Integration
26/07/21 - 05/12/23
Outer System Integration
02/11/23 - 22/01/24
Outer System Insertion into ITK
23/01/24 - 28/03/24
Inner System Insertion into ITK
29/03/24 - 09/05/24
Detector commissioning
01/06/24 – 01/04/25
Design optimization
PDRs
FDRs
Pre-prod
Local supports PRR
13/11/19
FE chip PRR
13/11/19
Planar Sensor PRR
30/04/20
Hybridization PRR
30/09/20
Outer Barrel Ready
27/11/23
Outer System Ready for insertion into ITK
22/01/24
Pixel Detector Integrated in ITK
09/05/24
ITK Ready for installation Date
01/04/25
+ 2 mo