Random Telegraph Signal Fluctuations of the Dark Count Rate in CMOS SPADs

SiPM workshop – Bari 2019

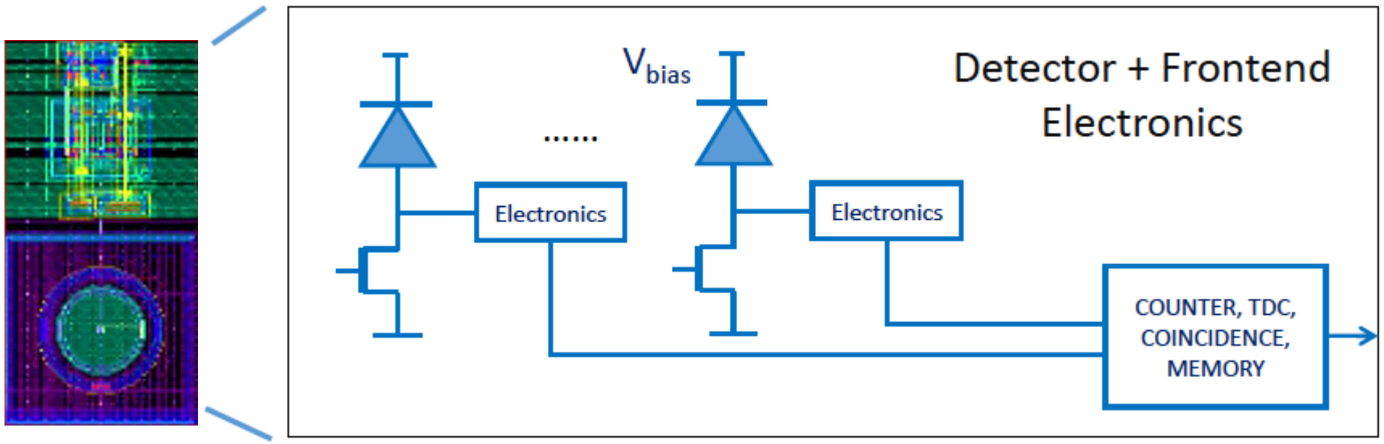
F. Di Capua, D. Fiore, M. Campajola, E. Sarnelli, L. Gasparini, M. Garcia

SPAD CMOS: adavantages and drawbacks

- First implementation of SPAD in CMOS technological process has been achieved in 2003, since them many improvements have been obtained

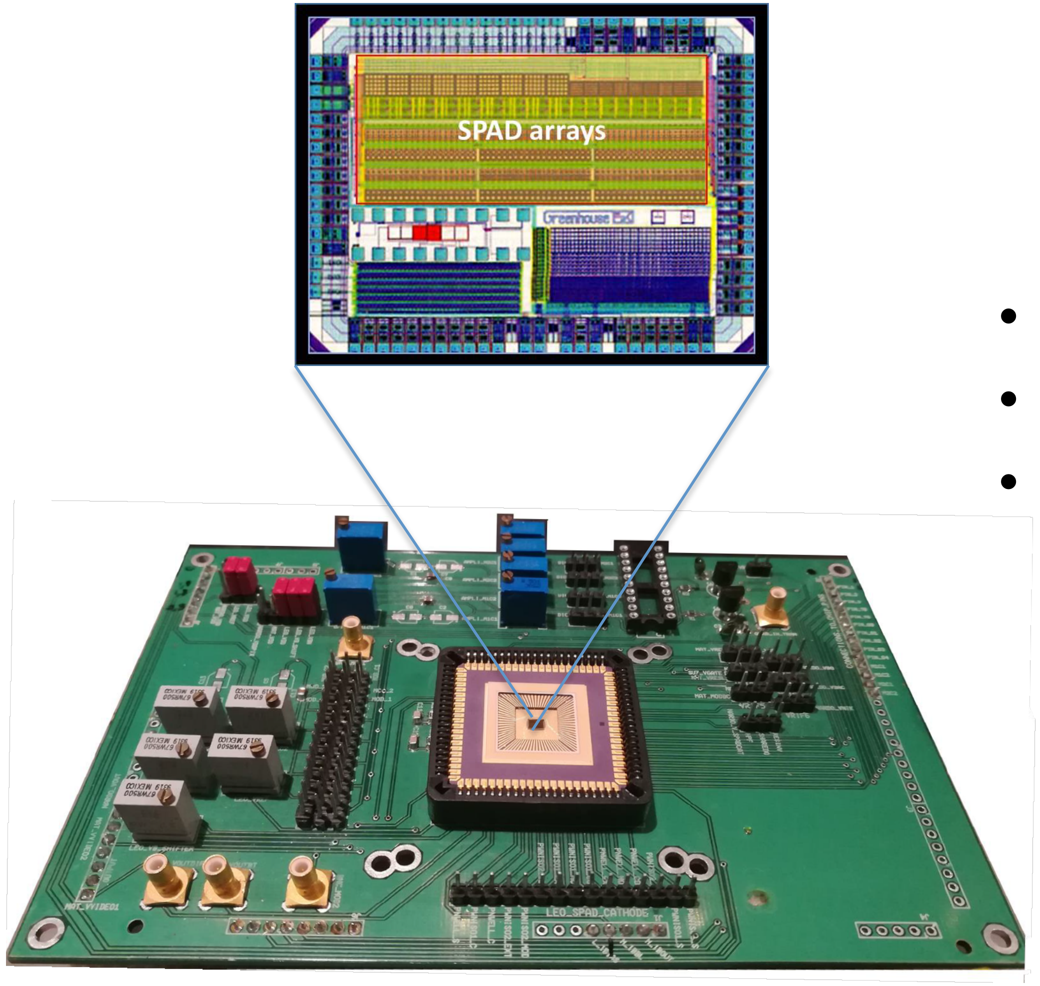
SPAD implemented in CMOS technology

- High time resolution
- Position sensitive device: particle tracking, imaging…
- Addressing the output of a single SPAD pixel
- Post-processing circuits integrated on chip
- Low power
- Still High-DCR with respect to custom processes



SPAD Devices Under Test

- Device designed by Fondazione Bruno Kessler (Italy)
- SPADs implemented in a 150-nm CMOS process (LFoundry)
- Several junction layouts and different active area size in the chip



- Matrices 5x5 and array lines
- 5, 10, 15, 20 μm dimension
- Different junctions lauyouts

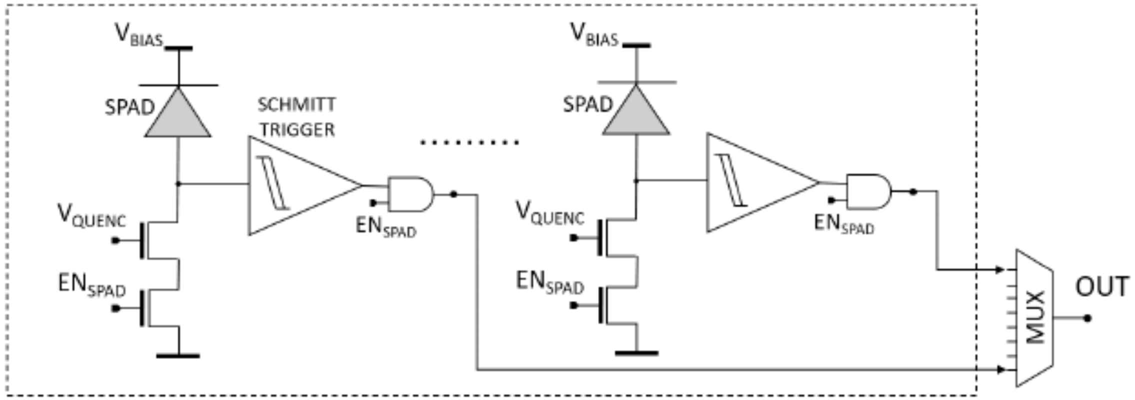
SPAD Devices Under Test

Pixel architecture

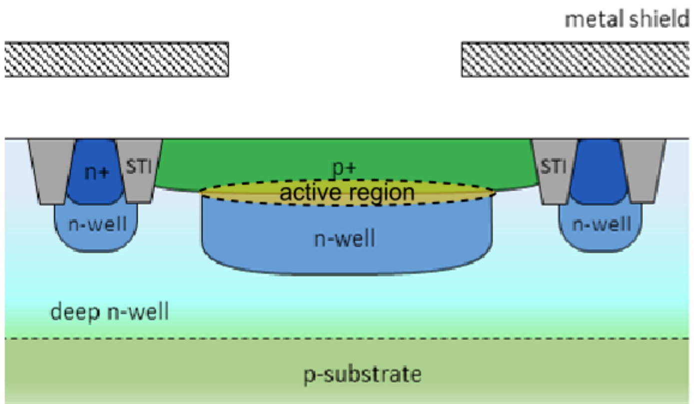
Each SPADs is implemented with front-end electronics:

- A trigger digitalize the pulse;
- MUX select one pixel at the time;

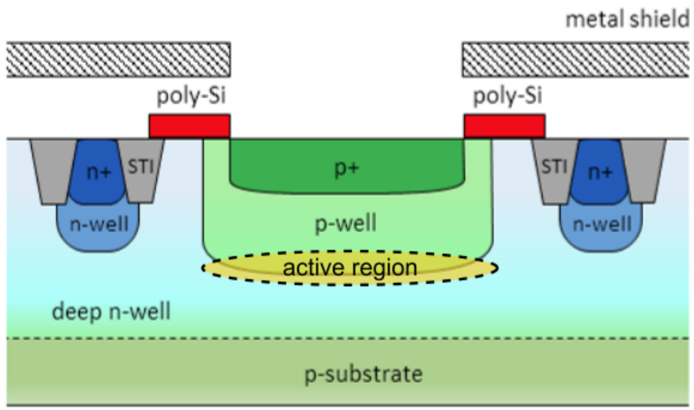
In-pixel front-end



P+/Nwell junction (PN)

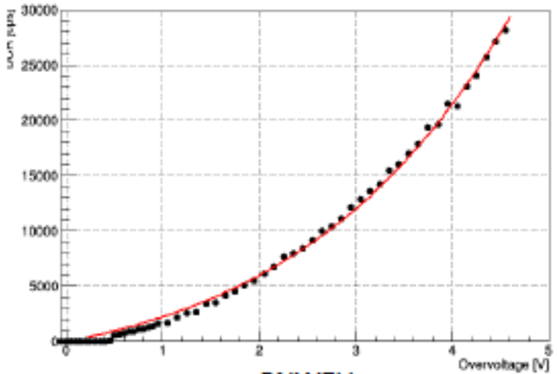


Pwell/Niso junction (PWNISO)

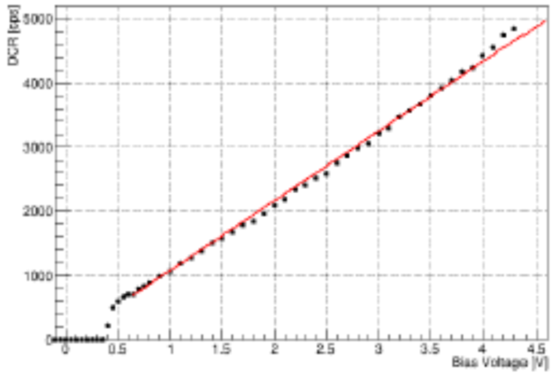


DCR Pre-Irradiation characterization

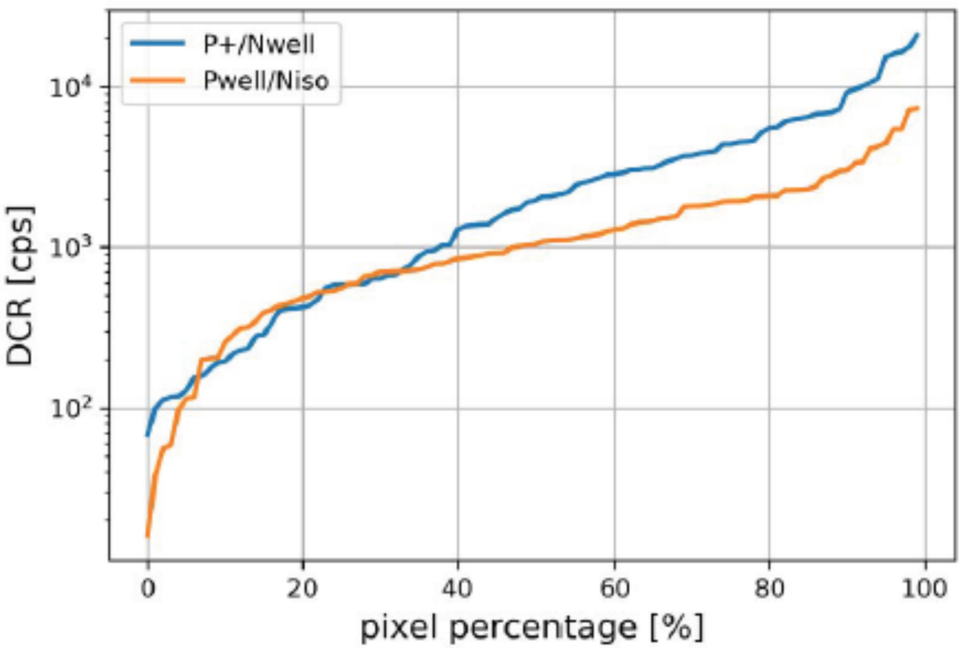
DCR vs Overvoltage



PNWELL



PWNISO1

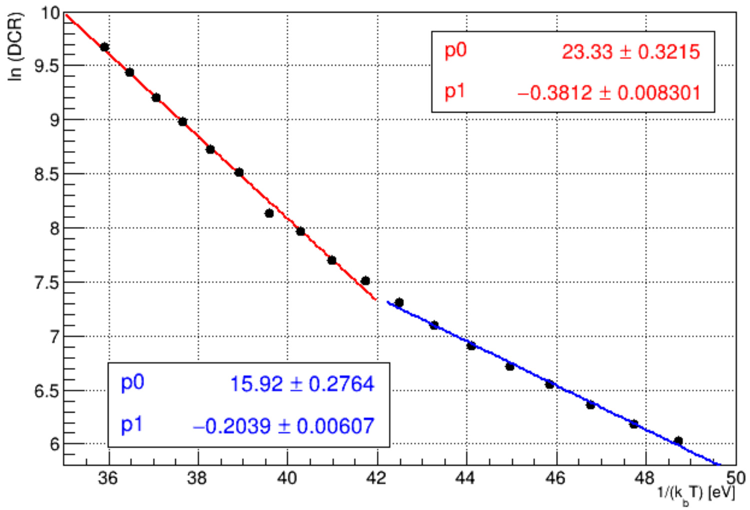


	PN	PWNISO
Median DCR (cps/μm^2)	19.4±0.4	10.4±0.3
Mean DCR (cps/μm^2)	33.4±0.6	14.5±0.4

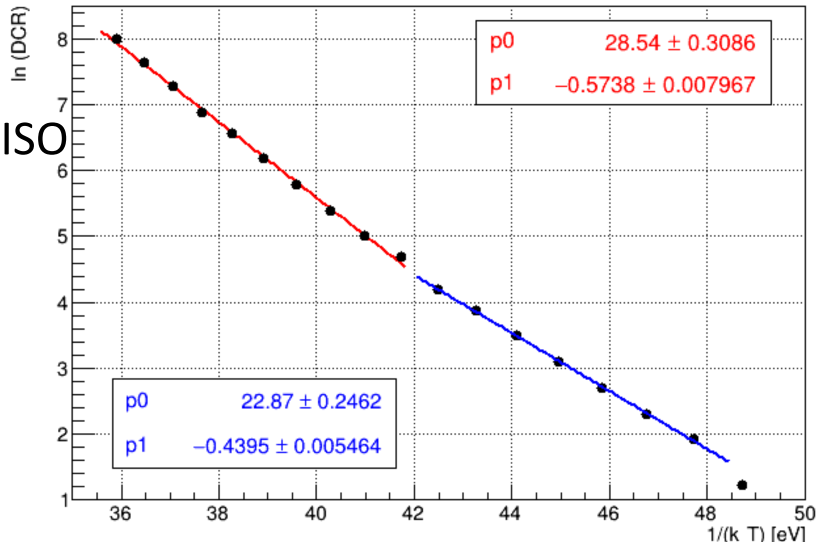
P+/Nwell exhibits twice larger DCR compared to Pwell/Niso designs

DCR vs Temperature: Activation Energy

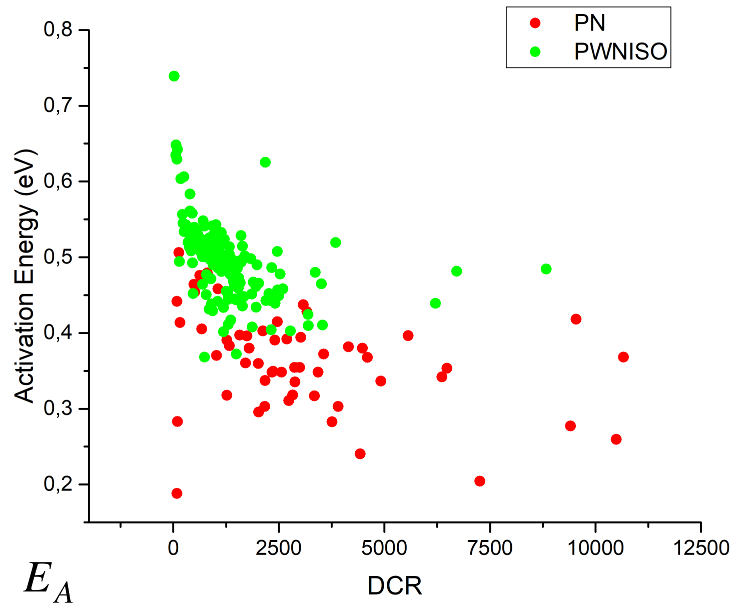
PN



PWNISO

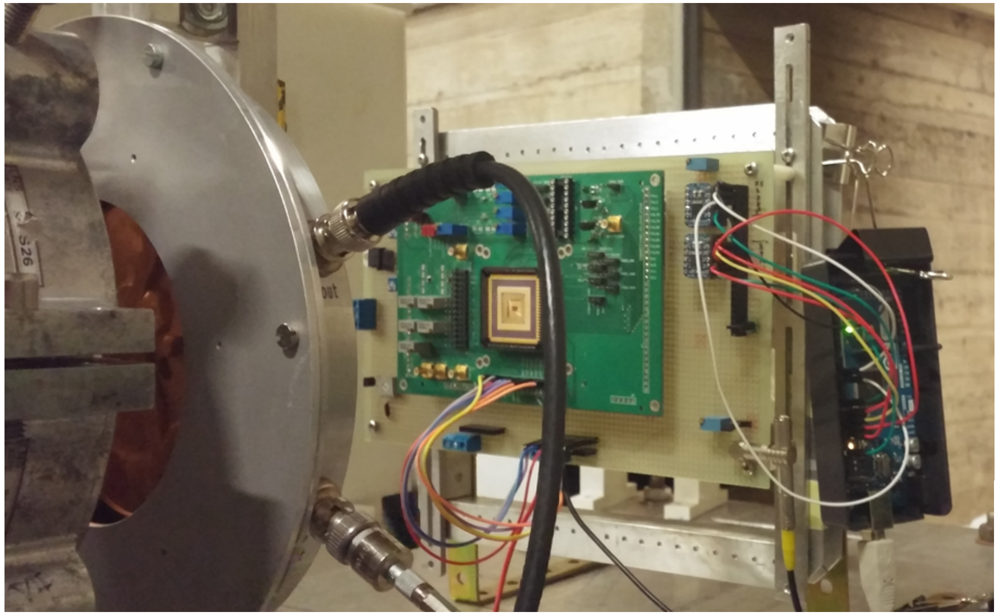


- The change of slope is more evident in PN structutes with respect to PWNISO
- On average the activation energy for PN is lower
- PN structures have by design higher electric fields in the junction: this implies an higher contribution from tunneling process to DCR

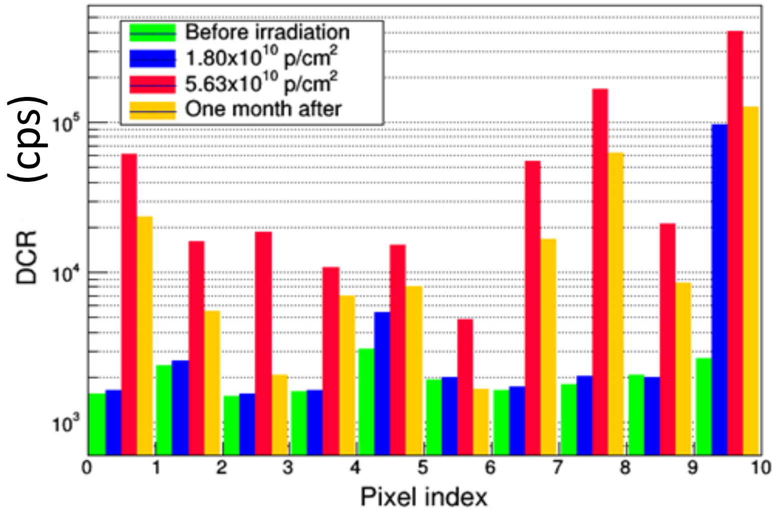


$$DCR = Ae^{-\frac{E_A}{k_B T}}$$

Proton Irradiation



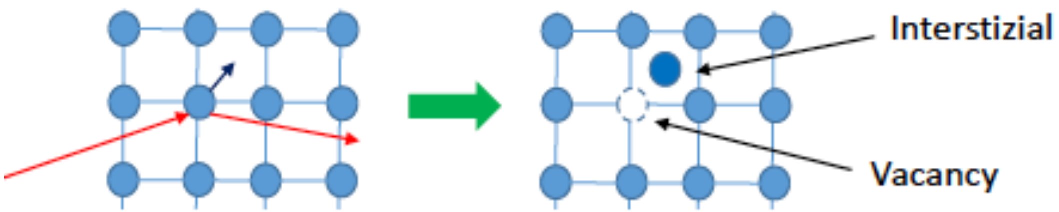
- 62 MeV protons at CATANA beam line (LNS, Catania – Italy)
- 24 MeV at Tandem accelerator (LNS, Catania – Italy)
- DCR measurements after irradiations

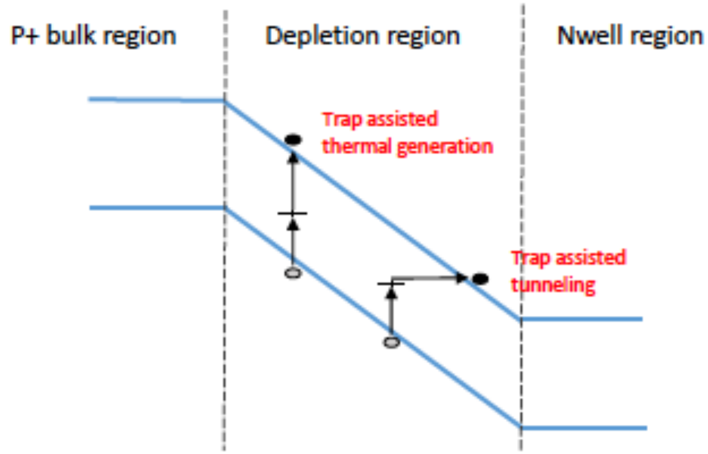


Chip	Run	Fluence [p/cm²]	Energy [MeV]	TID [krad]	DDD [TeV/g]
4		$9{,}10 \cdot 10^{10}$	21	30,5	608,1
5	1	$1{,}80 \cdot 10^{10}$	21	5,6	120,3
	2	$5{,}63 \cdot 10^{10}$	21	17,5	376,2
10	1	$2{,}52 \cdot 10^{10}$	60	3,5	101,4
	2	$5{,}04 \cdot 10^{10}$	60	6,9	202,8
	3	$7{,}56 \cdot 10^{10}$	60	10,4	304,2
15		$5{,}63 \cdot 10^{10}$	32,1	12,5	303,6

Displacement Damage Effect

- Displacement Damage is the result of energetic particles displacing atoms from their lattice structure
- As a consequence new energy levels are introduced in the mid-gap
- Increased Dark Count Rate in SPAD devices

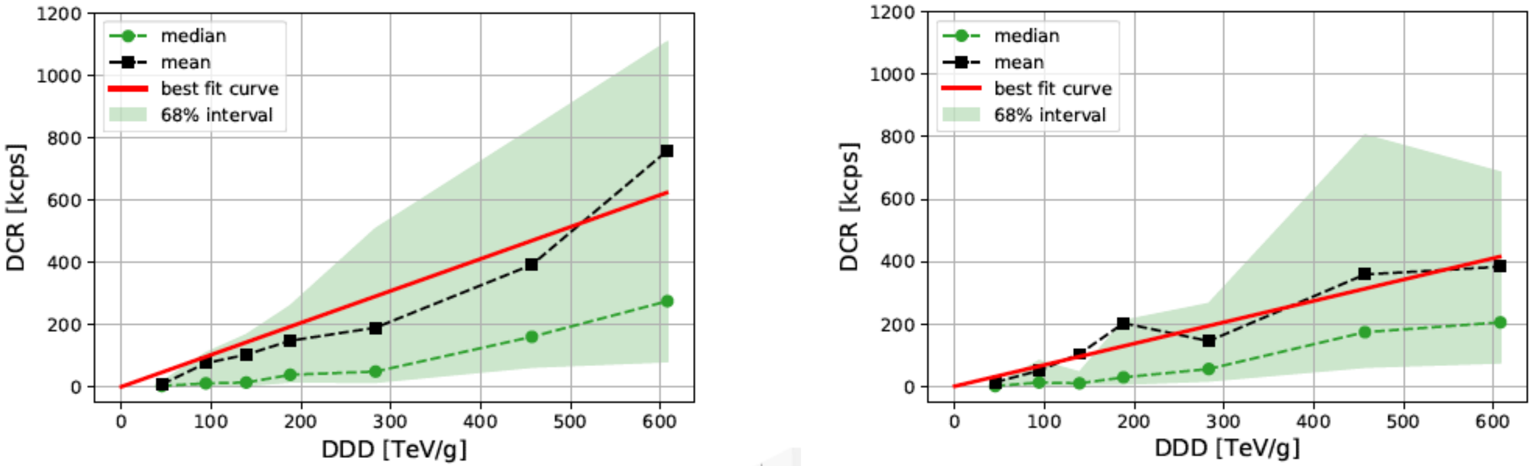


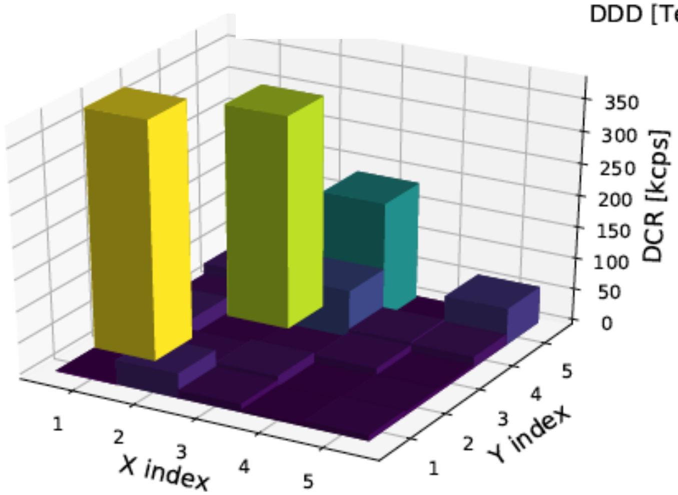


Displacement Damage effect on DCR

- DCR increases up to two order of magnitude at maximum dose delivered
- No significative change has been observed to the breakdown voltage

DCR increase in 10×10 μm^2 SPADs

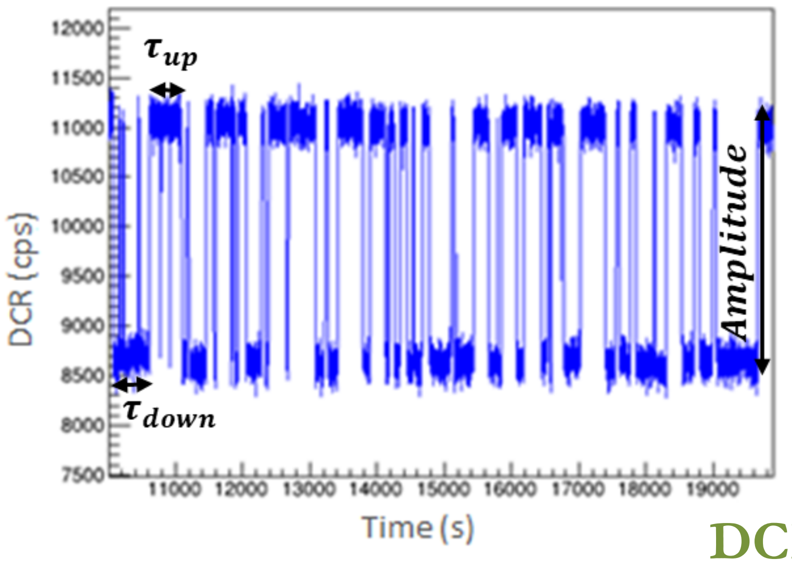


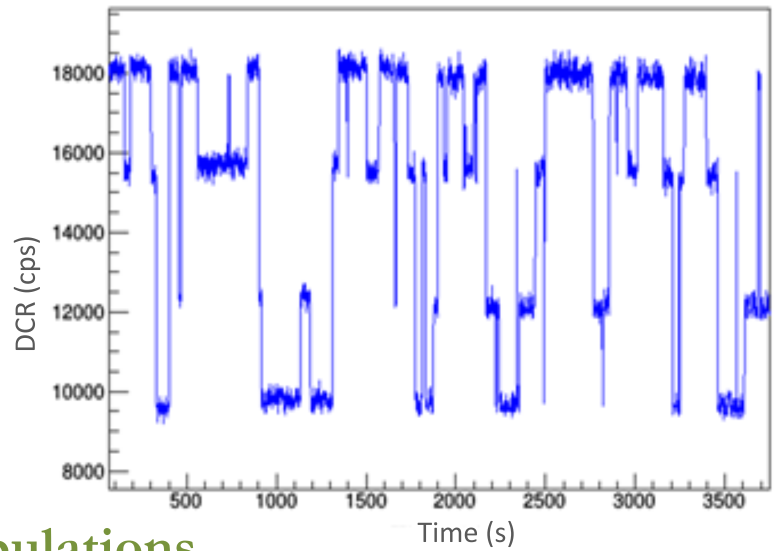


DCR in 5×5 matrix
at 98 TeV/g

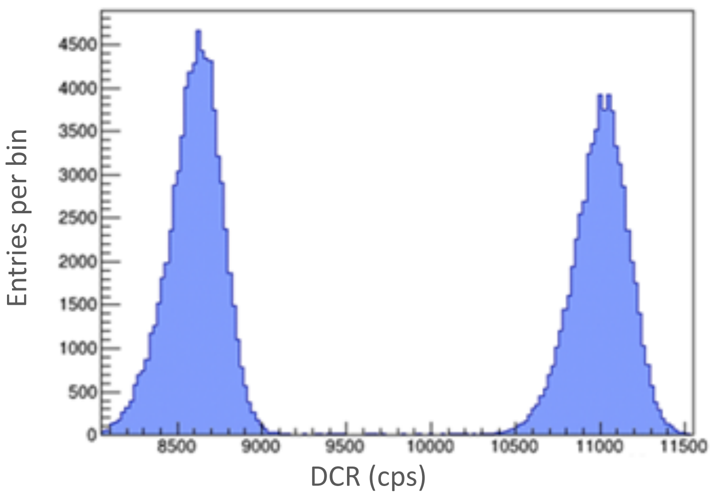
Random Telegraph Signal

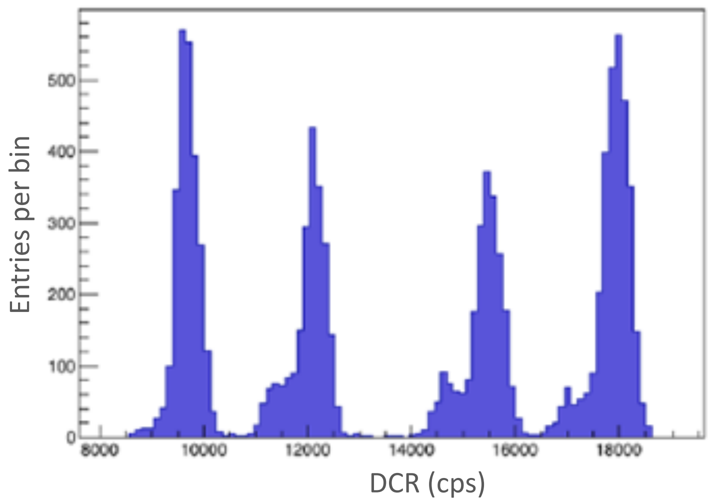
Discrete fluctuations of the DCR between two or more levels have been observed during long observation times





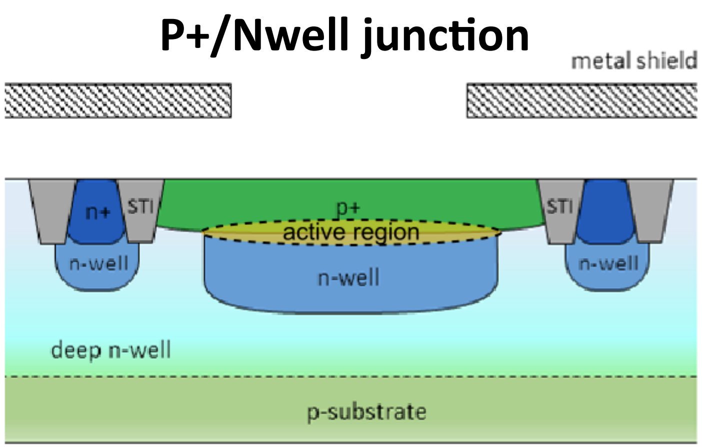
DCR populations

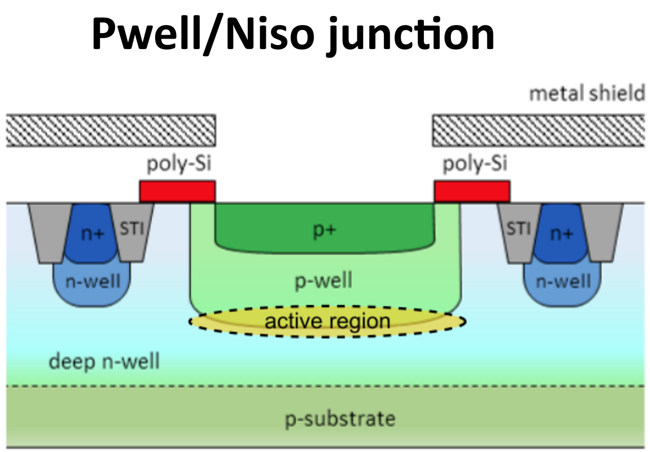




RTS behavior absent after gamma irradiation

RTS Pixels Classification



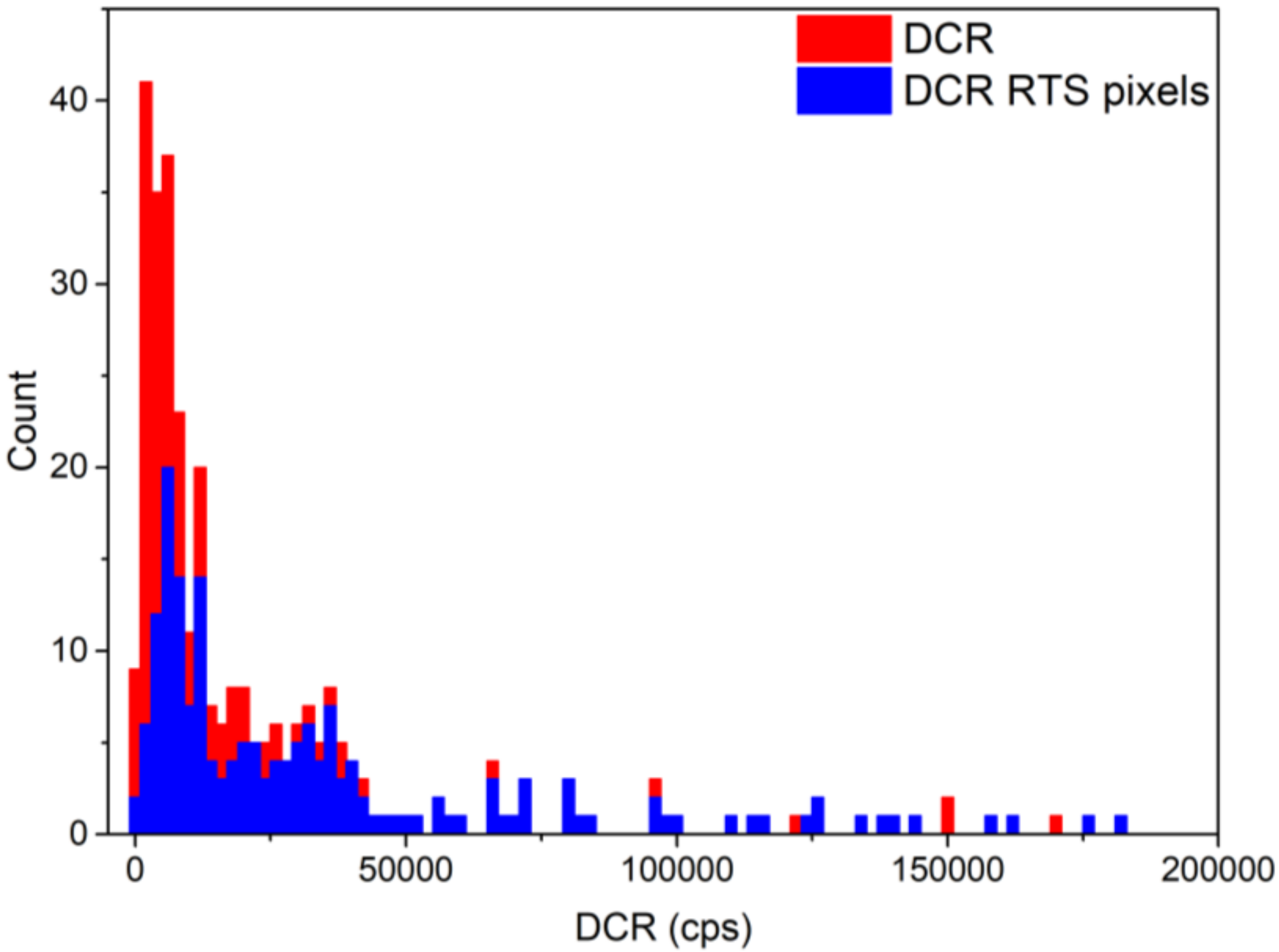


Layout	Analysed SPADs	RTS pixels	2 levels	3 levels	4 levels	≥5 levels	RTS fraction	DDD (TeV/g)
PN	118	65	18	10	10	27	55%	115
PN	124	80	31	11	5	33	65%	304
PN	139	118	17	11	8	82	85%	376
PWNISO	334	131	34	9	13	75	39%	115
PWNISO	334	190	51	19	16	104	57%	304
PWNISO	321	186	34	15	8	129	58%	376

Higher RTS occurence probability in PN junction

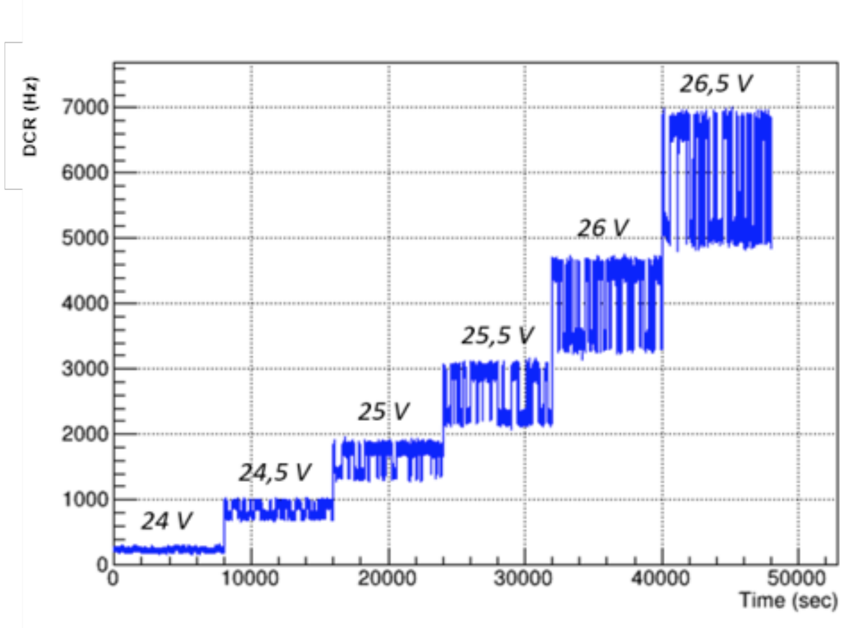
- **Higher doping concentration in PN junction → Higher electric field**

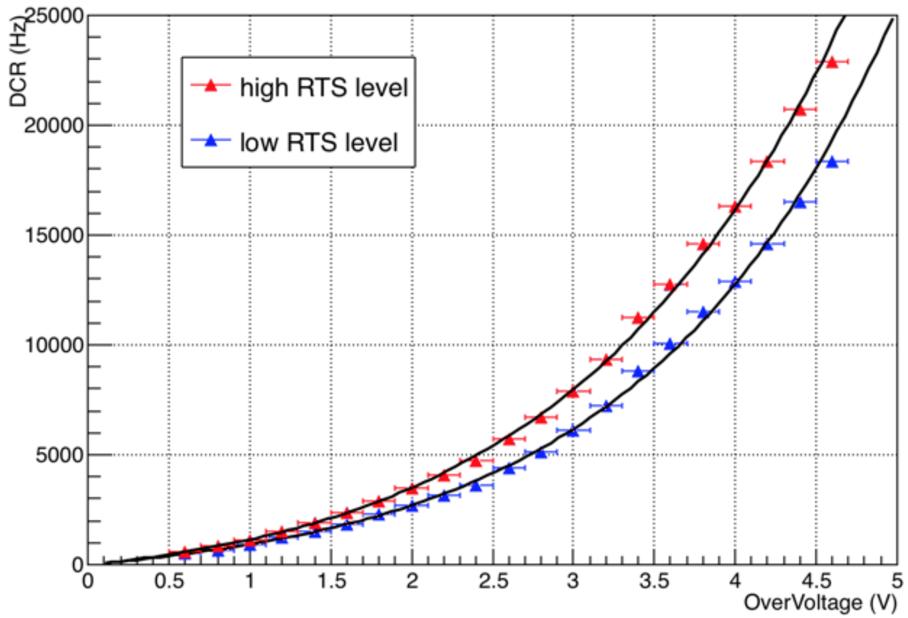
RTS vs DCR



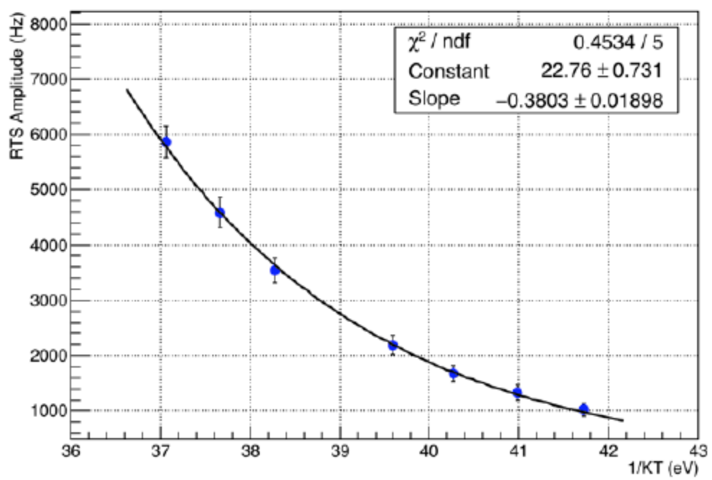
SPADs with high DCR have in most of cases also RTS behaviour

RTS amplitude





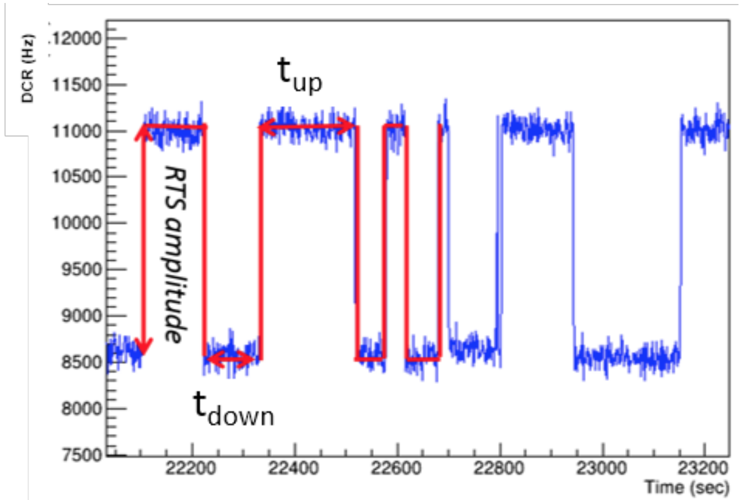
RTS amplitude vs. Temp

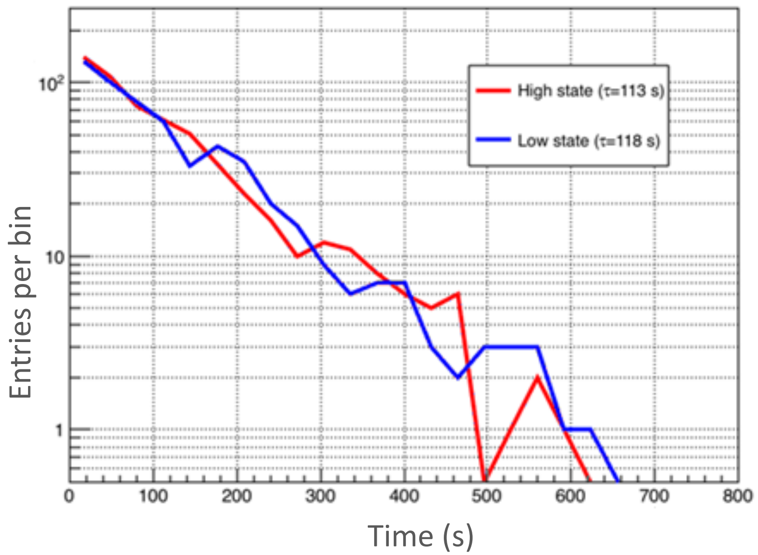


RTS amplitudes:

- increases with the overvoltage
- decreases by decreasing temperature

RTS time constant

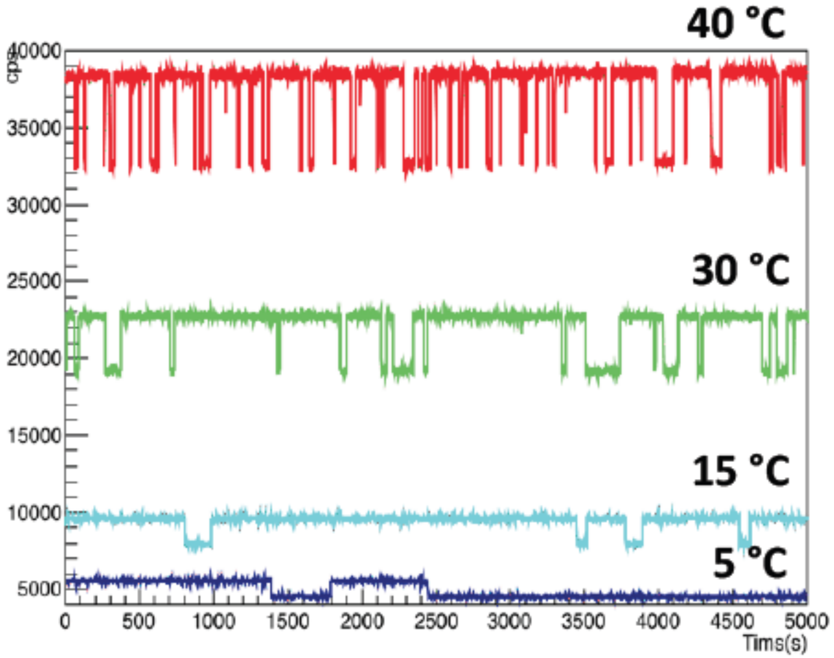




- The number of DCR switching in a fixed time interval follows a Poisson distribution for random switching events.
- As a consequence times between RTS transitions are exponentially distributed

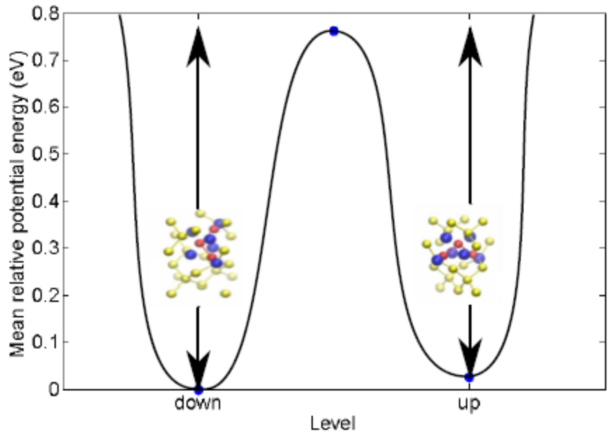
$$P_{switch}(t) = \frac{1}{\tau}\exp(-t/\tau)$$

RTS vs Temperature

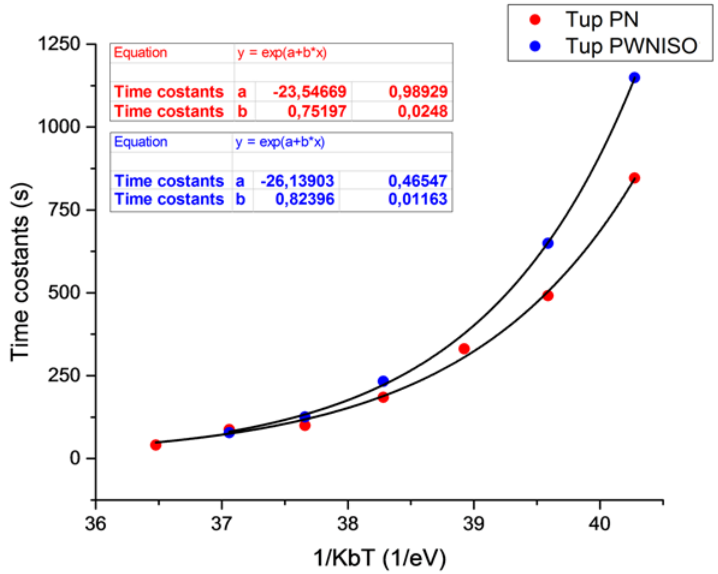


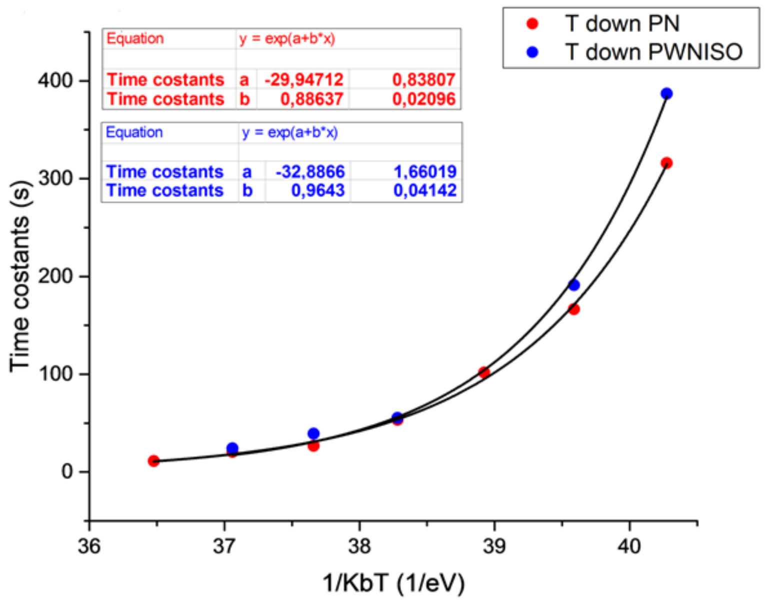
- The DCR switching probability increases with temperature
- RTS amplitude also increases with temperature

- RTS observed in SPADs is correlated with bulk damage: creation of meta-stable states (as already observed for CCD and CMOS imagers)
- Type of defects introduced by proton irradiation that can exist in two or more stable configurations
- It is possible that there is a potential barrier to switch from one configuration to another: for this reason the phenomenon depends on the temperature



Time Constants vs Temperature





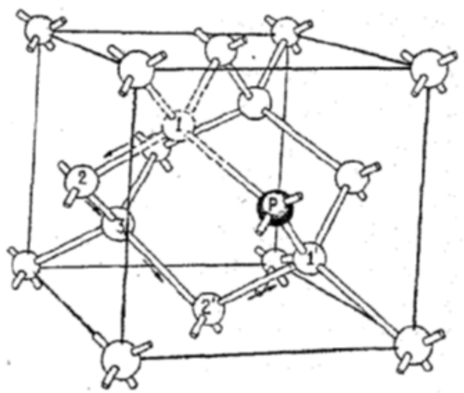
$$\frac{1}{\tau} = C\exp(-E_{act}/KT)$$

Time constants τ_{up} τ_{down} follow exponential distribution

RTS: a possible explanation

Pixel#	$E_{act} - \tau_{up}$	$E_{act} - \tau_{down}$
	PN	
1	0.75±0.02	0.89±0.02
2	0.70±0.02	0.62±0.02
3	0.88±0.03	0.85±0.05
4	0.85±0.02	0.89±0.05
Avg.	**0.80±0.02**	**0.81±0.04**

Pixel#	$E_{act} - \tau_{up}$	$E_{act} - \tau_{down}$
	PWNISO	
1	0.82±0.01	0.96±0.04
2	0.82±0.08	1.27±0.10
3	0.78±0.03	0.86±0.01
4	1.03±0.01	1.06±0.07
Avg.	**0.86±0.03**	**1.04±0.06**



- In silicon device doped with Phosphorus element the complex defect Phosphorus-Vacancy (PV) could be generated
- This complex defect has a dipole momentum due to an extra positive charge on the P atom compensated by an electron orbiting around vacancy
- In a PV complex a vacancy can occupy one of 4 Si atoms surrounding the P atom, the vacancy position can change, this implies a change on the PV dipole axis
- A calculation on the kinetics of the Phosphorus-Vacancy re-orientation gives a predictions of the presence of two energetic levels with a time constant activation energy of 0.93 eV*
- A PV defect anneals at 140°C

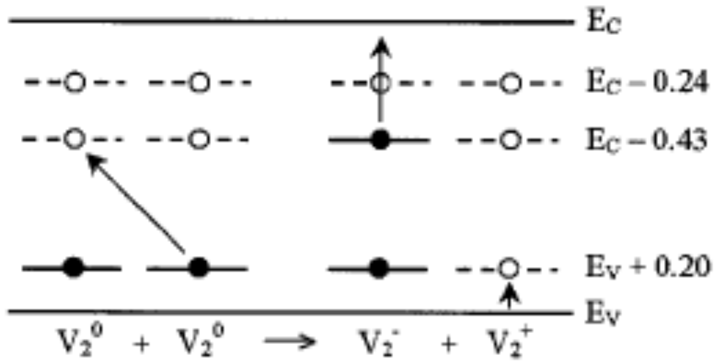
***[G. D. Watkins and J. W. Corbett, 1964; H. Hopkins, G.R. Hopkinson, 1995, T. Nuns, 2007]**

Di-Vacancy Clusters

- Such defects can exist in four charge states (+, 0,-,2-) and with three energy levels between conduction and valence band
- Neutral di-vacancy (most abundant) can give rise to a mechanism called "intercenter trasfer" which result in an increase of generation rate:

$$V_2^{\,0} + V_2^{\,0} \longrightarrow V_2^{\,+} + V_2^{\,-}$$

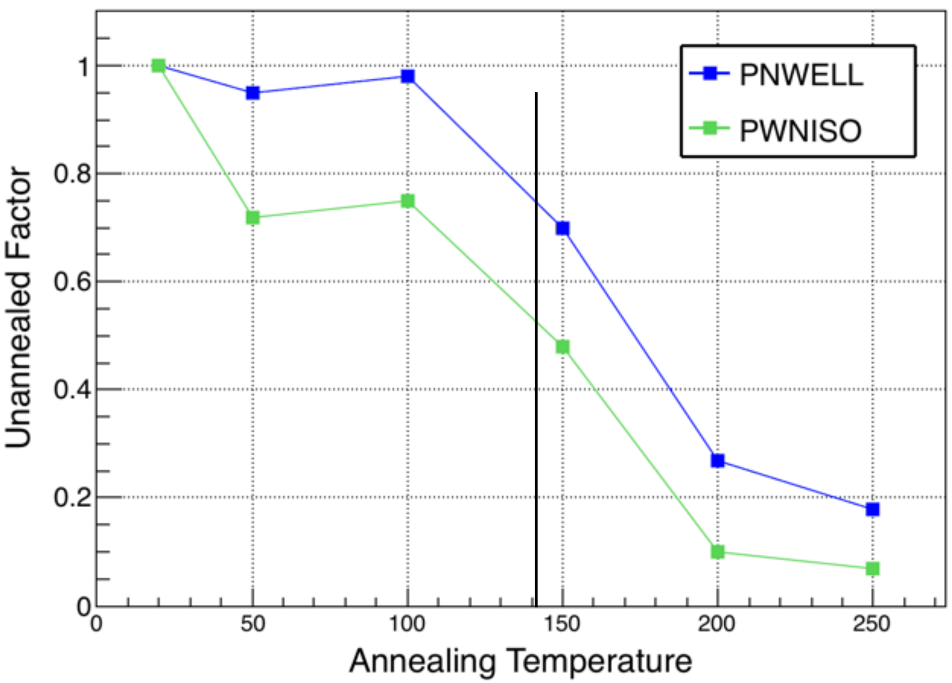
- Movement of divacancy could create "intercenter transfer" mechanism and
- This could be at origin of RTS
- A di-vacancy defect anneals at 270°C



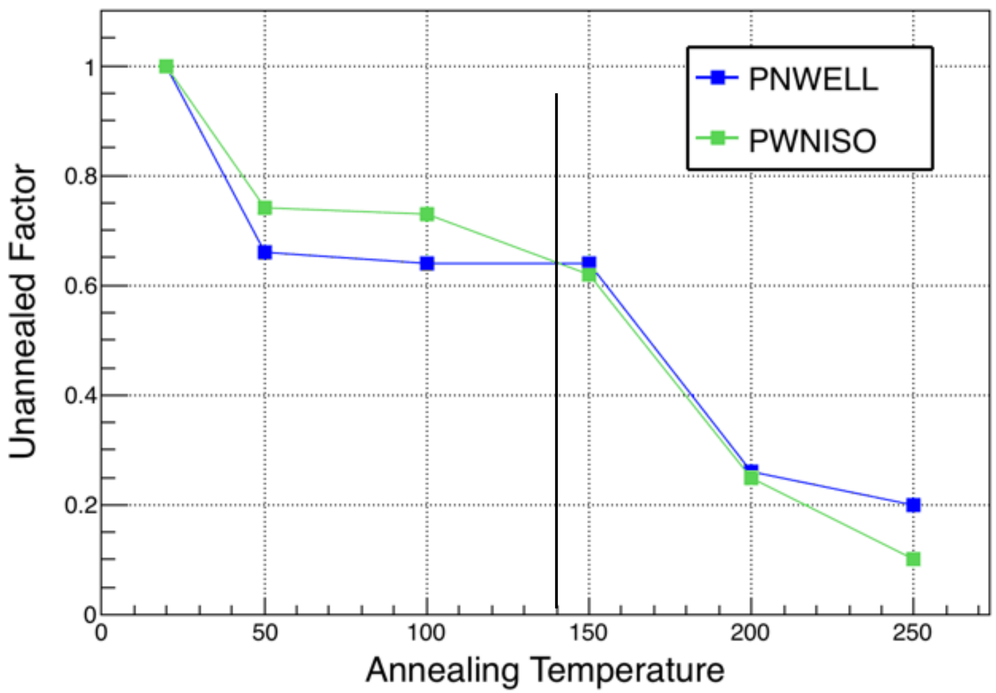
Annealing

- The annealing procedure is an useful tool to investigate the defects responsible for DCR and RTS
- Irradiated SPAD behavior has been studied after different annealing temperatures between di annealing 50°C and 250°C
- PV complex defects are expected to anneal at 140°C, di-vacancies at 270°C

DCR

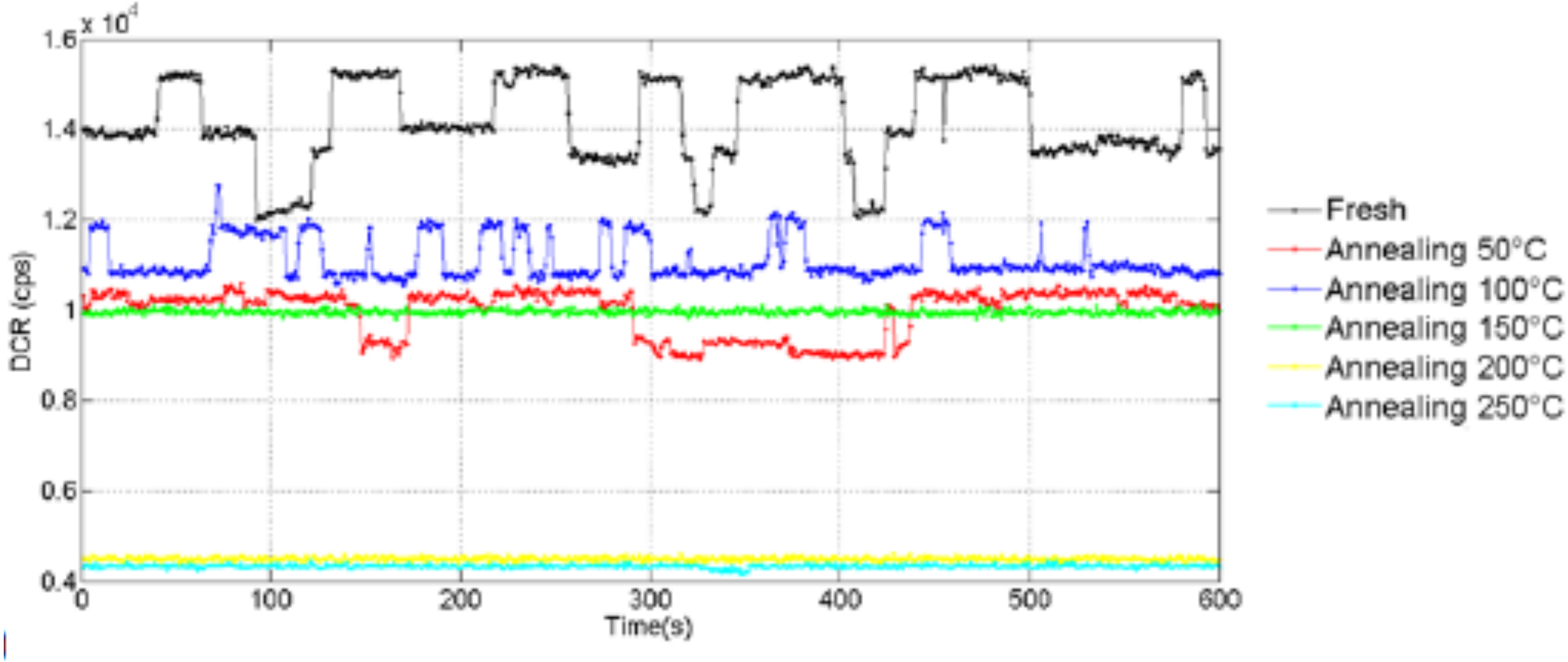


RTS



P-V could be considered one of the radiation induced type defect, but cluster of intrinsic defects should be also considered to participate [J.W. Palko, J.R. Srour, 2008]

Annealing(2)



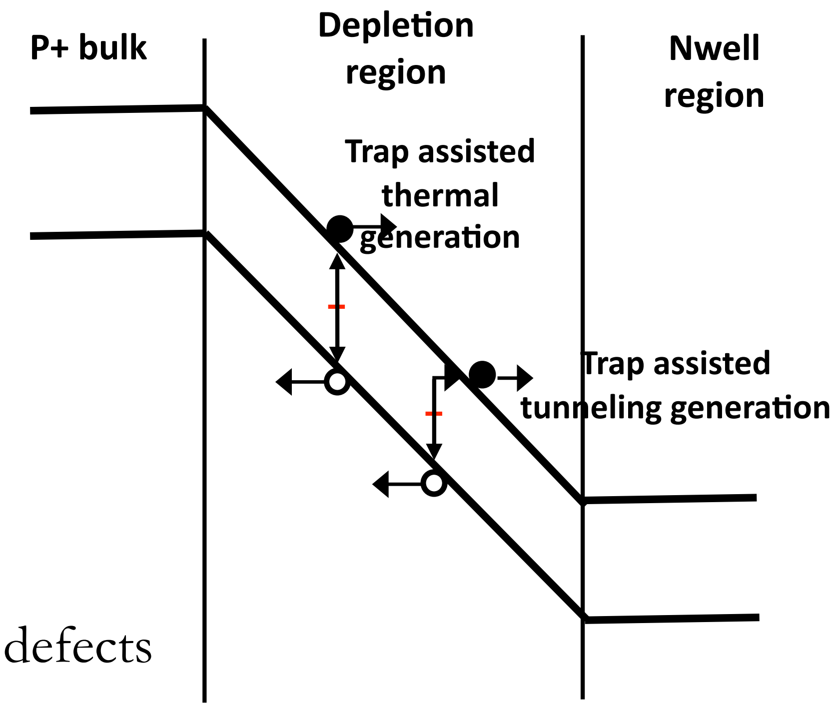
Annealing procedure trasforms multi-level RTS in lower level RTS and in less frequent RTS before to completely disappear

Conclusions

- We analyzed the dark count behavior of two different SPAD layouts in a 150-nm CMOS process
- One of them present increased DCR from tunneling contribution due to higher doping profile
- This layout after proton irradiation present higher RTS occurrence
- RTS characterization and annealing procedure indicate the PV complex defect as a possible responsible for RTS
- In future we will analyze SPAD with lower phosphorus doping and As-doping to further investigate the RTS origin

Backup slides

Dark Count Rate



Dark Count Rate increase depends on bandgap energy levels due to:

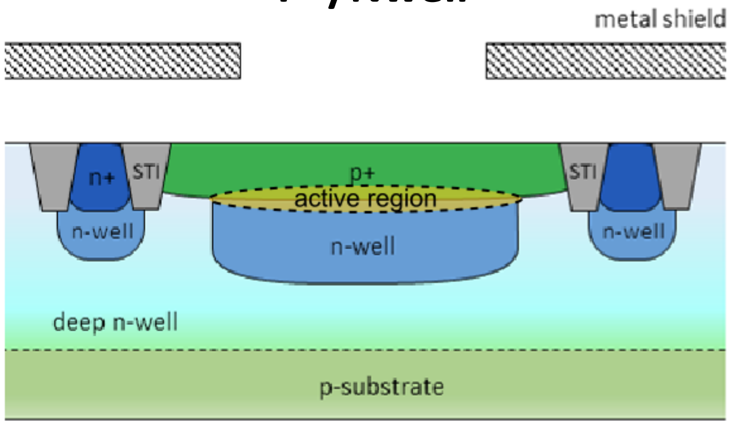
1. **Fabrication process**: impurities and crystal defects
2. **Irradiation environment**: radiation induced defects add energy levels between valence and conduction band

The energy levels cause the generation of carriers in depletion region through:

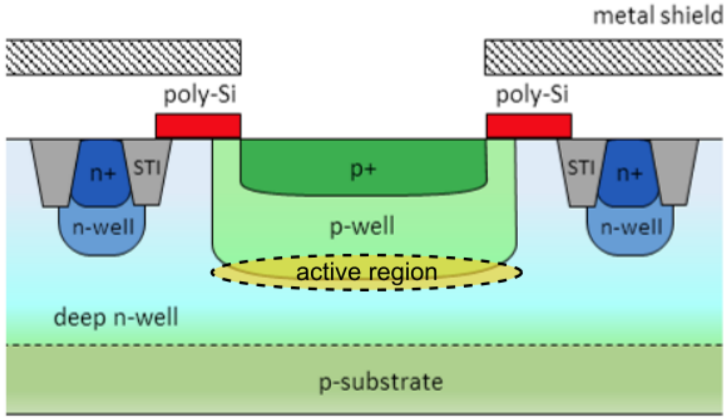
- **Shockley–Read–Hall generation**
- **Tunneling**

SPAD Layouts

P+/Nwell



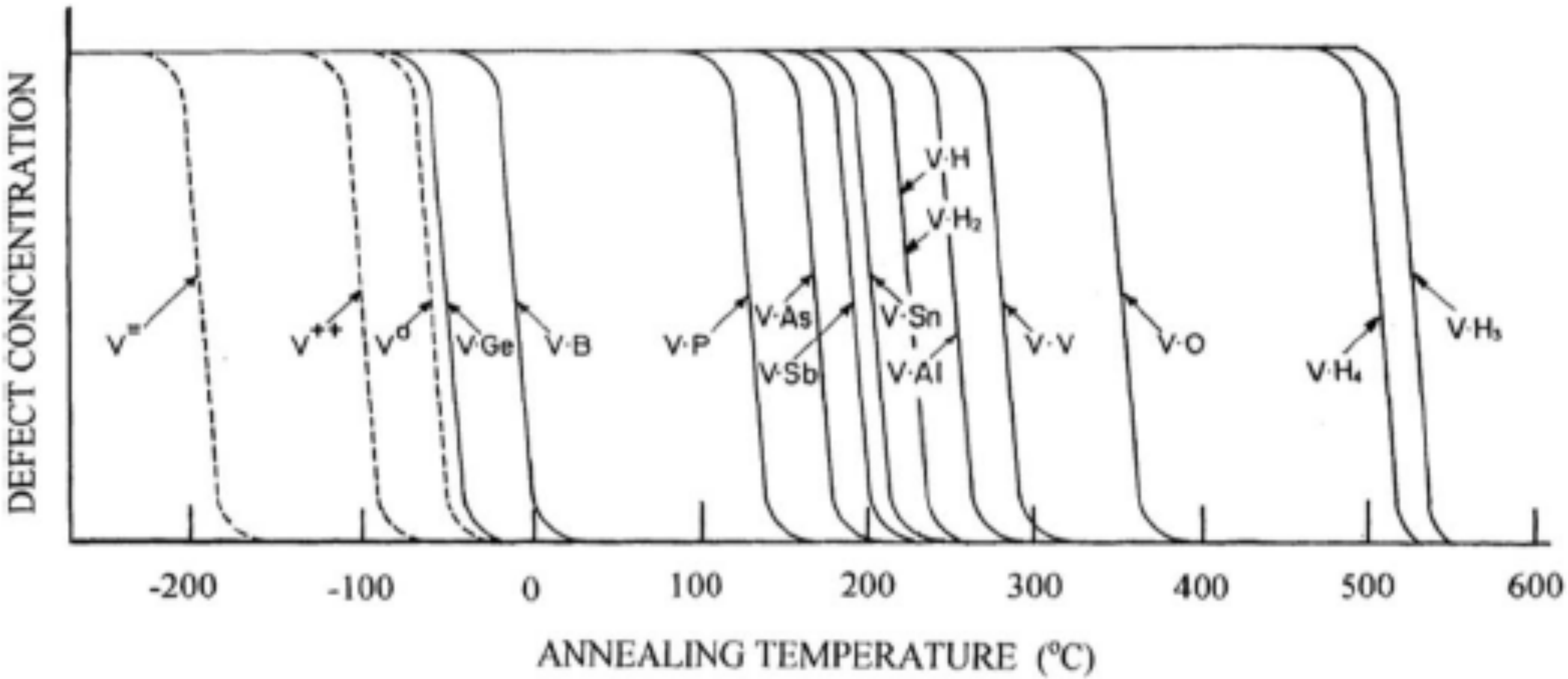
Pwell/Niso



- P+/Nwell junction with a guard ring obtained by blocking Pwell and Nwell at borders with a deep Nwell implantation: low doped ring obtained avoid premature periphery breakdown

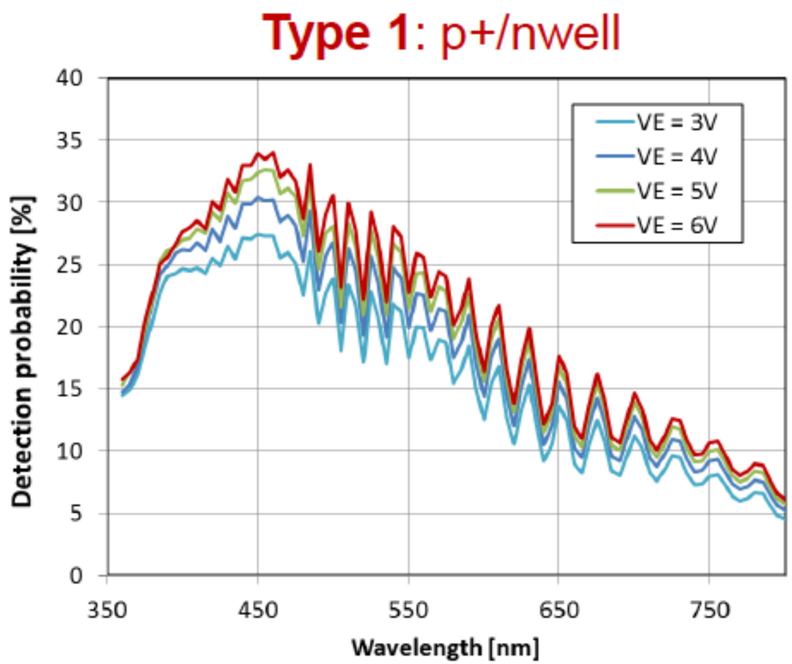
- Pwell/Niso junction. The guard ring is formed by avoiding well implantation at junction periphery. A poly-Si gate blocks p+ implantation avoiding the space charge region to reach the STI.

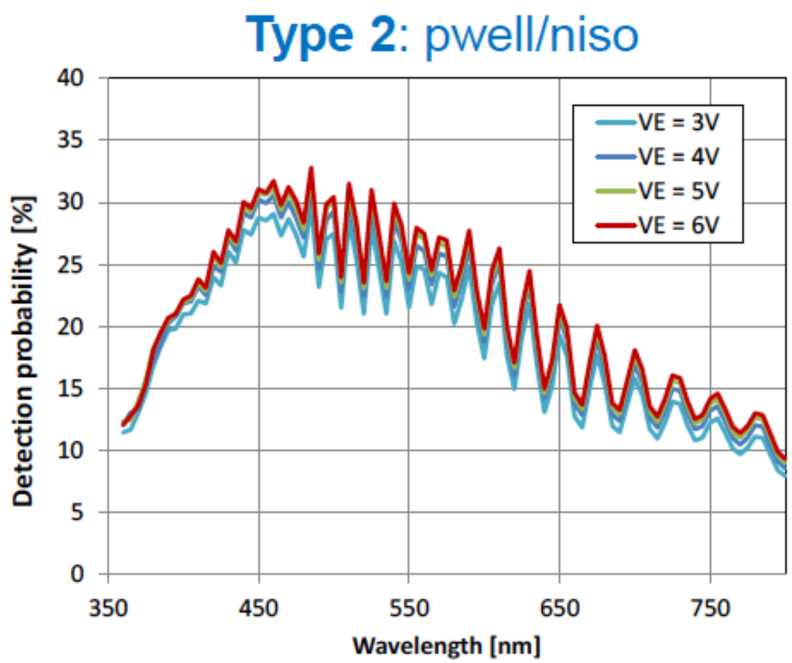
Annealing(2)



DEFECT CONCENTRATION
V·H
V·H₂
V·As
V·Sn
V·P
V·B
V·Ge
V·Sb
V·Al
V·V
V·O
V·H₄
V·H₃
-200
-100
0
100
200
300
400
500
600
ANNEALING TEMPERATURE (°C)

Photon Detection Efficiency

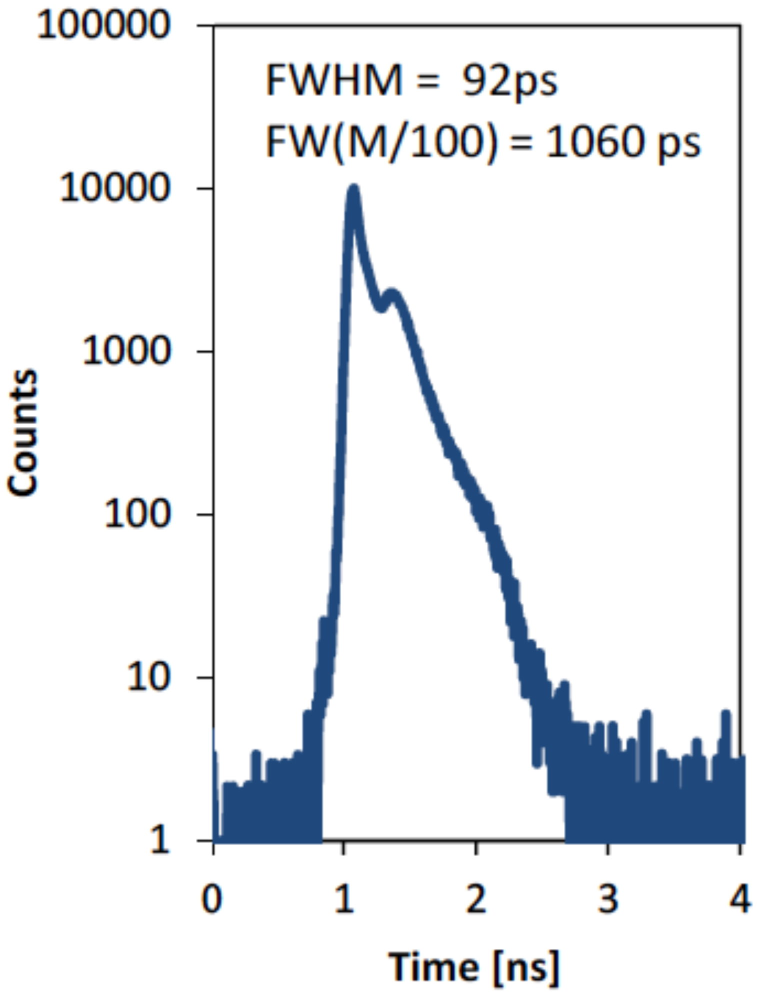




Timing

P+/Nwell junction

Type 1: **60ps FWHM**



Pwell/Niso junction

Type 2: **170ps FWHM**