FERS: a distributed Front End Readout System for multi-detector arrays

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SiPM workshop: from fundamental research to industrial applications – Bari, 2-4 Oct. 2019
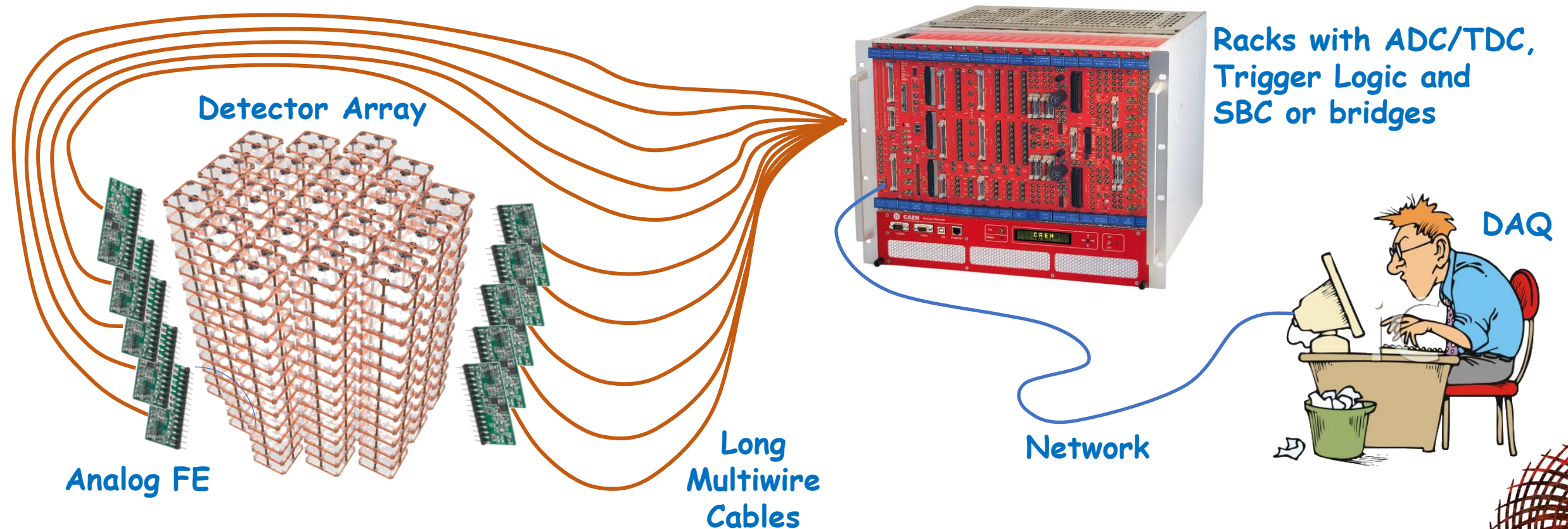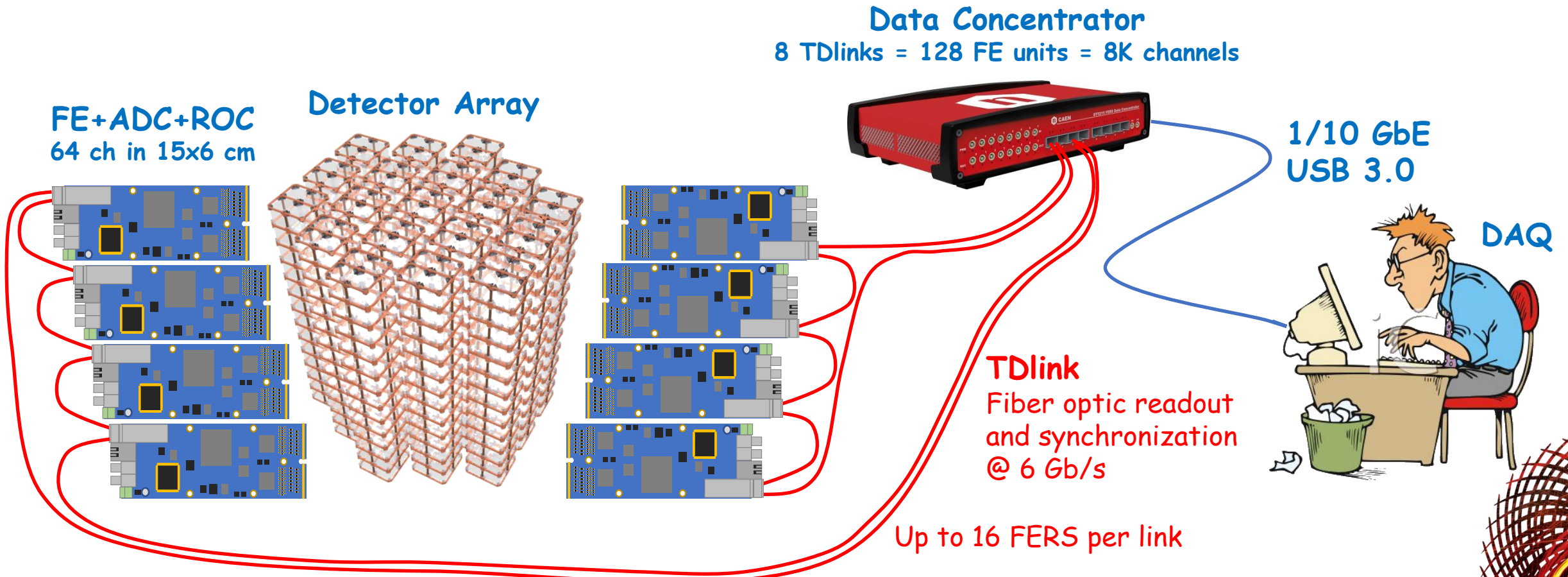
Traditional Readout System

- Front End Preamplifiers close to the detectors

- Long cables bring analog signals to readout electronics (ADC, TDC, etc.)

- A/D conversion, online data processing and communication concentrated in racks

Detector Array

Analog FE

Long Multiwire Cables

Racks with ADC/TDC, Trigger Logic and SBC or bridges

DAQ

**Network**

Distributed Front End Readout System

- Front End Preamplifiers, A/D conversion and data processing/readout in small **FE card** (typ. 64 ch)

- **TDlink**: single optical ring connection for synchronization, readout and slow control

- Data Concentrator: provides global synch, trigger logic, event data building and storage

- Easy scalability to thousands channels: up to 8192 channels per Data Concentrator

- Less cable cost, noise pickup, signal attenuation. Fast deployment

Data Concentrator
8 TDlinks = 128 FE units = 8K channels

FE+ADC+ROC
64 ch in 15x6 cm

Detector Array

1/10 GbE
USB 3.0

DAQ

TDlink
Fiber optic readout
and synchronization
@ 6 Gb/s

Up to 16 FERS per link

- **A52xx**: single card housing Front End ASICs, ADC and/or TDC, FPGA, I/Os and Interfaces

- Detector Bias included in some models (e.g. A5202 for SiPM)

- A new line of FE and readout electronics for:
  - SiPM
  - PMTs and MA-PMTs
  - Gas Detector, wire chambers
  - GEM
  - Micromegas
  - Silicon Strip Detectors
  - Neutron Detectors (Position Sense Tubes, He3 detectors)
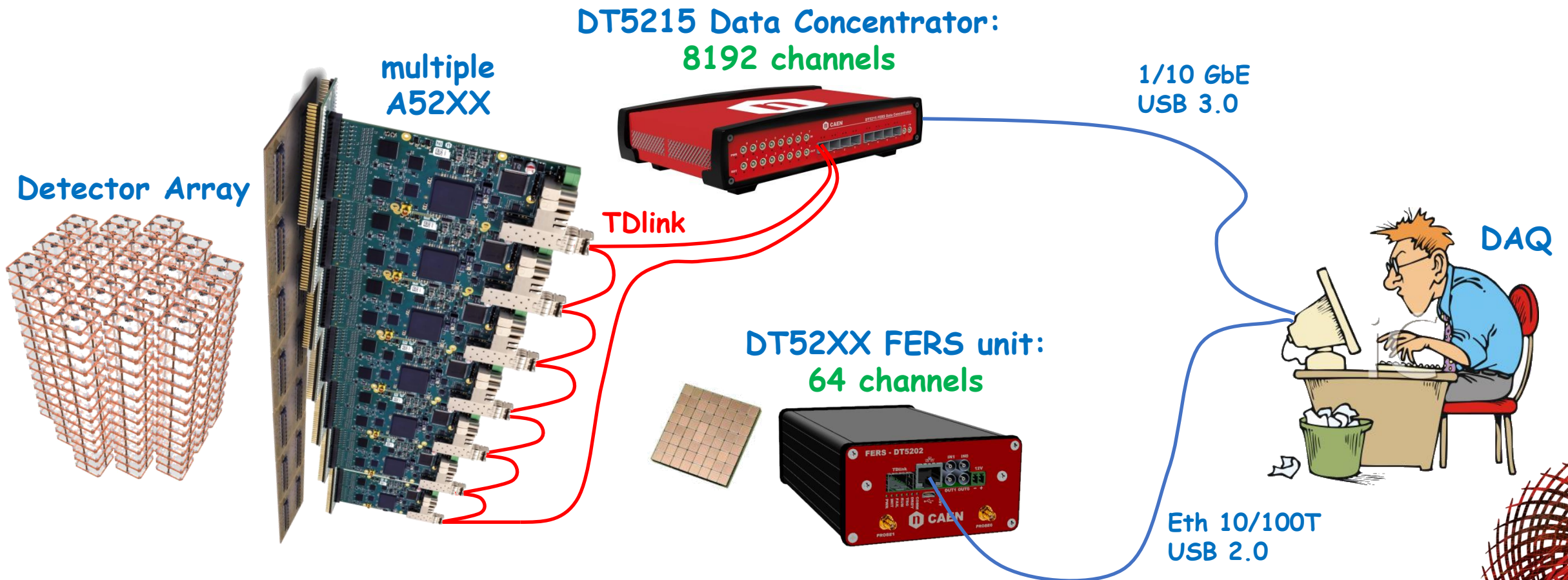 - Segmented HPGe detectors

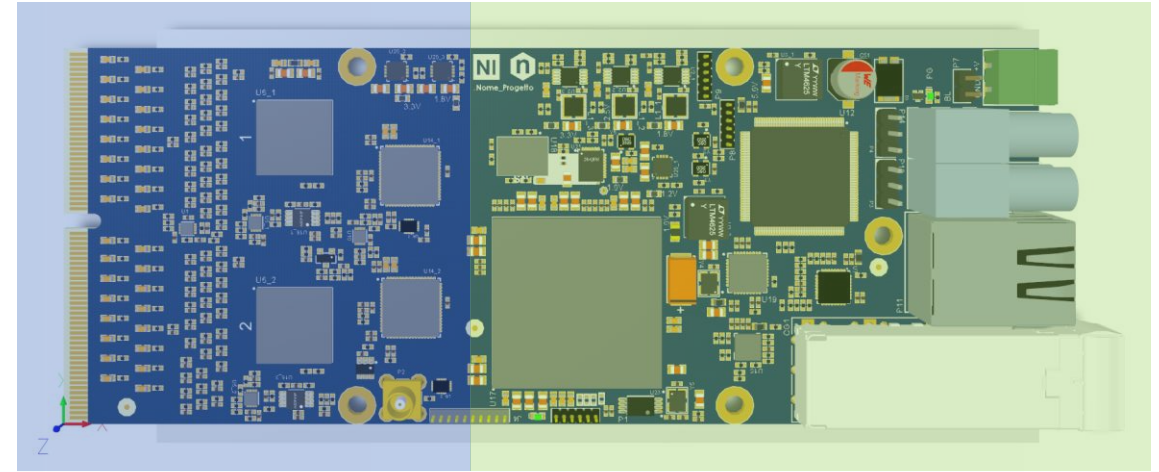- **Same Infrastructure for different Front Ends**
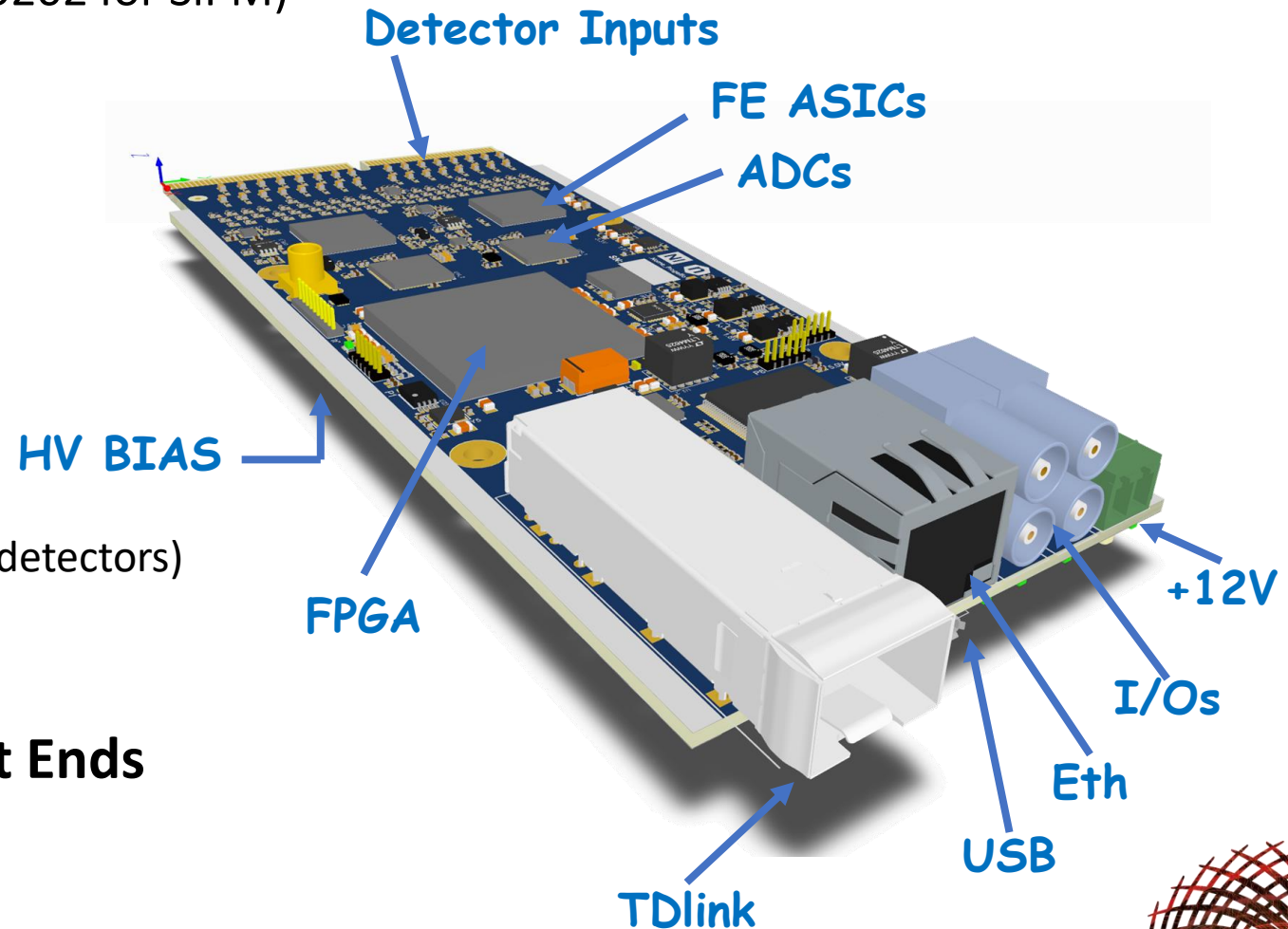
From evaluation to large experiments

- One FERS unit can be used stand-alone in a desktop form factor

- Direct connection to PC (USB or Ethernet). No additional hardware required!

- Same user interface (SW, libraries, etc.), same hardware and performances

- Naked FERS units can be easily arranged in backplanes/mechanics to build large systems

multiple A52XX

DT5215 Data Concentrator:
8192 channels

1/10 GbE
USB 3.0

Detector Array

TDlink

DAQ

DT52XX FERS unit:
64 channels

Eth 10/100T
USB 2.0

FERS flavors (future plans)

DETECTOR SPECIFIC   **COMMON INFRASTRUCTURE**

- **Citiroc:** SiPM Spectroscopy (Weeroc)

- **Petiroc:** SiPM timing (Weeroc)

- **Maroc:** MA-PMT (Weeroc)

- **Skiroc:** Silicon Detector (Weeroc)

- **Gemroc:** Gem Detector (Weeroc)

- **VMM3**: Micromegas, Gem (BNL)

- **Sampic:** 10 GS/s SCA waveform digitizer and ps TDC (LaL)

- **AARDVARC / ASOC:** 13 GS/s and 3.2 GS/s SCA waveform digitizer and ps TDC (Nalu Scientific)

- **picoTDC**: 3/5 ps TDC (CERN)

- **Hybrid Solutions**: FE in separate box, plug-in FERS with flash ADCs (e.g. 16 channel, 100 MS/s, 14 bit)

  - **A1442:** 16/32 channel preamp for Silicon Strip Detectors
  - **PADIFF**: 32 channel preamp for Neutron Detector
 - **Detached ASIC** boards for **cryogenic** applications

A5202: 64 channel SiPM readout (Citiroc 1A)

- Based on two ASICs Citiroc 1A (Weeroc): 64 channel SiPM readout

- Embedded HV bias (20-85V) with temperature feedback. Individual HV adjust per channel

- Programmable gain and shaping time for High Res PHA (Multiplexed A/D, max Trg Rate = 100 Kcps)

- Individual discriminator thresholds: down to 1/3 p.e.

- Discriminator outputs for high rate counting (20 Mcps), Time stamping (0.5 ns) and ToT (low res PHA)

- 50 ps TDC for high resolution time stamping of OR trigger (to an external time reference signal)

- Acquisition modes: photon counting, spectroscopy mode (PHA), list mode (channel ID + Tstamp + ToT)
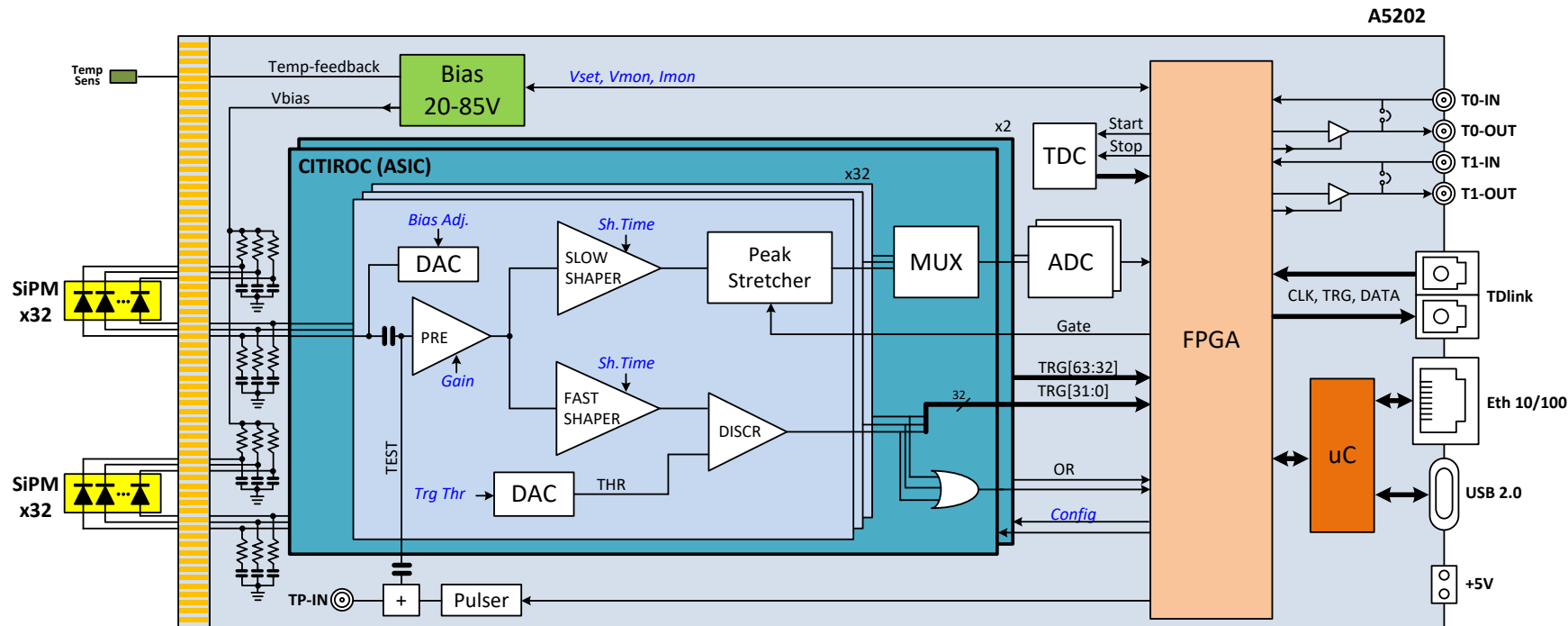
- **Spectroscopy Mode (PHA)**:
  - A/D conversion of the pulse height (preamp + shaper + peak hold + mux + 14 bit ADC)
  - Common trigger (int. or ext.)
  - Zero suppression with programmable thresholds (read fired channels only)
  - Max trigger rate = 100 KHz (dead time = ~10 μs per trigger)

- **Counting Mode** (e.g. photon counting in SiPMs):
  - Counters fed by fast discriminator signals
  - Simultaneous latched at programmable time frames and saved to memory (MCS mode)
  - No dead time in counting, up to ~20 Mcps/ch

- **Timing Mode** (List of Tstamps and/or Time over Threshold):
  - Independent hit recording: channel ID + timing (0.5 ns resolution)
  - Common start or common stop (T-ref signal from LEMO input)
  - Gating mode (coincidence with external gate)
  - Optionally, **ToT** (0.5 ns) provided for low resolution PHA: Charge Resolution = 1.5%
  - Max total hit rate = ~50 Mcps/board

- **Waveform Mode**:
  - Signal inspection: mux output waveform and control signals
 - Not used for physics (in A5202), only for debugging

Readout Modes

- **Common Trigger Mode**

  - **FERS units**: generate a trigger request (typically OR of channel discriminators)

  - **Data Concentrators**: receive and combine requests from all units and generate the **Global Trigger**

  - Triggers produce formatted data packets in the FERS units. Little local data buffering.

  - Data Concentrator reads data fragments belonging to the same event from FERS units (using Tstamp or Trigger-ID)

  - **Event Building** and data reduction takes place in the ARM processor of the Data Concentrator

- **Trigger-less Mode (independent channel acquisition)**

  - **FERS units**: each channel pushes data asynchronously, typically at different rates

  - Data aggregated in small packets in FERS units, then bigger packets in Data Concentrator

  - No trigger and data correlation in HW. Events reconstruction in DAQ.

- ARM processor running **Linux** and local DDR memory available in Data Concentrator

- High throughput data transfer to host computers via 10 GbE or USB 3.0

- Users can run custom routines for data handling in the embedded ARM

Event Building in Concentrator Board
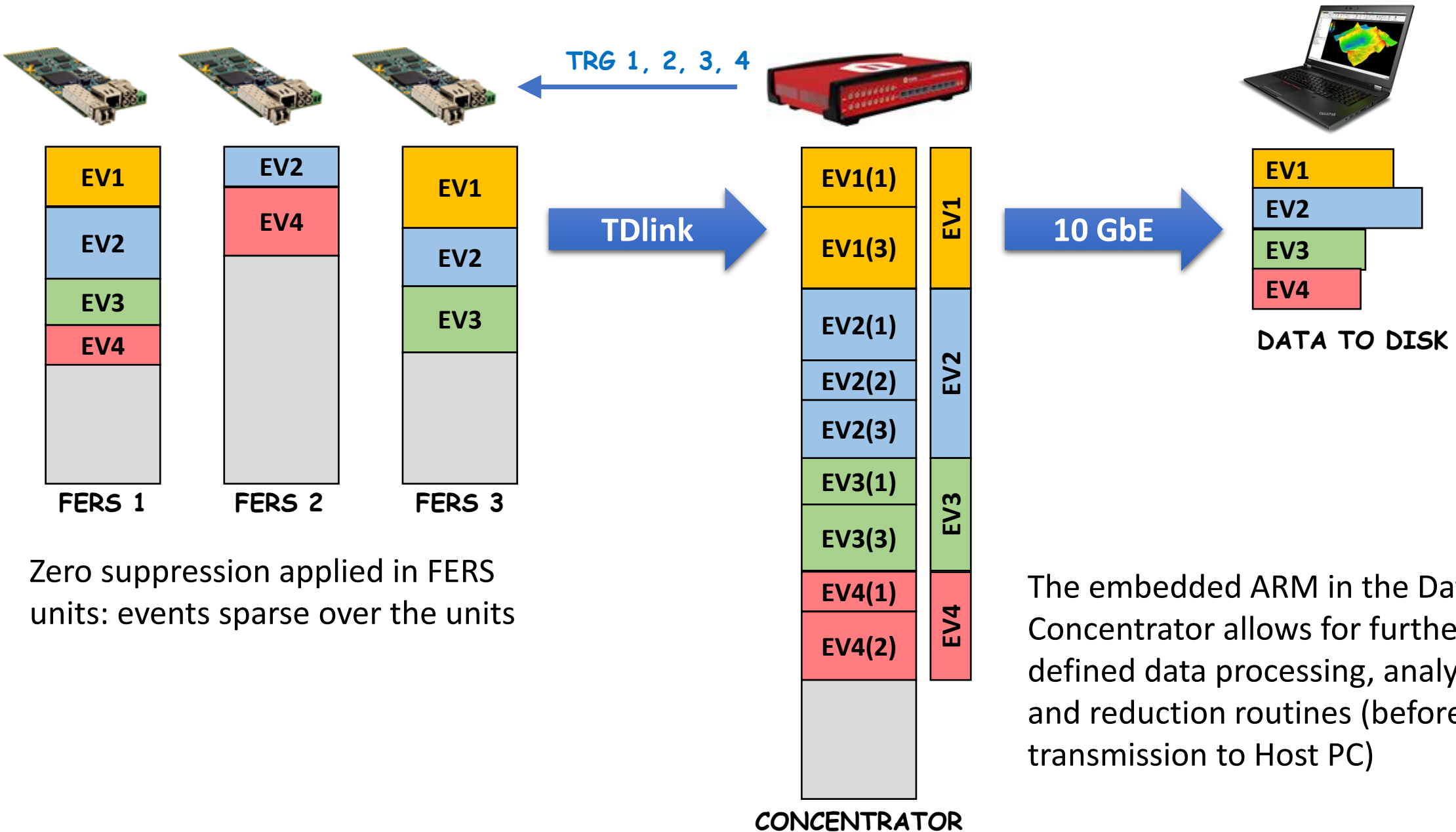
Zero suppression applied in FERS units: events sparse over the units
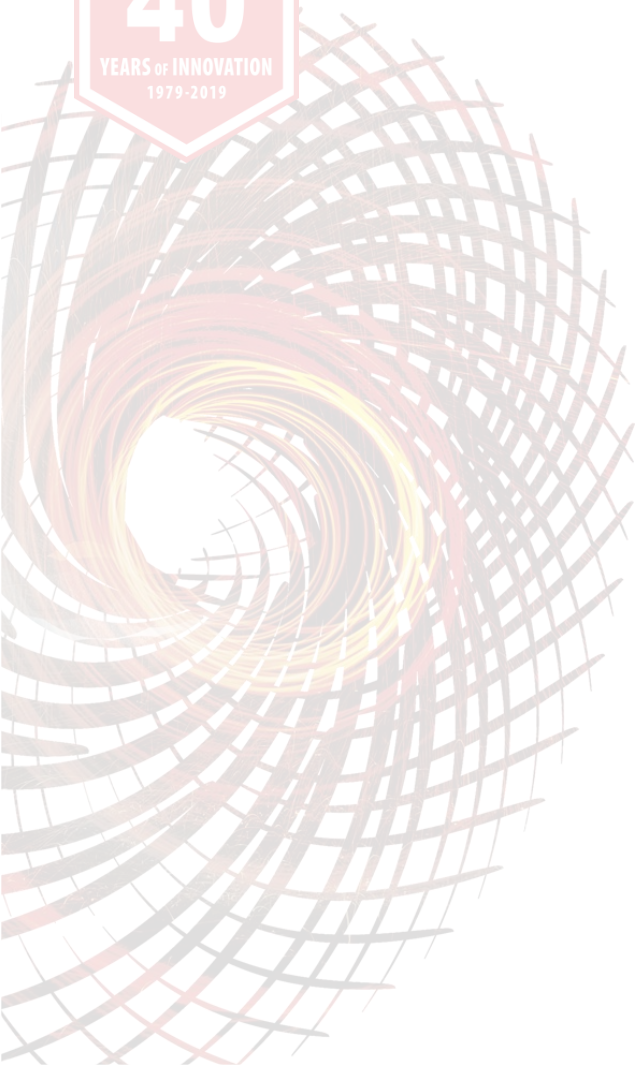
The embedded ARM in the Data Concentrator allows for further user defined data processing, analysis and reduction routines (before data transmission to Host PC)

- A new line of distributed readout electronics for multi-detector arrays is under development

- The FERS is a compact, scalable and versatile readout system

- Easy scaling up from a single desktop evaluation board to a >10K channel system

- Single fiber option ring connection for synchronization, slow control and readout

- 1st member of the family: A5202, 64 channel, SiPM readout module with Citiroc 1A and HV bias. Under test…

- Other FERS units with different Front End electronics coming soon