Padme based DAQ for ReD

Padme DAQ

- Simple DAQ based on CAEN V1742 and A3818 PCIe VME bridge.
- Main author is Emanuele Leonardi from Roma1 (big thanks)
- Available at : https://github.com/PADME-Experiment/padme-fw
- Used as-is, no warranty, limited but precious support from Emanuele
- Currently in production for PADME data acquisition (several hundred acquisition channels)
- Simple enough to be readable by myself (and “almost” all in this room) and solid (little dependencies on third party s/w)

Overview

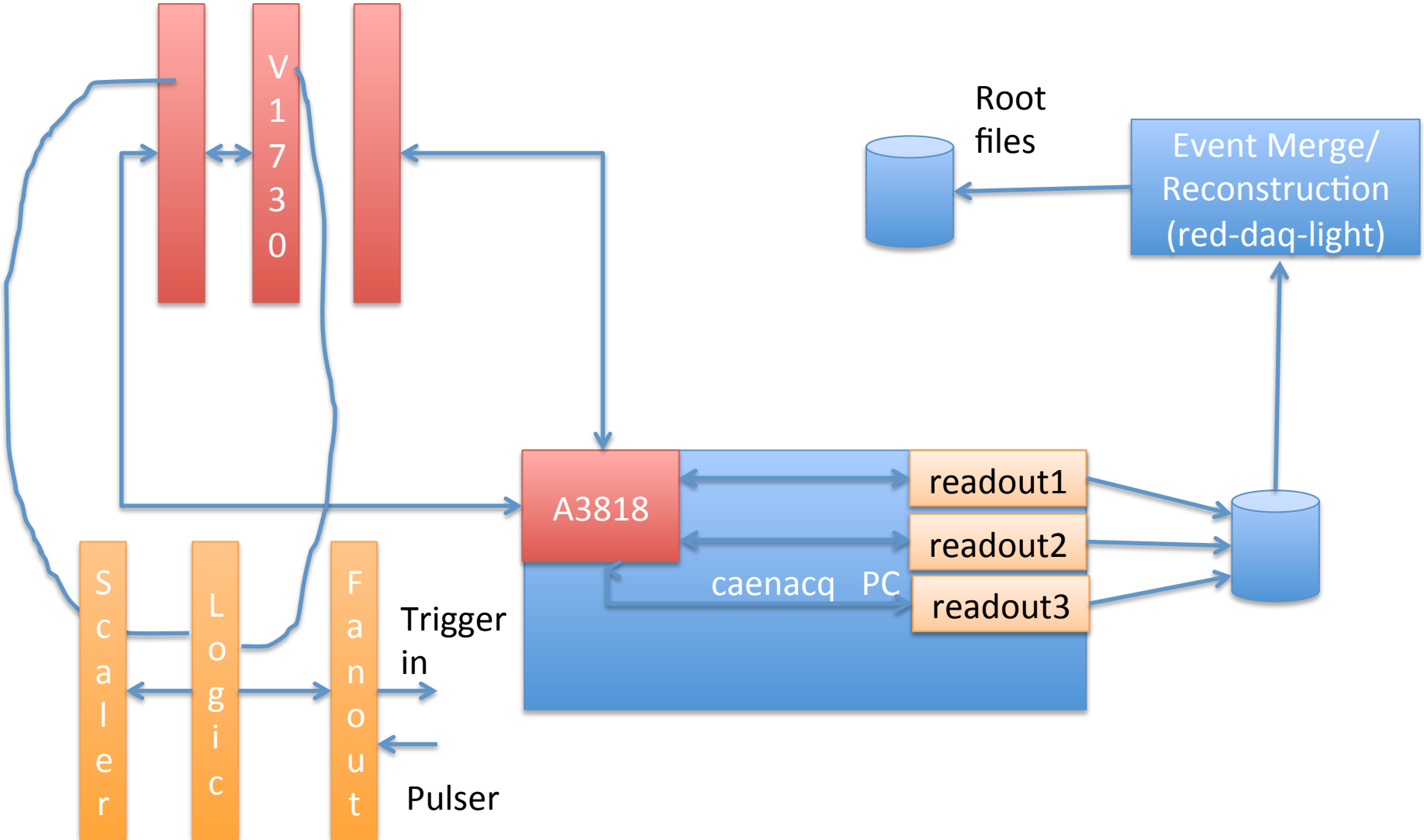
- Different components (DAQ, binary→root conversion, Reconstruction), in addition:
  - A Run control based on tk
  - Board configuration modification also through simple ascii files
  - Interfaced to mysql for run condition database and file/events accounting
  - Event building and reconstruction classes (form the base infrastructure of red-daq-light reconsctruction code)

- Code available on baltig (INFN git hub)

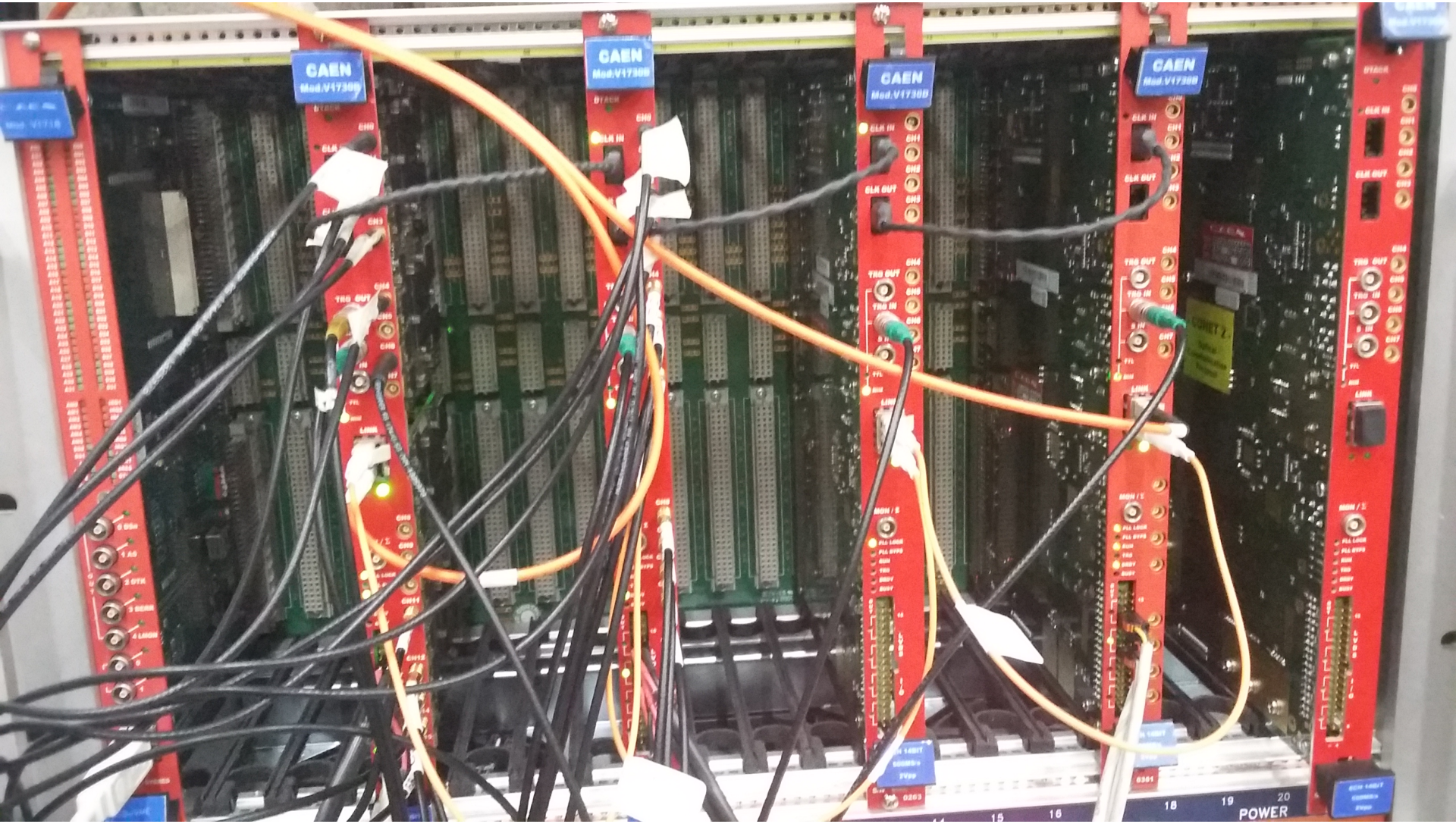
https://baltig.infn.it/rescigno/ReD-DAQ

- Simple installation
- Up to date with Napoli/CT setup

Data Flow


V1730
Root files
Event Merge/ Reconstruction (red-daq-light)
A3818
readout1
readout2
readout3
caenacq PC
Scaler
Logic
Fanout
Trigger in
Pulser

The thing



Data Rates

- Number for LNS runs so far
- On going improvements
  - New 4 channel a3818 interface purchased
  - New DAQ server ordered 16 physical cores, 128 MB ram,
  - 40 TB disc, with RAID0/10 controller

Event Size (double fase)	**4.2 MB**
Max theoretical readout BW	2x80 MB/s
Maximum write speed	~40 MB/s
Maximum trigger rate	~10 Hz

Event Size (double fase)	**4.2 MB**
Max theoretical readout BW	3x80 MB/s
Maximum write speed	Up to x4
Maximum trigger rate	~40 Hz ?

Data Rates (2)

- We don’t have any compression in data
- Test on July data double phase data can be compressed to 30-40% their size
- Can implement this on the fly?

- Require light-weight s/w modifications to both DAQ and red-daq-light

DATA rates(3)

- Zero suppression firmware could be purchased and installed in V1730

ZLE idea

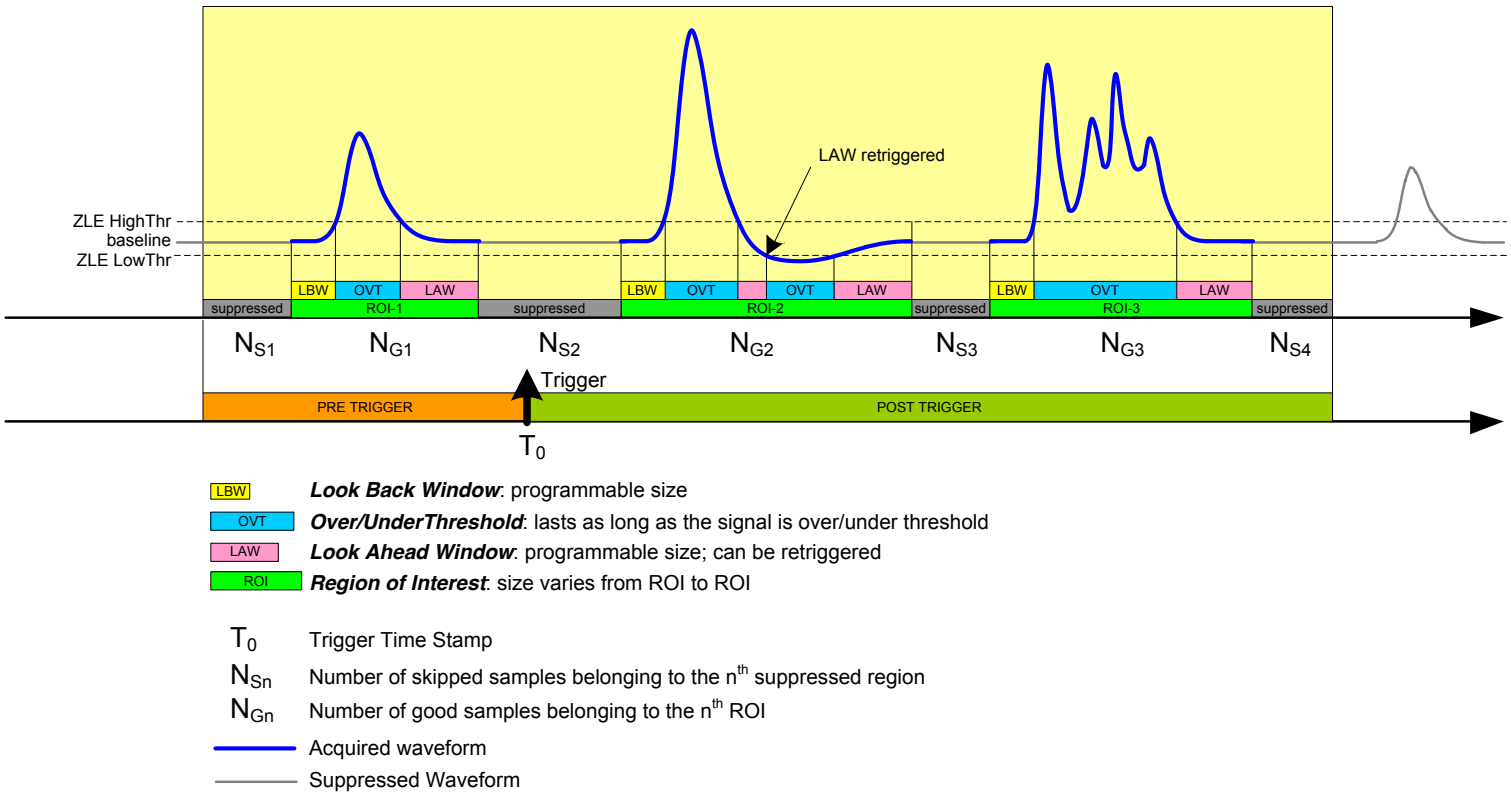


Fig. 2.1: DPP-ZLE*plus* algorithm description

DATA rates(3)

- Zero suppression firmware could be purchased and installed in V1730
  - This would allow to suppress the data below threshold in between S1 and S2, or the largely zero data of silicon and Lsci channel
  - Would allow faster readout through the optical link by an estimated factor >2
  - Data format would change, require s/w modification both in DAQ and in red-daq-light

With ZLE

EVENT DATA FORMAT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
CHANNEL EVENT SIZE																																HEADER
EVENT TRIGGER TIME TAG																																
BASELINE VALUE																																

0	0	NUMBER OF SKIPPED SAMPLES (N_{S0}) * 8		
1	1	SAMPLE 2 (ROI 1)	SAMPLE 1 (ROI 1)	SAMPLE 0 (ROI 1)
1	1	SAMPLE ... (ROI 1)	SAMPLE ... (ROI 1)	SAMPLE ... (ROI 1)
1	1	SAMPLE J (ROI 1)	SAMPLE J-1 (ROI 1)	SAMPLE J-2 (ROI 1)
0	0	NUMBER OF SKIPPED SAMPLES (N_{S1}) * 8		
1	1	SAMPLE 2 (ROI 2)	SAMPLE 1 (ROI 2)	SAMPLE 0 (ROI 2)
1	1	SAMPLE ... (ROI 2)	SAMPLE ... (ROI 2)	SAMPLE ... (ROI 2)
1	1	SAMPLE K (ROI 2)	SAMPLE K-1 (ROI 2)	SAMPLE K-2 (ROI 2)
...				
0	0	NUMBER OF SKIPPED SAMPLES (N_{Slast}) * 8		

EVENT DATA

DATA rates(3)

- Zero suppression firmware could be purchased and installed in V1730
  - This would allow to suppress the data below threshold in between S1 and S2, or the largely zero data of silicon and Lsci channel
  - Would allow faster readout through the optical link by an estimated factor 2
  - Data format would change, require s/w modification both in DAQ and in red-daq-light
- Note: a similar scheme already implemented in software in the original code

DATA rates(4)

- Sample decimation or down-grade of v1730 to 250 Ms/s is also a possibility
- Would only affect timing resolution of Si/PMT not TPC

- Possibility to acquire different sample length for different detector is not possible now to Trigger limitations

Trigger Schemes

Pulser	**OK**
[(Si E && Si DE) && Any PMT]	OK
[(Si E && Si DE) && TPC bottom] || Si Mon	OK
[(Si E && Si DE) && Any PMT] || Si Mon	Requires s/w (3 1730 trigger board)
[(Si E && Si DE) && TPC bottom] || [(Si E && Si DE) && PMT0	Requires s/w (3 1730 trigger board)
[(Si E && Si DE) && TPC bottom] || [(Si E && Si DE) && PMT || Si Mon	Require an extra vt1730 in the setup

Trigger Upgrade

- Logic within the V1730 is flexible enough to not recommend a separate signal path for trigger processing
- A separate trigger module always fore-seen and actually in our hands
- Not included due to man-power limitation so far

V2495 module

1 Introduction

Would substiture the NIM logic modules

64 logical input would allow to process the 8 + busy + veto signal of up to 6 boards

NIM mezzanine need to be added to generate TRIG_IN lemo signal for V1730 boards

Would greatly improve the reliability of board synchronization through front-panel LVDS daisy chains used now

The V2495 is a general purpose programmable FPGA and I/O unit housed in a 1-unit wide VME 6U module. The board is a suitable solution for the implementation of digital functions such as Coincidence, Trigger Logic, Gate and Delay Generator, Input/Output Register and more.

The programmable architecture is based on the User FPGA (hereafter UFPGA). The UFPGA is directly interfaced to the front panel I/Os and to an onboard Gate and Delay Generator, that allows to delay and gate up to 32 signals. A second FPGA, the Main FPGA (hereafter MFPGA), is responsible for USB and VME interface management. The MFPGA communicates with the UFPGA through an internal local bus.

The presence of three expansion slots interfaced to the UFPGA allows to extend the channel interface of the V2495 by adding up to three independent mezzanine boards. Five mezzanine board types are available: A395A, A395B, A395C, A395D, A395E (see **Tab. 1.2**). The V2495 can reach a maximum of 194 I/O channels.

The board can be controlled and programmed through either the VME or the USB interface. The CAENUpgrader software tool is provided to upload the FPGA firmware. An onboard dedicated JTAG connector allows for in-system JTAG configuration and debugging (e.g. using Altera SignalTap).

The V2495 can be considered as an evolution of CAEN V1495 board with which it bears several analogies (e.g. the front panel connectors have the same function and nomenclature with respect to the V1495). In addition, it provides enhanced logic resources, features and interfaces.

The following **Tab. 1.1** is a comparison table between the two modules.

V2495 module

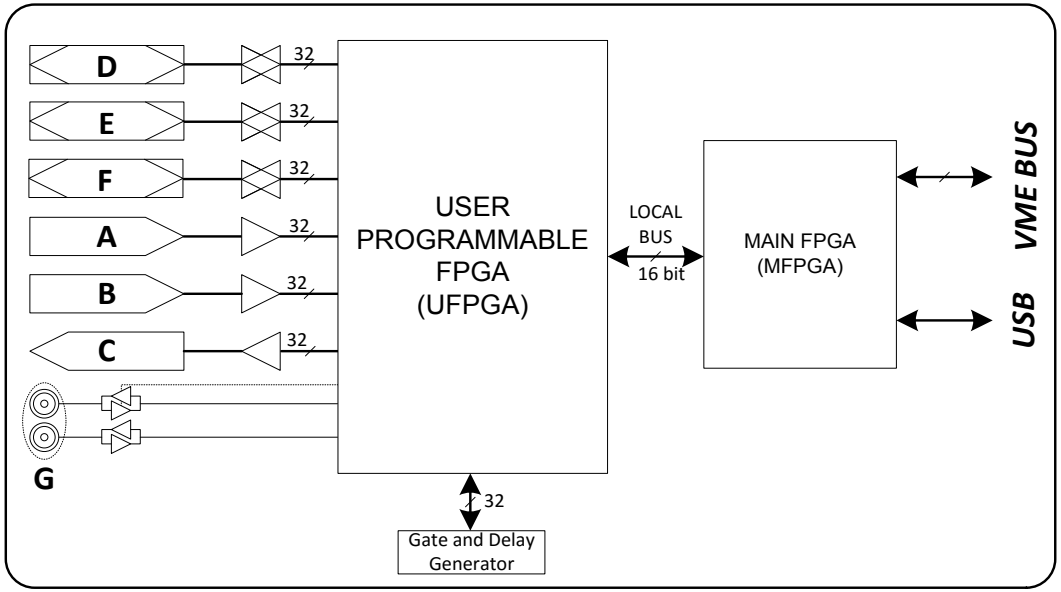


Fig. 2.1: Block diagram

- Main problem is to writhe the USER FPGA code
- CAEN provides building blocks/demo that are not sufficient for our scope
- No FPGA expert in the group

Operational problems/Reliability

- Non exhaustive list…
- Baselines not monitored, trigger threshold hardwired in configuration files and recorded in DB:
  - Suggest to integrate in the serrator code the writing of ADC threshold and baseline , reload those for the subsequent runs until a new laser run is taken/validated
- Event mis-alignment
  - Source of this is the delay introduced by the LVDS propagation of the busy/veto signal, normally this is recovered nicely in the event building/reconstruction stage
- Clock synchronization problem
  - Biggest problem so far, not clear the origin (board 3 h/w problem?)
  - Potentially induce large difference in event triggered (observed with sources, not beam)
  - Induce event window misalignment by exactly the pretrigger-window
  - A script to detect such a problem readily is available
  - Ask some help from CAEN, suggestion to be collected /implemented in due time, no clear evidence of board failure

Miscellanea

- Running laser together with data
- Ad hoc solution can be invented for special task
- Given the statistics needed for good laser calibration (100 kevents?), and assuming to devoto to this 1 Hz will take 1 full day

Update for Low energy

We need:

- 16 more channels for the neutron camera: trigger on the sum.
- Ideally we want to monitor continuously without changing DAQ settings:
  - SiMon spectrum: beam current.
  - Full Be Band spectrum: beam energy and Θ_{Be} (position of peaks), beam divergence (width of peaks).
  - Lower energy peak of Li Band: so C/H ratio degradation of target can be monitored.
  - TPC/Neutron detector time coincidences: together with full Be Band Spectrum -> Geometrical interception of neutron beam with detectors.
  - Accidental background rate in TPC using High Be blob.

A more complicated DAQ logic possible?

- Thresholds are set for each detector: SiTel, SiMon, TPC, LSci, Neutron Camera.
- Digitized counters for each channel.
- Only acquire digitized traces when necessary.
- Neutron detector threshold adjusted to 100 keVee, TPC to 30 keVee.
- Trigger types:

0-	SiMon (acquire SiMon only)	~1 Hz
1-	SiTel with no other trigger (acquire SiTel)	~ 50 Hz + LiBand
2-	SiTel + TPC time coincidence (acquire SiTel+TPC)	~ 1 Hz for 5 nA
3-	SiTel + Neutron detector time coinc. (acquire SiTel+TPC+LSci)	~ 5 Hz for 5 nA

Willing to contribute to changes.