FSSR2 Readout of SVT Layer 5

- The SVT external layers at SuperB will be longer than in BaBar => higher C_{load} and higher R_S.
- To start with, we assume all other geometrical parameters of the detector to remain unchanged.
- Can the FSSR2 front-end chip (possibly with a modified analog section) provide adequate S/N performance?

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- The worst-case situation is the phi-side of layer 5:
  - Total strip length = ~37 cm (on a half-module)
  - If we assume, as measured on BaBar LY5, a total strip capacitance of ~1.5 pF/cm, we get: C_{load} = ~55 pF
- The published noise parameters of the FSSR2, at the longest shaping time of 125 ns, are:

  ENC = 190 e^- + 21.5 e^-/pF * C_{load} (without BLR)

  ENC = 220 e^- + 24 e^-/pF * C_{load} (with BLR)
- Then the expected noise contribution from the detector capacitance would be:

  ENC(C_{load}) = ~1370 e^- (without BLR)

  ~ 1540 e^- (with BLR)

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- At such short shaping times (and high C), the noise contribution from series resistance could be even larger:
  - Assuming R/L = 10 ohm/cm for the metal strip (the value measured on BaBar LY5) the resistance of the metal strip turns out to be ~370 ohm
  - The resulting noise contribution is ENC(R_S) = ~2300 e^- (!!)
- The remaining noise contributions are negligible:
  - I_{leak} = 10 nA => ENC(I_{leak}) = ~120 e^-
  - R_{bias} = 4 Mohm => ENC(R_{bias}) = ~136 e^-
- The total noise would be: ENC_{tot} = ~2.7 ke^-

  => for a m.i.p. we get S/N ~ 8.5 (not enough!)

WARNING

- For the striplet and telescope detectors we obtained noise values sensibly higher than predicted...

  => Lab tests planned in order to try and understand the reason for this discrepancy

- Radiation damage will greatly increase the leakage current and slightly degrade the amplifier performance.

Possible (?) ways out

- Redesign the analog front-end, increasing the shaping time

  => how much would be acceptable from the standpoint of occupancy?

  Note: The occupancy will likely be dominated by noise events, so a lower noise would partially offset the effect of increasing tau.

  – Caution: longer tau => higher parallel noise (but there is room for improvement)

- Optimize the detector design for minimum capacitance, but:

  – significant improvement not likely

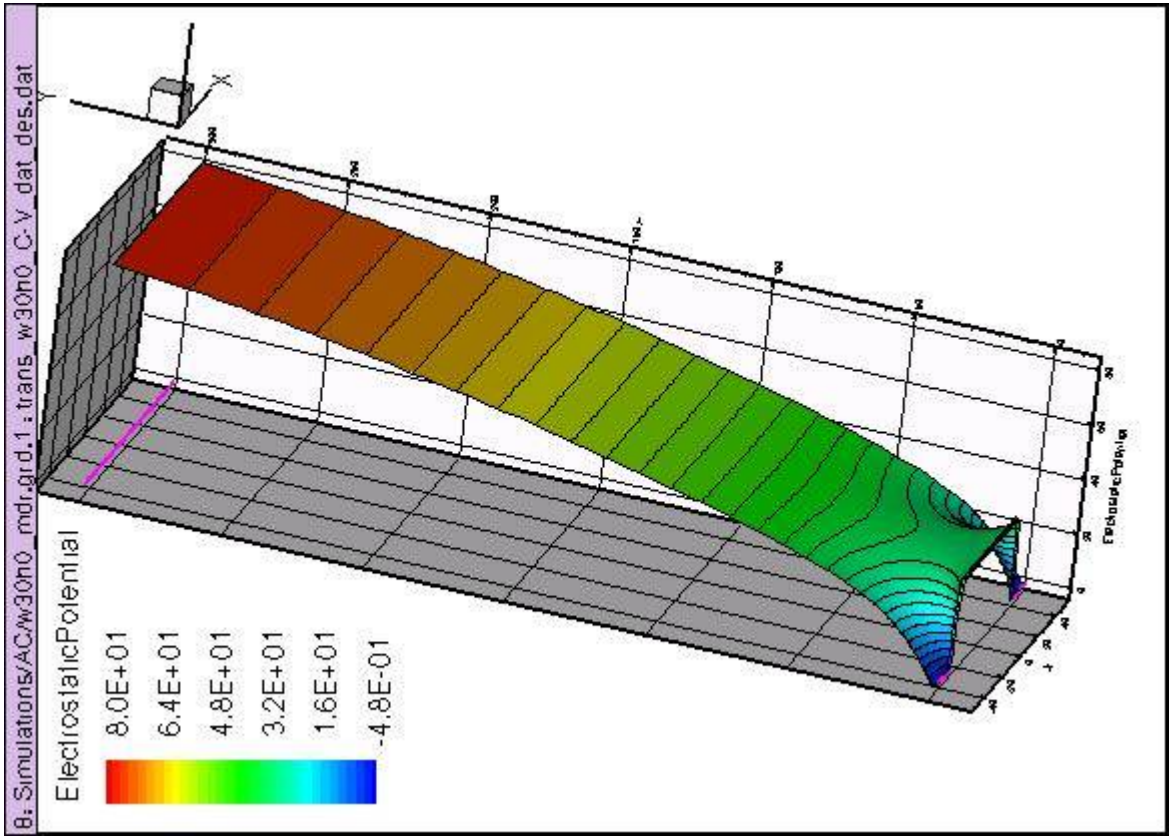
  – minimum *C* and minimum R_s are partially conflicting goals

  – low *C* => small *w/p* ratio => low field regions between strips

Conclusions

- A preliminary, rough estimate of the expected noise appears to preclude using the present version of the FSSR2 chip for the readout of the external SVT layers.
- More refined estimates of the detector parameters will be made, and the z-side (n-side) will also be considered.
- Geometry changes (strip pitch, width) can be explored with the help of simulations.
- An evaluation of the possible improvement coming from a redesign of the chip analog section is needed.

Simulated electrostatic potential



Electrostatic potential in a (single sided) 300 µm thick detector, with 30 µm wide strips at 100 µm pitch. The region from the mid point of a strip to the mid point of the a neighboring one has been simulated. The detector (depleted at 37 V) is biased at 80 V. (A. Starodubtsev - INFN Trieste)