VIII International Course

Detectors and Electronics for High Energy Physics, Astrophysics, Space and Medical Applications

INFN – Laboratori Nazionali di Legnaro, April 1-5 2019

Pixel Front-end Electronics for High Time Resolution

Adriano Lai – INFN Sezione di Cagliari

Istituto Nazionale di Fisica Nucleare

Forewords

As it is impossible to teach advanced subjects in 1 hour, I decided to set this lecture on basic concepts and suitable to "non-specialists".

The subject is very interesting and full of subtleties – (a) completely different approach(es) could have been possible

I apologize to "specialists" if they find this lecture usuless

I hope to give some useful hints to the others

Pixels with timing: What are we talking about

Vertex detectors with timing: Phase-2 ATLAS-CMS vertex detector + 30 ps rms per pixel → Vertex detectors from 2030 (LHCb) and beyond (future colliders?)

Target specifications:

Sensors:

→ "Native" or intrinsic time resolution of 20-30 ps rms (proven as possible)

→ Active area: tipically 50x50 μm2 (ATLAS, CMS, LHCb) – Vertex detectors In timing layers we can reach wider sizes

Electronics (@ Vertex)

→ High particle rates (1-3 GHz/cm^2)

→ High data bandwidth (10's of Gb/s per chip, some Tb/s per detector)

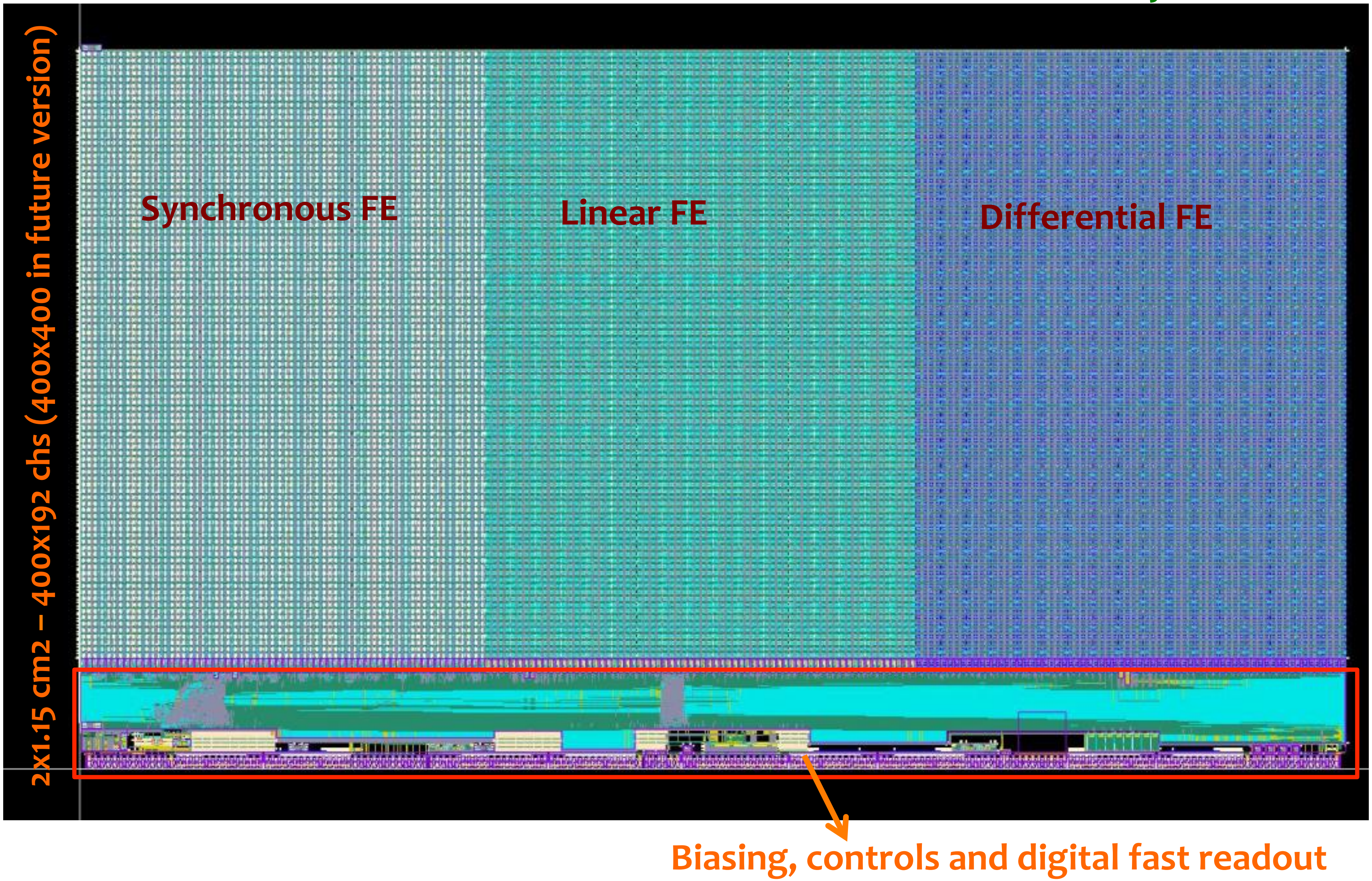
→ Low power (mainly to limit max power dissipation) 100-300 mW/cm^2 ATLAS-CMS W/cm^2 LHCb (better cooling system) → 10 to 50 μA per pixel

Many of the issues above are already "under control" (e.g. ATLAS/CMS RD53 device(s)), but…

Pixels with timing: What are we talking about

Reference: RD53A, the best beast*

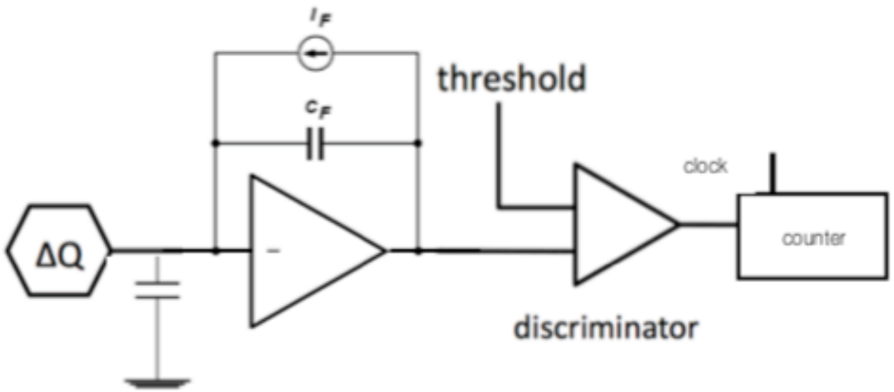
*as of today



Analog FE scheme(s) in RD53A

Source: L. Demaria TREDI 2019 25/2/19

1. Signal charges fast Feedback Capacitance (Cf) ;
2. A stable current discharges Cf, making the signal duration linearly dependent wrt charge;
3. Discriminator determines when the signal is above threshold : **Time over Threshold**
4. a clocked counter counts the ToT

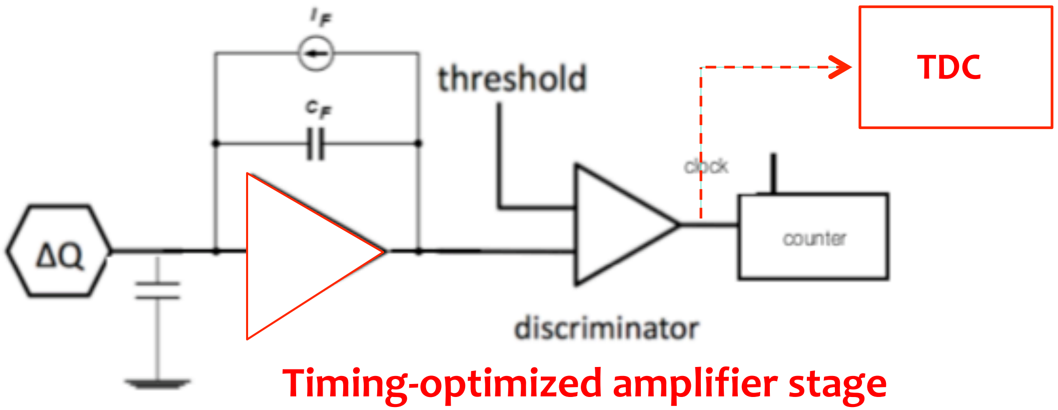


	Input	Ileak to sensor	Feedback-current	Discriminator	Threshold pixel tuning	ToT-count clock
Linear FE	single ended	Krummenacher		Asynchronous	4-bit trimming DAC	40 MHz chip clock
Diff FE	differential	LCC circuit	IFF	Asynchronous	5-bit trimming DAQ	40 MHz chip clock
Synch FE	single ended	Krummenacher		Synchronous with BX	Autozero Pulse 200ns@abort gap	20-400 MHz local clock

Analog FE scheme(s) in RD53A

… But we want time and highly resolved time

1. Signal charges fast Feedback Capacitance (Cf) ;
2. A stable current discharges Cf, making the signal duration linearly dependent wrt charge;
3. Discriminator determines when the signal is above threshold : **Time over Threshold**
4. a clocked counter counts the ToT

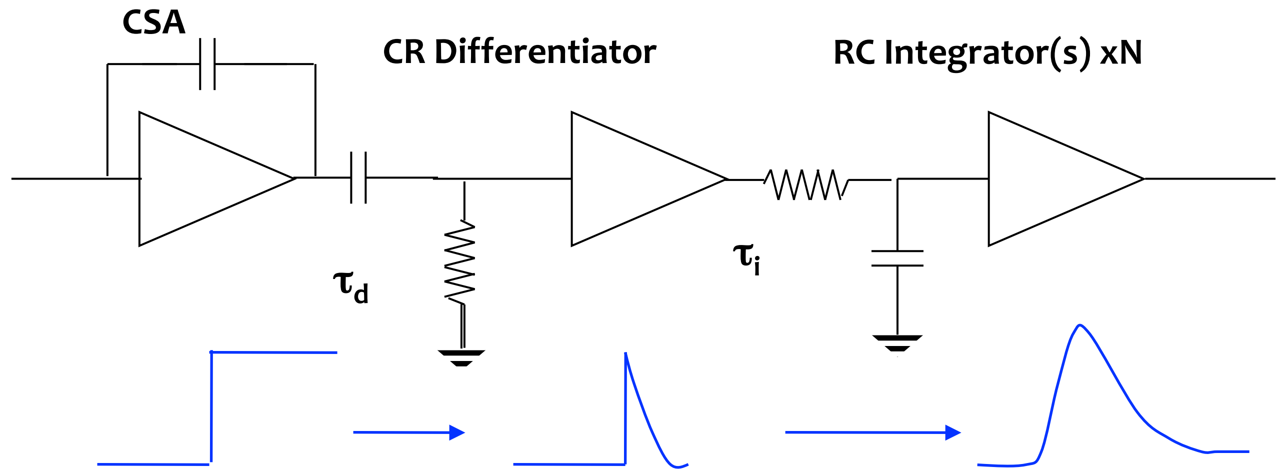


High time resolution TDC 1 per channel or group of channels

	Input	Ileak to sensor	Feedback-current	Discriminator	Threshold pixel tuning	ToT-count clock
Linear FE	single ended	Krummenacher		Asynchronous	4-bit trimming DAC	40 MHz chip clock
Diff FE	differential	LCC circuit	IFF	Asynchronous	5-bit trimming DAQ	40 MHz chip clock
Synch FE	single ended	Krummenacher		Synchronous with BX	Autozero Pulse 200ns@abort gap	20-400 MHz local clock

Old good times: CSA+ semi-Gaussian filter

Basic FE classic scheme for low noise Energy measurement from Capacitive sensors



Transfer function (frequency domain)

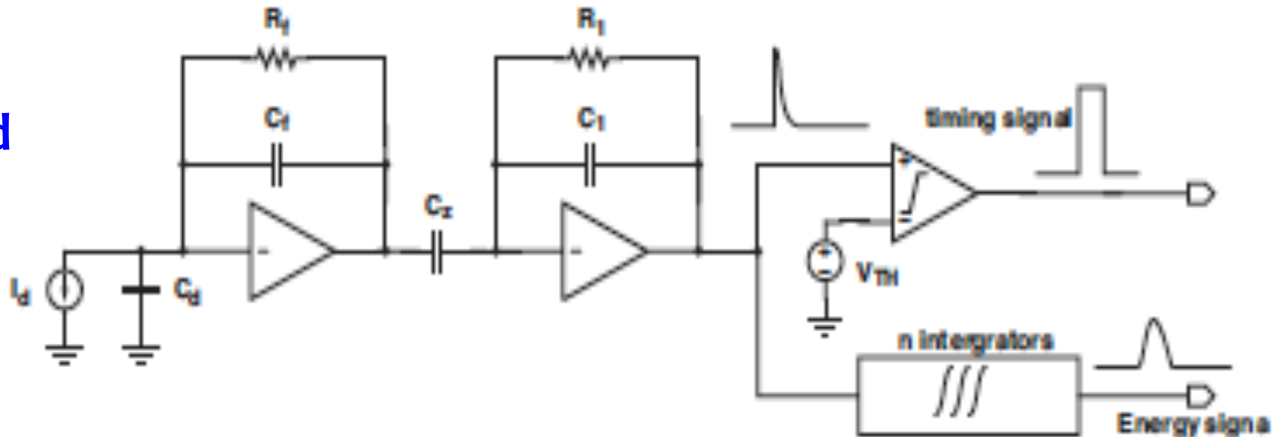
$$H(s) = \frac{1}{sC_f} \times \frac{s\tau_d}{1+s\tau_d} \times \frac{1}{1+s\tau_i}$$

∂ pulse response (time domain)

$$h(t) = \frac{1}{C_f} \otimes \delta(t) - \frac{1}{\tau_\mathrm{d}} e^{-t/\tau_\mathrm{d}} \otimes \frac{1}{\tau_\mathrm{i}} e^{-t/\tau_\mathrm{i}}$$

S-transform/ anti-transform

Timing output privileges fast(er) and steeper components of the processed signal



(Very) Basic concept on electronic time measurement

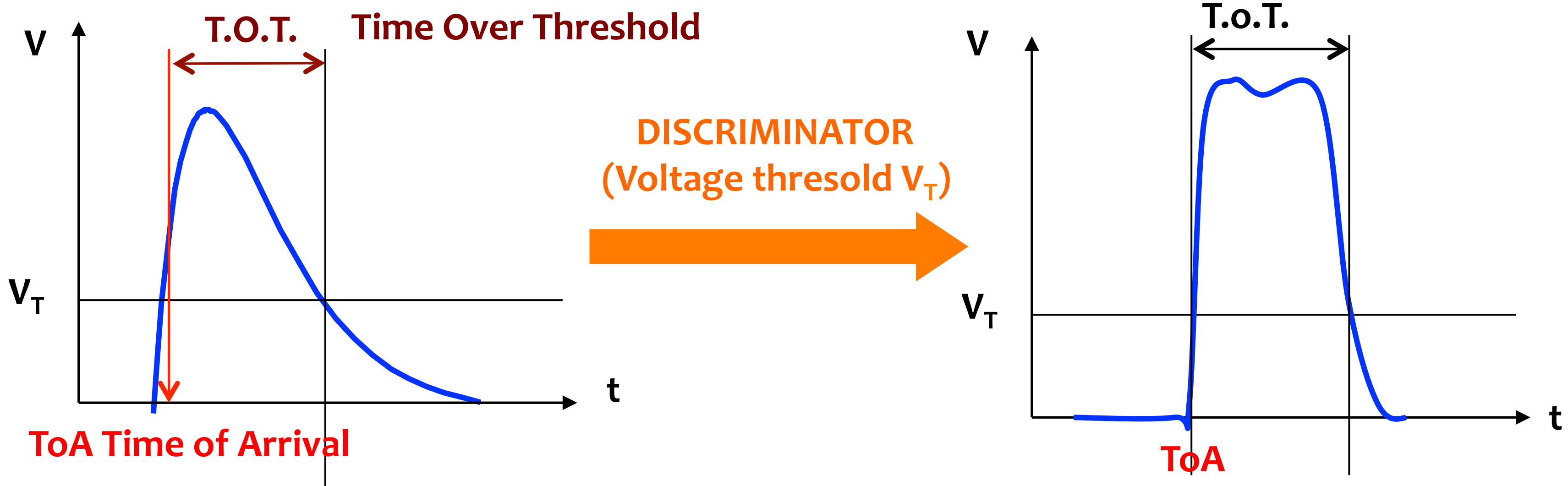
Energy (amplitude) → TIME

NOISE → JITTER

Conceptual method:

1. Get an analog signal (F/E amplifier) → 2. Apply a threshold → 3. Get a binary signal (Discriminator) →
→ 4. Measure the delay from a time reference (system clock, TDC)

Analog signal (out CSA/Shaper) → Binary Signal (out Discriminator)

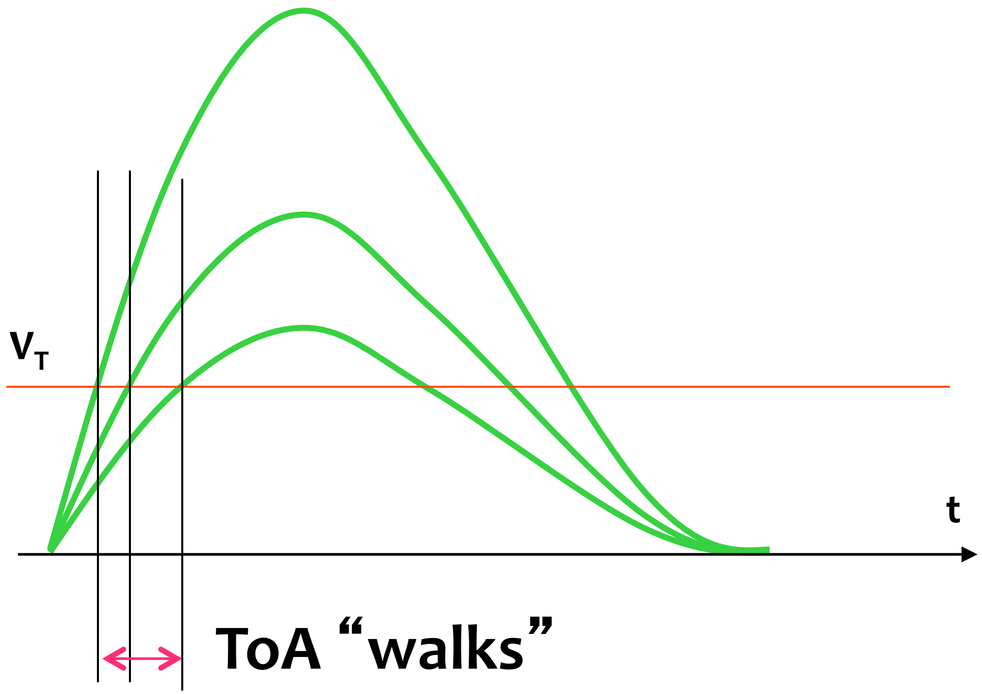


Time walk effect on signal

CSA+CR-RC^n output:

Constant T_{peak},
Amplitude proportional to charge

ToA depends on amplitude (or deposited charge)



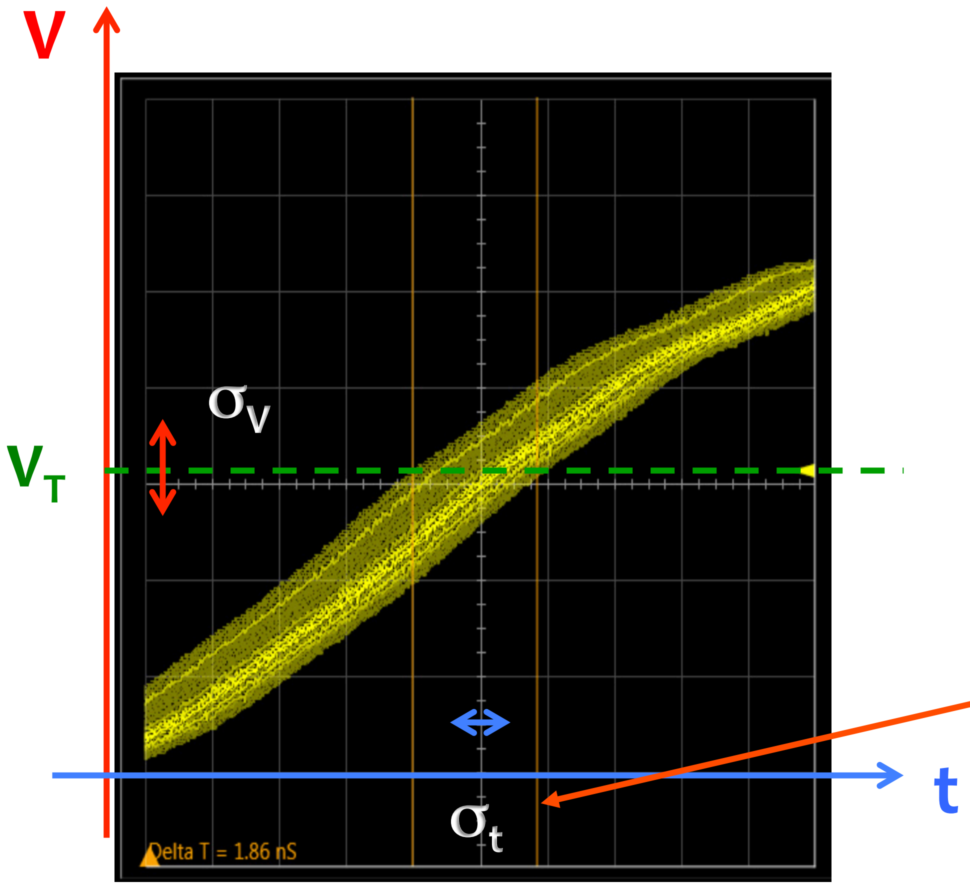
ToA "walks" = Time Walk (TW)

TW can be minimized

→ **Using lower V_T as possible**
→ **Correcting by ToT (~ proportional to amplitude)**
→ **Using Constant Fraction Discrimination**

σ_t: from amplitude to time noise

Uncertainty (fluctuation) in voltage threshold crossing → time resolution



Fluctuations depend on voltage amplitude noise (σ_V), which has several and different contributions

The projection of σ_V on the time axis gives time resolution σ_t

$$\sigma_t = \frac{\sigma_V}{\left.\frac{dV}{dt}\right|_{V_T}}$$

low σ_t:

→ low σ_V

→ high derivative

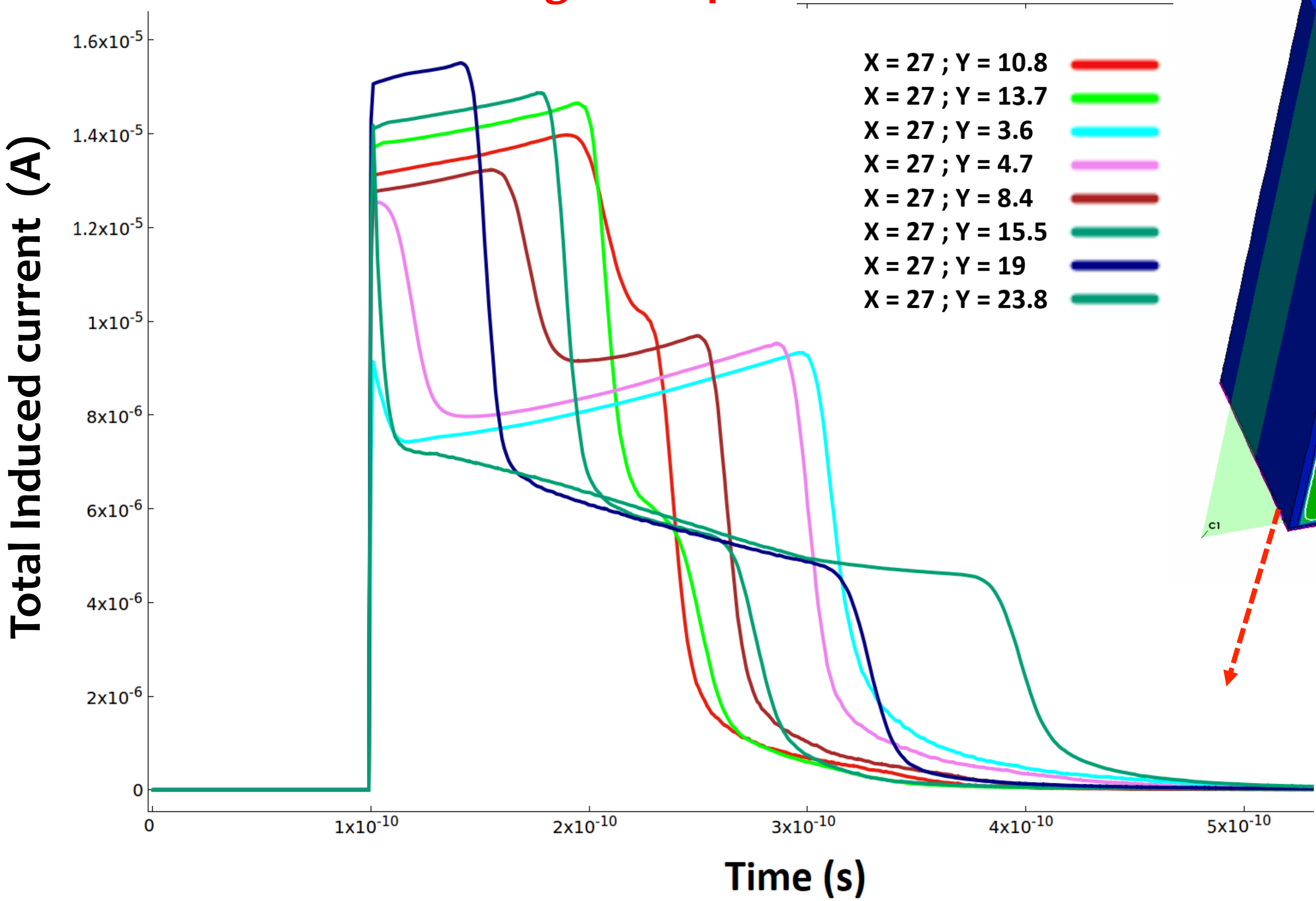
What "makes" σ_t ?

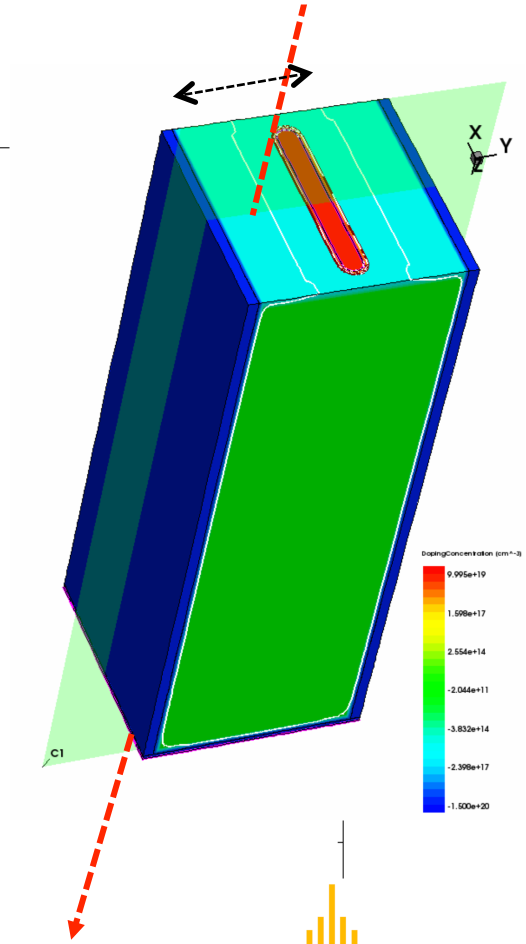
Starting point: sensor signals.

example from a 3D (fast) silicon sensor

π^+ tracks with different impact points

What matters out of the signal shape?

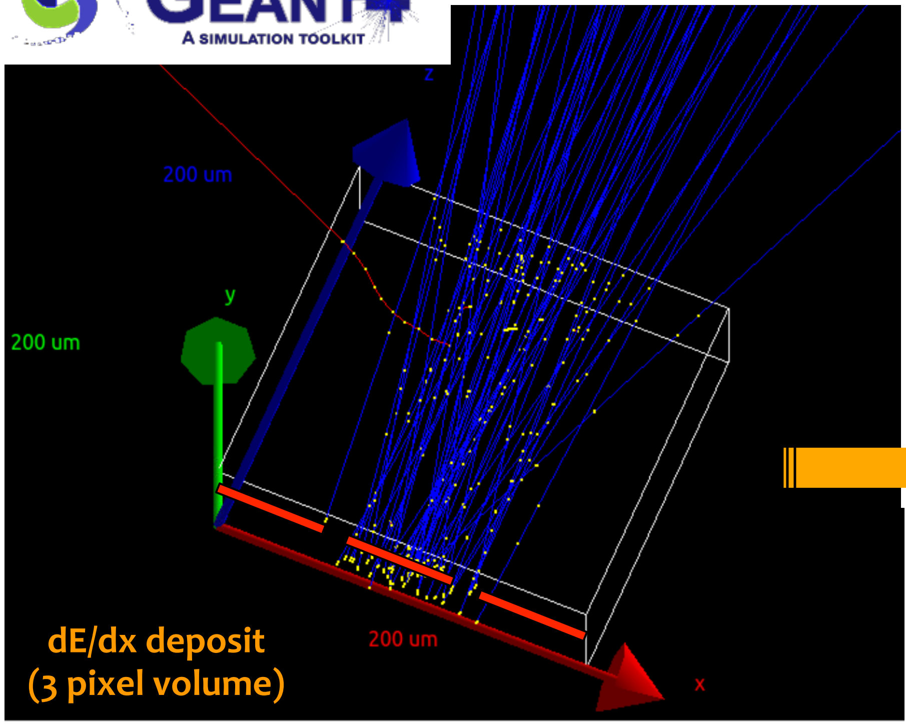


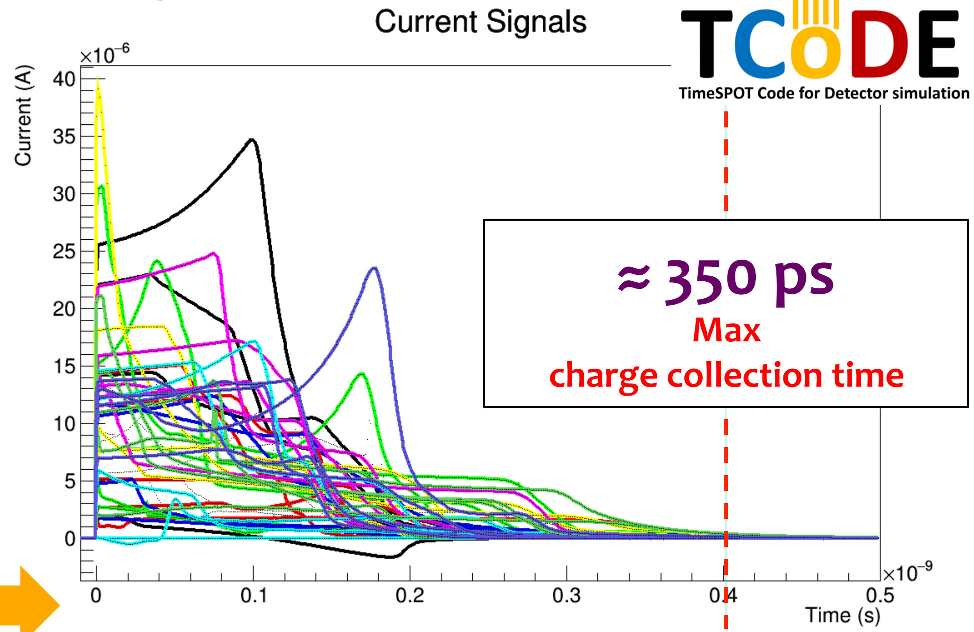


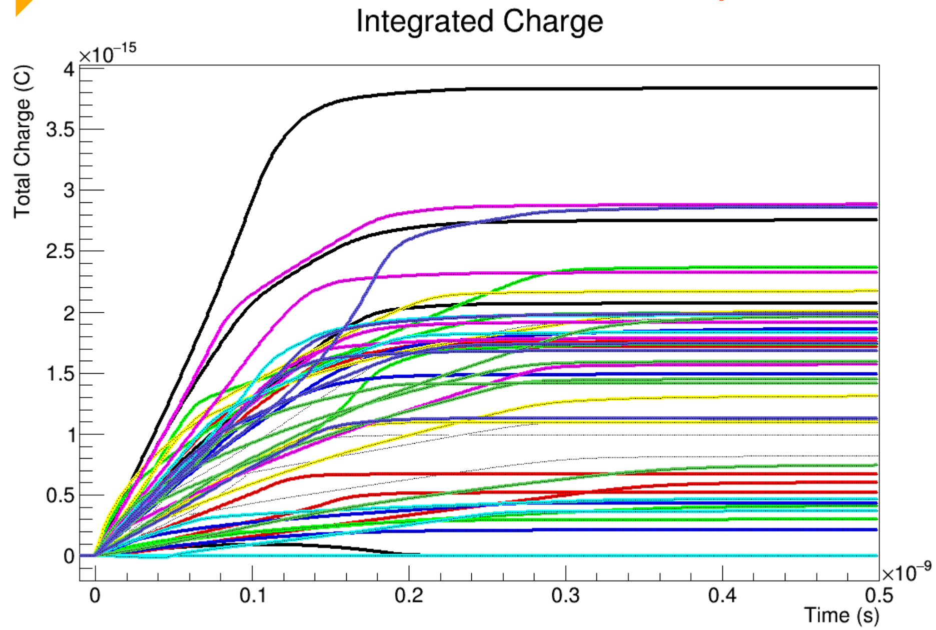
TCoDE
TimeSPOT Code for Detector simulation

A. Contu, A. Loi
INFN Cagliari

σ_t and signal dispersion







50 tracks on a 3D pixel.
→ Induced current signals on read-out electrode.

Dispersion is still important after averaging by front-end electronics

Uncertainties to t measurement:
Classification (factorization) of contributions

$\sigma^2_t =$ σ^2_{Jitter} +

Depends on intrinsic noise σ_n from sensor and amplifier and on amplifier speed, which varies in a competitive way. The subtlest one

$\sigma^2_{Time\ Walk}$ +
$\sigma^2_{Disuniformity}$ +
$\sigma^2_{Landau\ Noise}$ +

Depend only on fluctuations due to sensor geometry and signal amplitude variations (differences in energy deposits). Independent of front-end noise

σ^2_{TDC}

Depends only on electronics. On general grounds, it is not a relevant contribution to the final resolution. It can become important when issues of area and consumption budget come into the game (as happens for pixels)

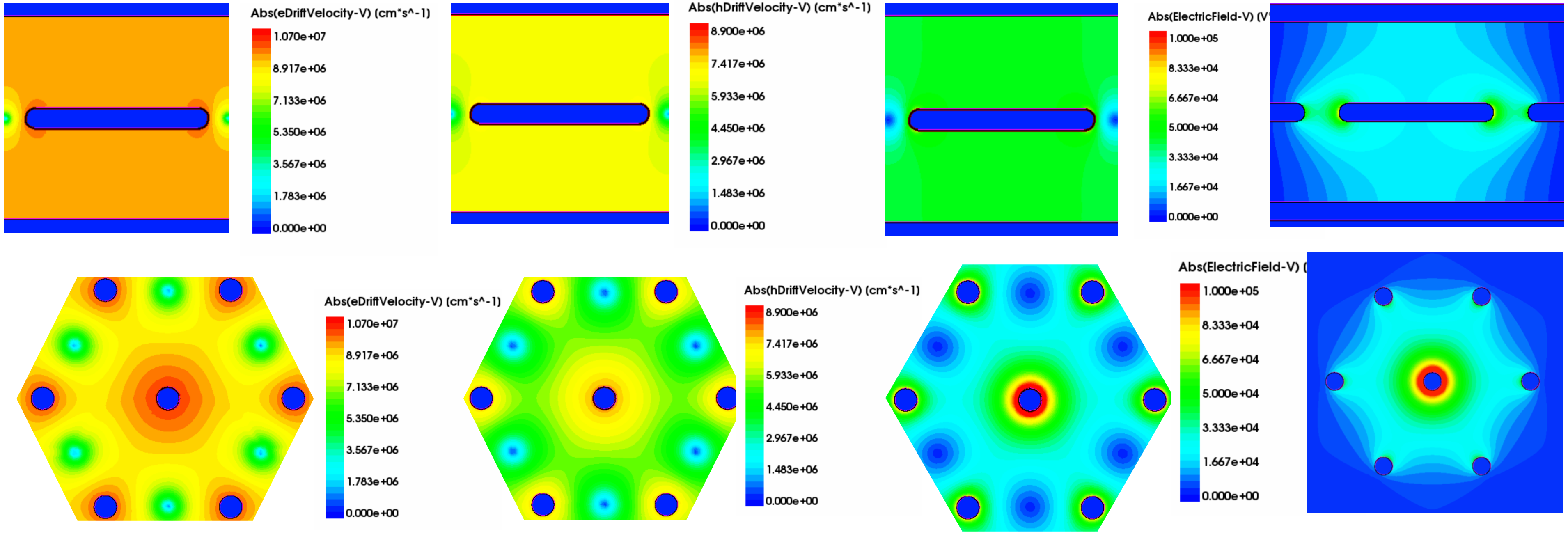
An example: 3D silicon sensors (again!)

$$\sigma^2_t = \sigma^2_{Jitter} + \sigma^2_{Time\ Walk} + \sigma^2_{Landau\ Noise} + \sigma^2_{Disuniformity} + \sigma^2_{TDC}$$

Sensor & electronics

Sensor and dE/dx

Electronics
V_{bias} = 100 V



Electron drift velocity

Hole drift velocity

Electric field

Weighting field

$I_{induced} = qv \cdot E_w$ (Ramo's Theorem)

INFN
Istituto Nazionale di Fisica Nucleare

σ_n and σ_t (σ_{jitter})

From now on we will indicate σ_{jitter} as σ_t, *focusing on the interplay between sensor and electronics and leaving aside the other contributions to time resolution, to be optimized separately**

$$\sigma_t = \frac{\sigma_n}{\frac{dV}{dt}} \approx \frac{\sigma_n}{\frac{V_{max}}{t_r}} = t_r \left(\frac{S}{N}\right)^{-1}$$

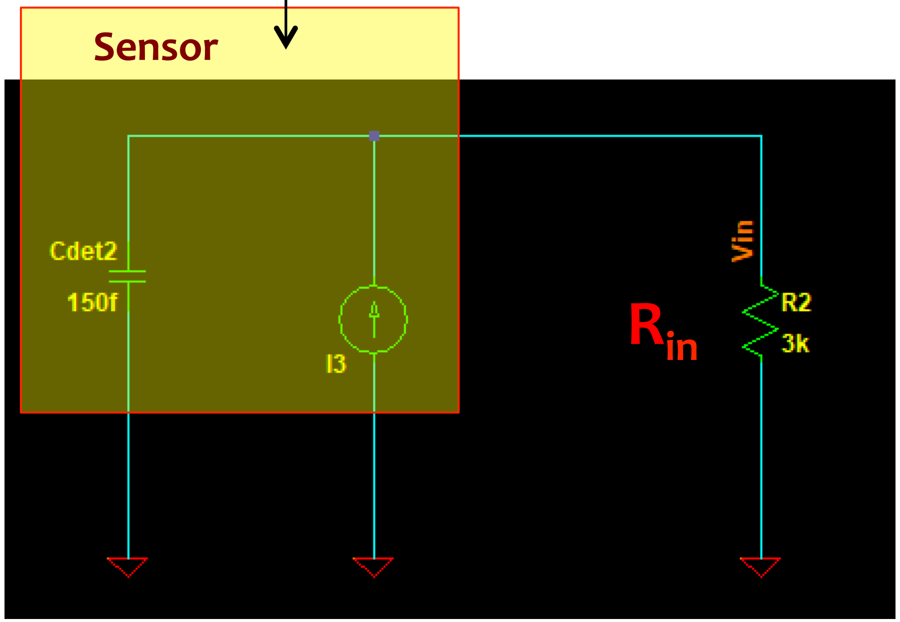
low σ_t
- → low σ_n
- → small t_r
- → large amplitude

***indeed, $\sigma_{\text{Time Walk}}$ will come back to bother us soon !**

The simplest possible read-out circuit(s)

Induced current pulses on the sensor electrodes "experimentally" are almost "abstractions" – to be measured they must be necessarily modified (processed)
Athough the simulator models the sensor capacitance, it is not even considered, as we are "measuring" the current with an ideal zero impedance Amperometer

The sensor is well modeled by a current (signal) source and a capacitor



In practice, any component you will connect, it will have some finite impedance

The ~~trans~~impedance (un)amplifier

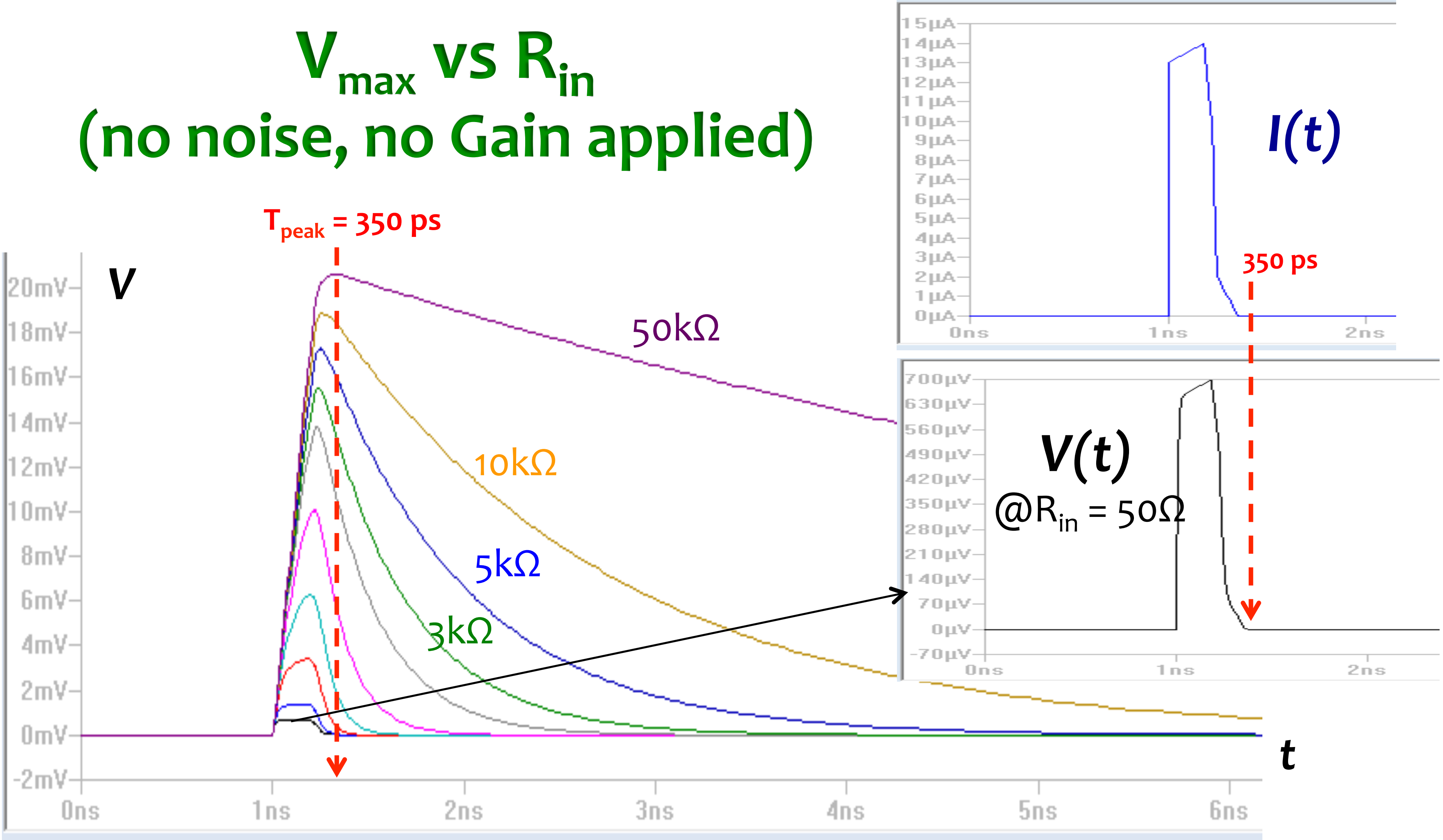
$$I_{in} \rightarrow V_{out}$$

Leakage: $\sigma^2_{leak} = 2qI_{leak}BW$

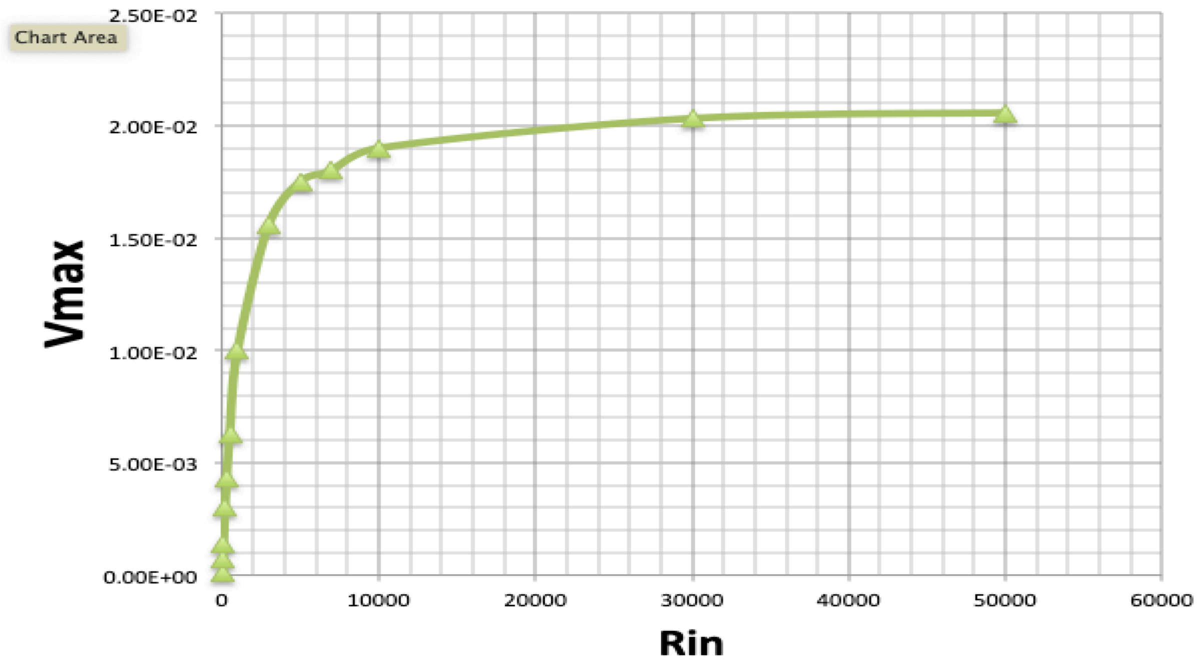
Depends on Sensor. Here considered as negligible

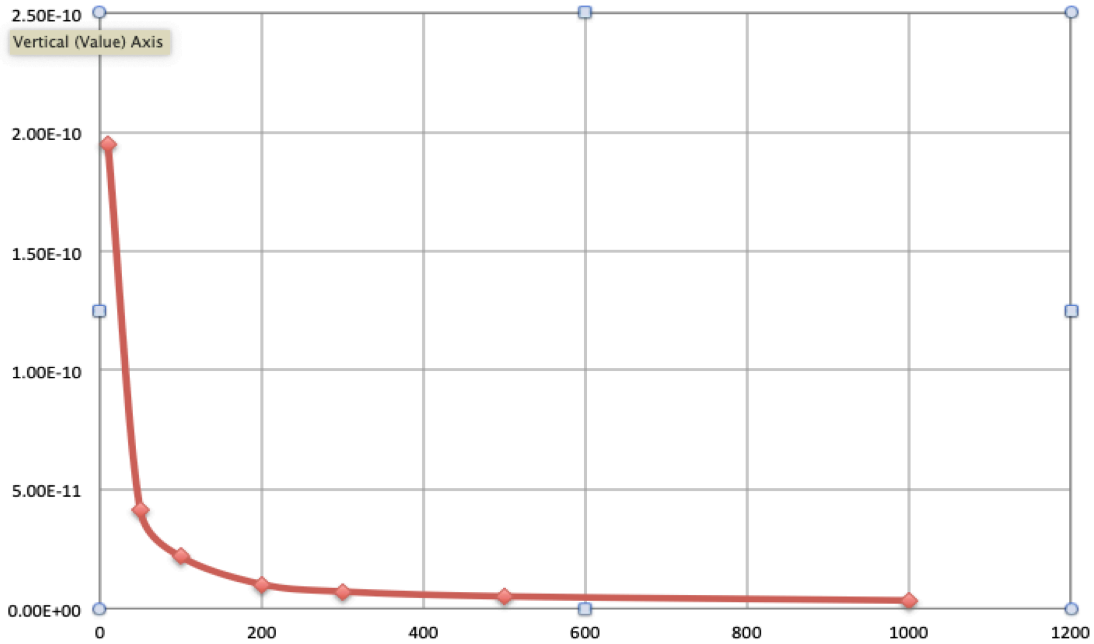
Thermal: $\sigma^2_{therm} = 4kTR_{in}BW = kT/C$ *(see below)*

V_{max} vs R_{in}
(no noise, no Gain applied)



- At small R_{in} the V signal tends to follow the induced current shape. The signal width follows the t_c (collection time of charge carriers, t_c ~ 350 ps in this special case)
- Increasing R_{in}, the V signal approximates an ideal integrator, with $V_{max} \approx Q_s/C_s$. T_{peak} tends to t_c. The only capacitance here is C_s, so T_{peak} ~ time needed to charge C_s at I ~ const





C_s = 150fF

I_s ~ 13 μA

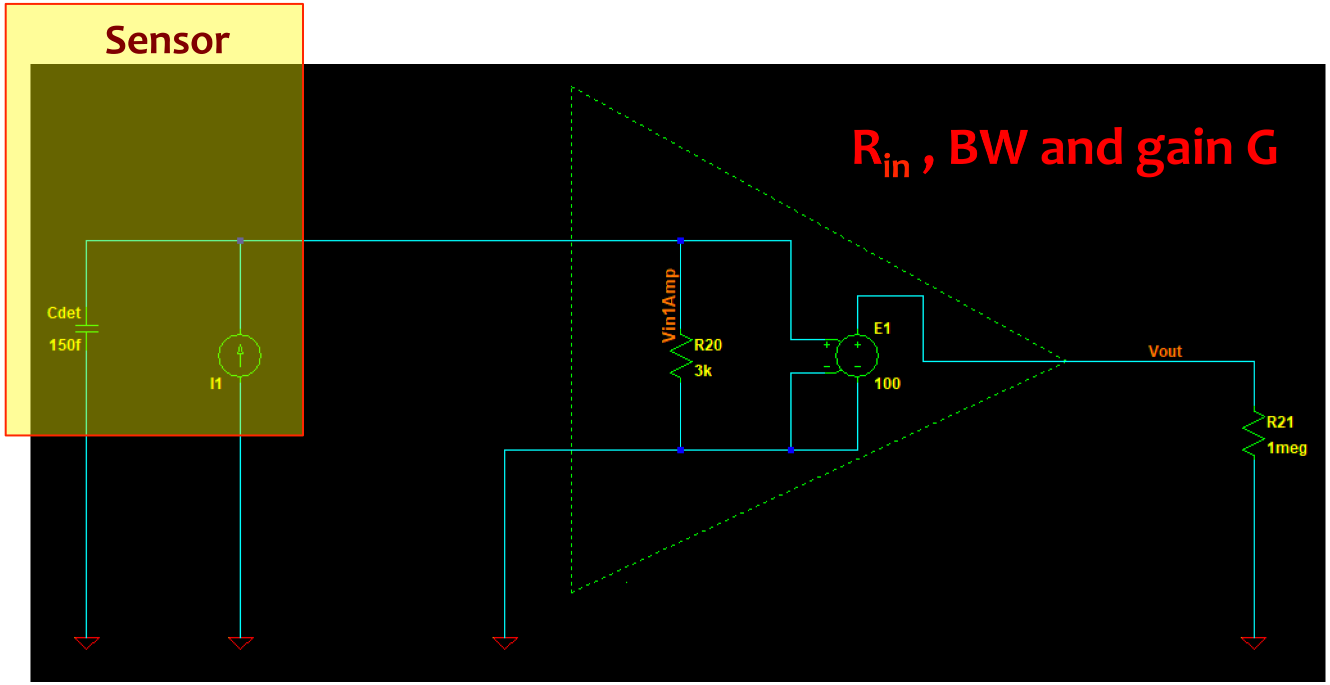
Signal amplitude V_{max} vs R_{in}

A large R_{in} (ideal integrator behaviour) helps

$t_{vmax}/V_{max} \approx \sigma_t$ vs R_{in}

Amplifier, BW & noise

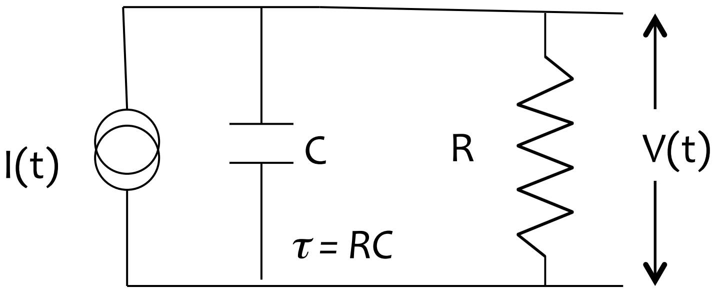
In principle, the impedance un-amplifier with high R_{in} would fit our needs. Of course this is practically unadequate: to trasmit the information we need a larger signal and a low-impedance driver, that is a true amplifier stage

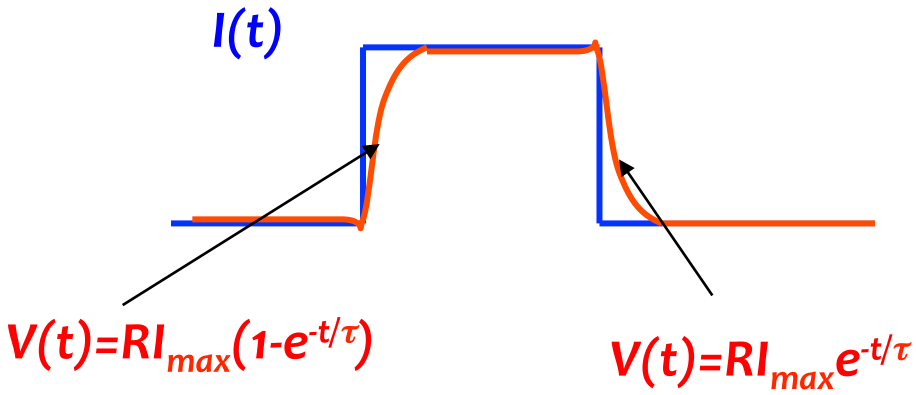


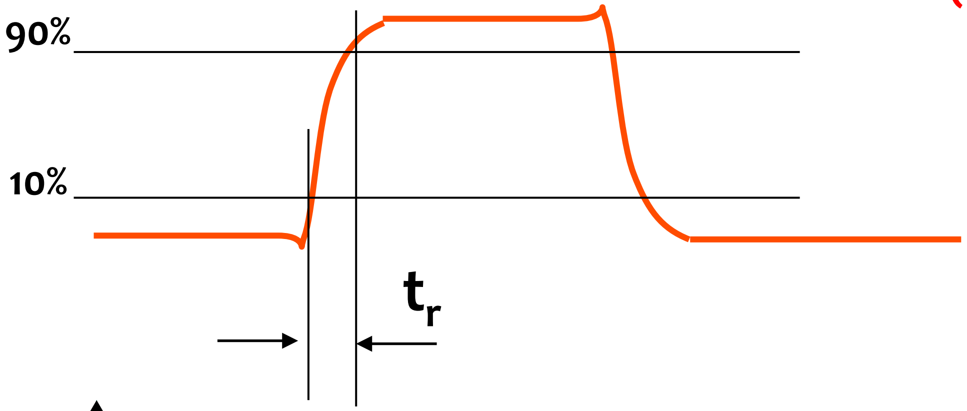
R_{in} is now seen as the input impedance of the amplifier.
Introducing an amplifier stage means introducing additional poles in the system transfer function, thus changing the signal shape dramatically
What should be the amplifier BW for optimal time resolution?

Single pole network: signal *rise time* (t_r) and *Band Width*

RC circuit

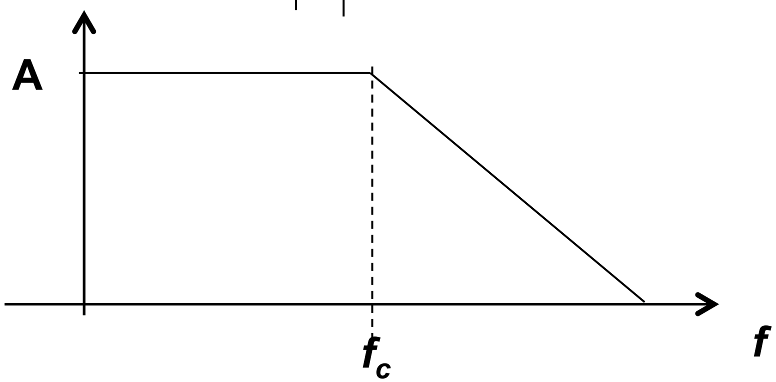






$$t_r \cong 2.2\tau \approx \frac{0.35}{f_c}$$

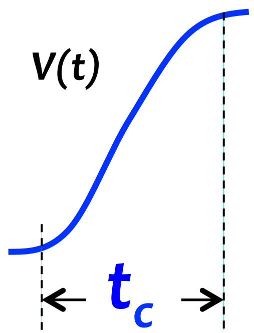
$$f_c \equiv \frac{1}{2\pi\tau}$$



NB → t_r is related to the 1st pole frequency of the network f_c (BW)

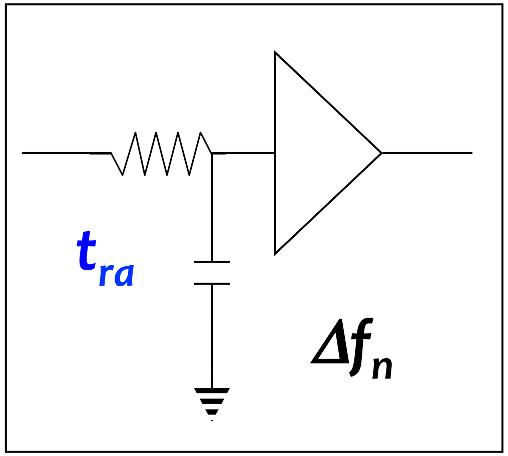
Es. oscilloscope BW = 250 MHz → t_r(max) = 1.4 ns

Maximize t_r and minimize noise



t_c = charge collection time

v_{ni} → Input noise



t_{ra} = amplifier rise time. Δf_n = amplifier BW (approximated to an RC stage)

V_{no} → output noise

$$t_r = \sqrt{t_c^2 + t_{ra}^2}$$

t_r (output)

Exact if stages are Gaussian. Good approximation within ~10% otherwise

Output noise (from integrating amplifier stage)

$$\sigma^2_v = V_{no}^2 = \int v_{ni}^2 \, df = v_{ni}^2 \, \Delta f_n$$

(white noise)

For a pure integrator stage (single pole)

$$\Delta f_n = \frac{\pi}{2} f_2 = \frac{1}{4\tau} = \frac{0.55}{t_{ra}}$$

(see next slide)

$$\Delta f_n \propto \frac{1}{t_{ra}}$$

Δf_n = output noise bandwidth

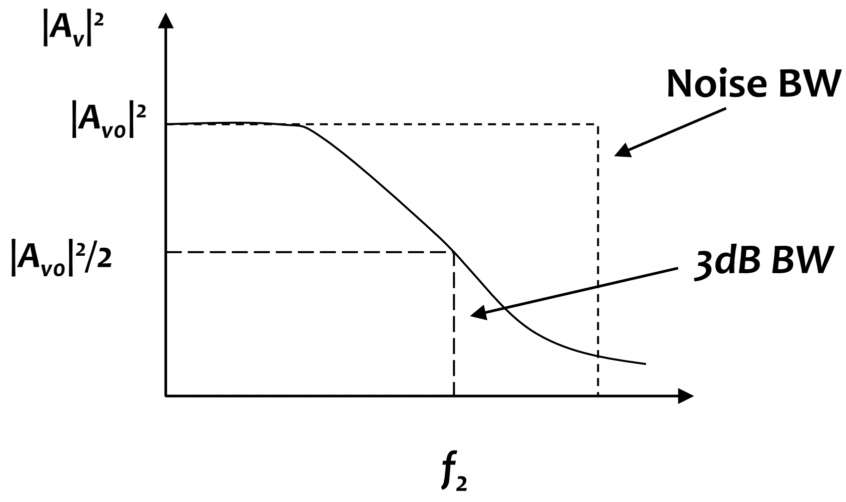
→ Noise and speed are competitive effects → optimization

A note on BW (Δf)

(skip it now)

Δf

Interval of frequency corresponding to the base of a rectangle having the same area of the effective power gain of the system



$$\Delta f = \frac{1}{A_{vo}^2}\int_0^{\infty} \left|A_v(f)\right|^2 df$$

If the system has one pole (e.g. a Pass Bass Filter):

$$\Delta f = \int_0^{\infty} \frac{df}{1+\left(f/f_2\right)^2} \xrightarrow{f = f_2 \tan\vartheta} \Delta f = \int_0^{\pi/2} \frac{f_2 \sec^2\vartheta\, d\vartheta}{1+\tan^2\vartheta} = f_2\int_0^{\pi/2} d\vartheta = \frac{\pi}{2} f_2$$

(normalized to 1)

$$\Delta f = \frac{\pi}{2} f_2$$

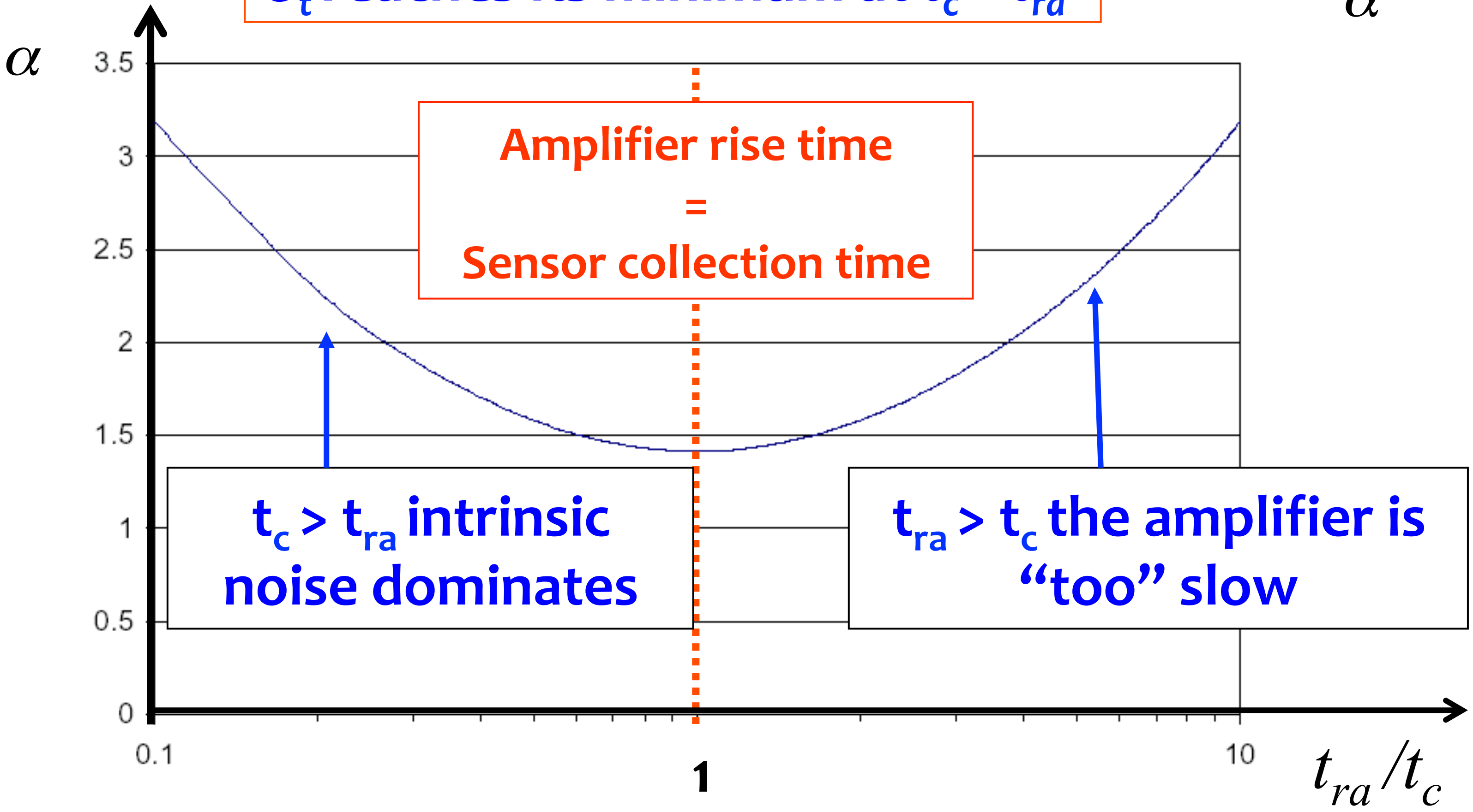
Simple RC stage:
f_2 = 3dB frequency

Estimate of OPTIMUM t_r (fixed $V_{max}=V_o$)

$$\sigma_t = \frac{\sigma_v}{dV/dt} \approx \frac{\sigma_v}{V_0/t_r} = \frac{1}{V_0}\sigma_v t_r \propto \frac{1}{V_0}\frac{1}{\sqrt{t_{ra}}}\sqrt{t_c^2+t_{ra}^2} = \frac{\sqrt{t_c}}{V_0}\sqrt{\frac{t_c}{t_{ra}}+\frac{t_{ra}}{t_c}}$$

$\alpha = \sqrt{\frac{t_c}{t_{ra}}+\frac{t_{ra}}{t_c}}$

σ_t reaches its minimum at $t_c = t_{ra}$

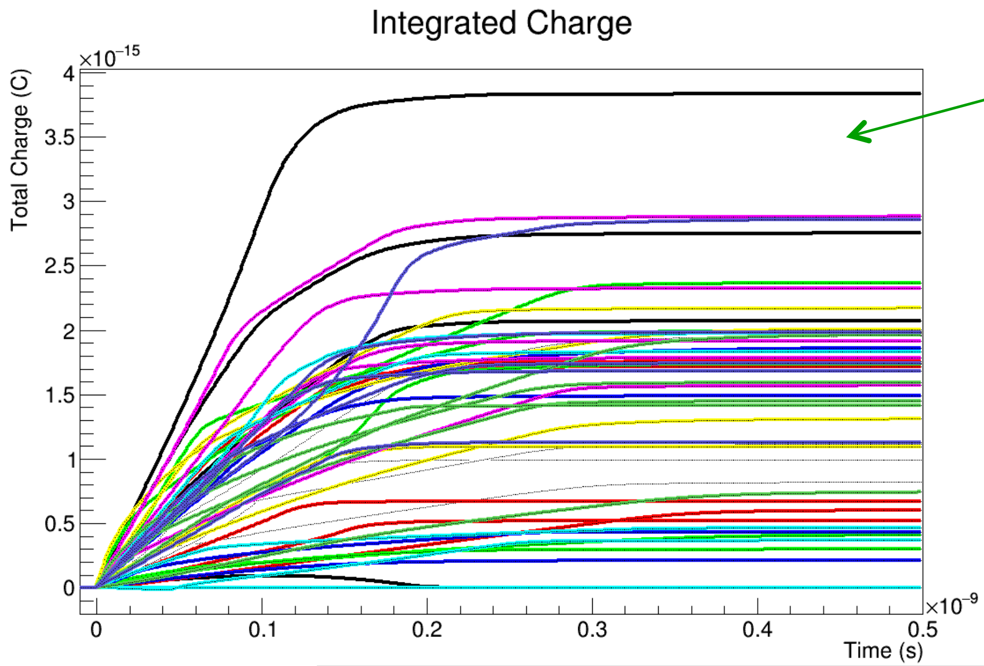


Have we eventually found the ideal amplifier for timing ?

High R_{in} (high signal, high decay time, although – see later on this point)
$1/R_{in}C_s \sim BW_{amp}$ (optimal speed-noise BW trade-off)

but

Amplifying the signal, while keeping the right slope, requires high power consumption



The output signal sees different signal shapes in the active volume of the sensor.

Even different C_s in the different sensor batches can matter in this case

$$\sigma^2_t = \sigma^2_{Jitter} + \sigma^2_{Time\ Walk} + \sigma^2_{Landau\ Noise} + \sigma^2_{Disuniformity} + \sigma^2_{TDC}$$

They enter back through the window !!

Charge Sensitive Amplifier

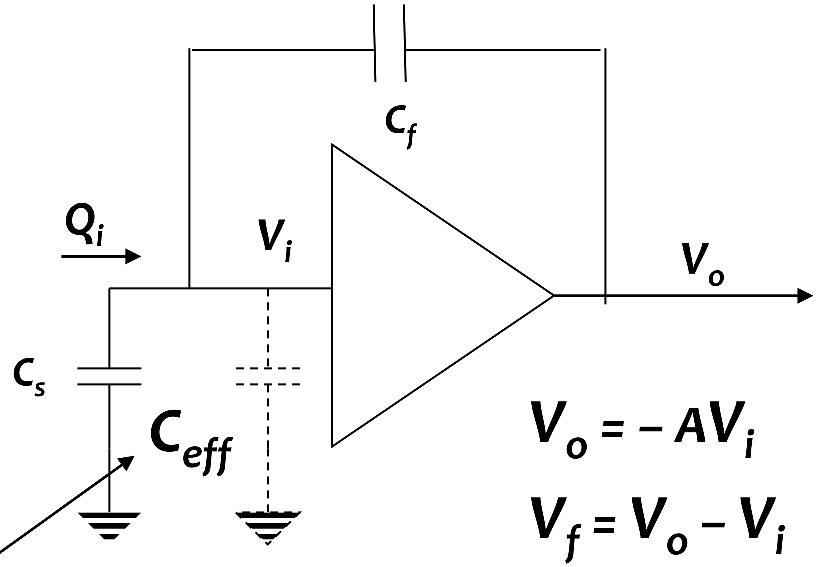
The way to make V_o strictly proportional to charge and independent of C_s

(assuming $R_{in} \sim \infty$)

$$v_f = (A+1)\, v_i$$

$$Q_f = C_f\, v_f = C_f\,(A+1)\, v_i$$

(Miller effect)



$$V_o = -AV_i$$

$$V_f = V_o - V_i$$

Effective Capacitance moved at the amplifier input

$$C_{eff} = \frac{Q_i}{v_i} = C_f\,(A+1)$$

Charge Gain A_Q:

The amplifier capacitance (and BW) dominates

$$A_Q = \frac{dV_o}{dQ_i} = \frac{A\,V_i}{V_i\,C_{eff}} = \frac{A}{C_{eff}} = \frac{A}{A+1}\cdot\frac{1}{C_f} \approx \frac{1}{C_f} \quad (A >> 1)$$

CSA-like amplifer pros and cons

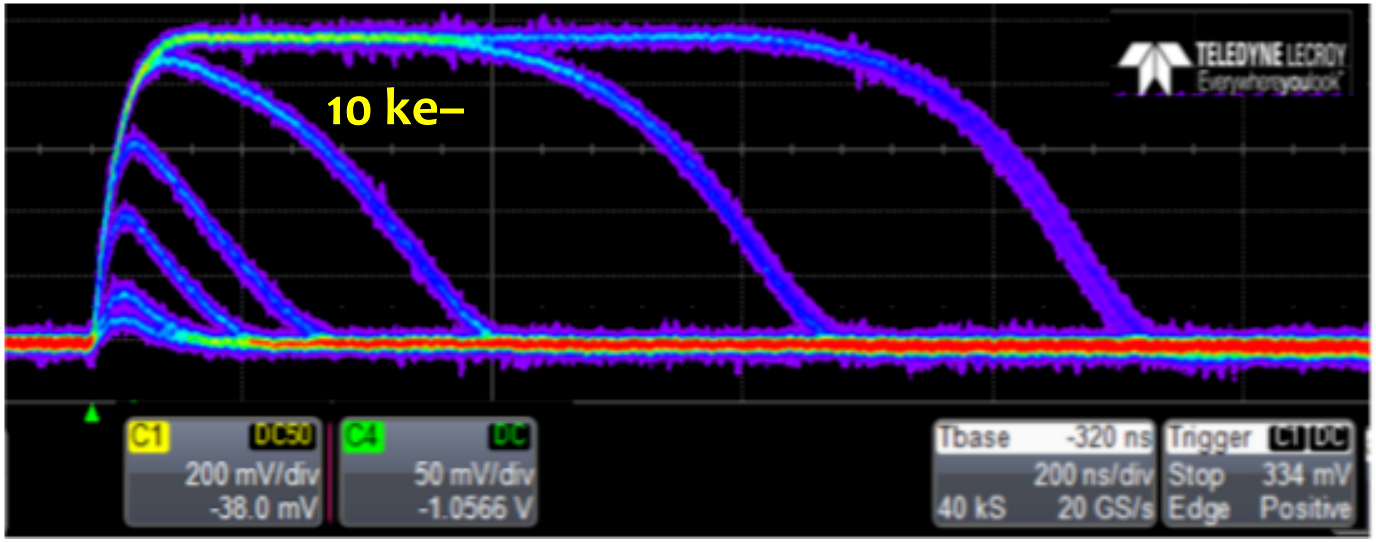
Pros

- The output behaves similar to an ideal integrator with output proportional to Q_{in} (high V_{max}, good T_r)
- TW is due only to different Q_{in} and is independent on sensor C_s
- In constant-current discharge schemes, the ToT has a good degree of proportionality to Q_{in}, so allows TW correction (T_{peak} is not constant – as it is in CR-RC shapers
- Good performance in terms of noise and power consumption
- It is a well-established solution with wide experience in our design centers

Cons

- TW corrections, based on ToT can be easily done on data, but this is not suitable to real-time response (could be a serious limitation in Real Time processing): real-time corrections on FE?
- Alternatively, a CFD is needed, which is a complex and power-consuming circuit in systems based on dense small pixel matrices
- It does not have theoretically optimal performance

Source: L. Demaria
TREDI 2019 25/2/19



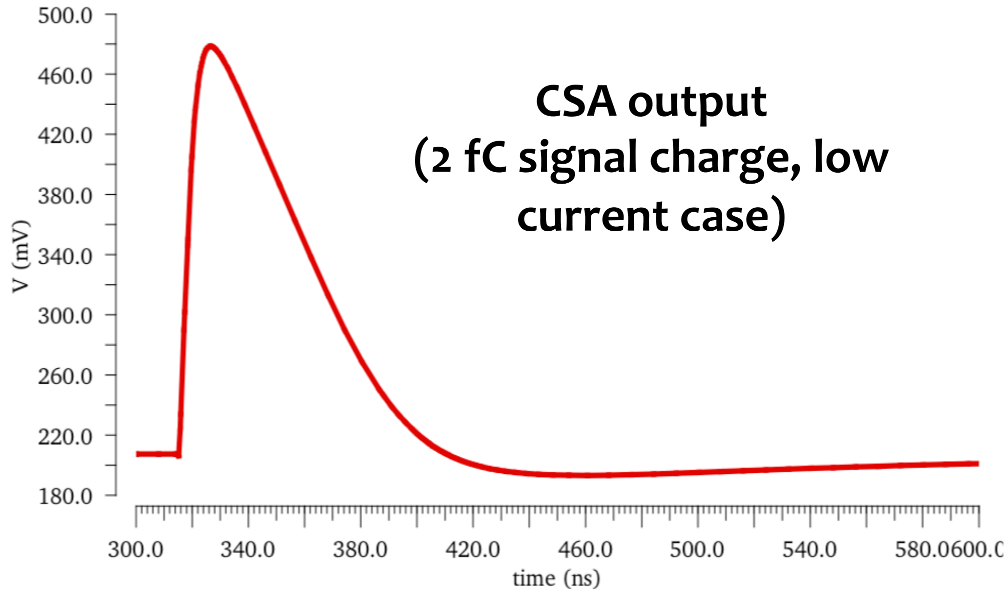
CSA output from RD53A

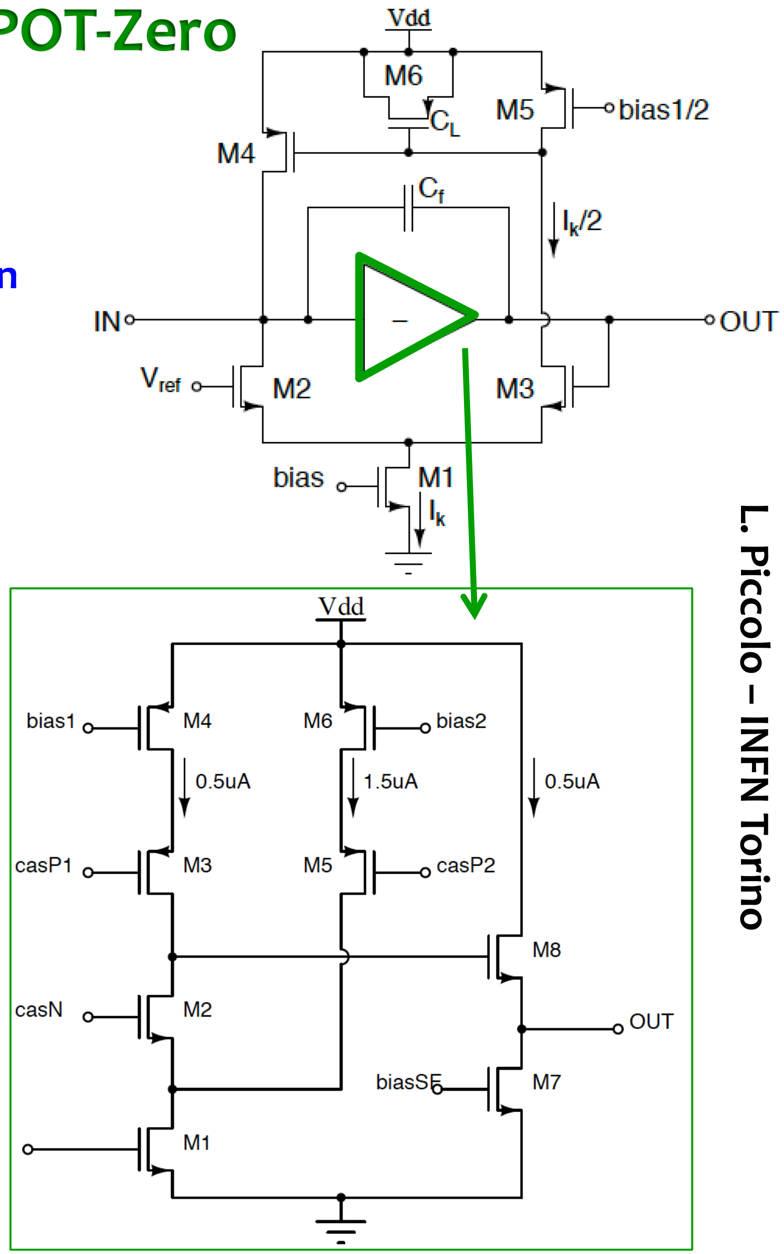
CSA-like implementation

Istituto Nazionale di Fisica Nucleare

0-th prototpype: TIMESPOT-Zero

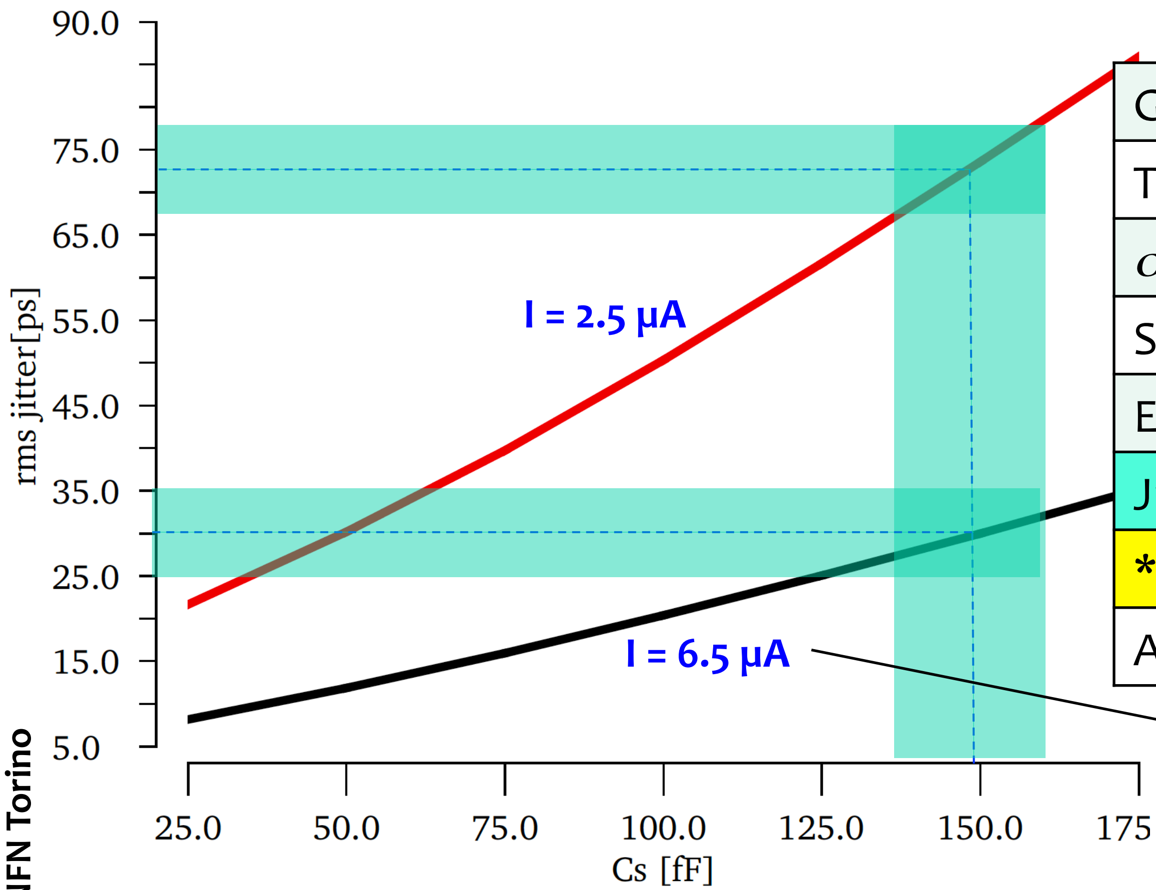
- Output voltage proportional to input charge
- Constant peaking and falling times for better timing
- Low noise
- Krummenacher (active) filter: DC current compensation of input leakage current
- Programmable input MOST current (this prototype)
- Cascodes can be switched on/off to improve S/N ratio (this prototype)
- The Slew Rate (dV/dt) can be increased increasing the current in the input stage by different biasing





L. Piccolo – INFN Torino

CSA-like implementation (2)



σ_t vs C_s(total capacitance of pixel) @ Q_{in} = 2 fC

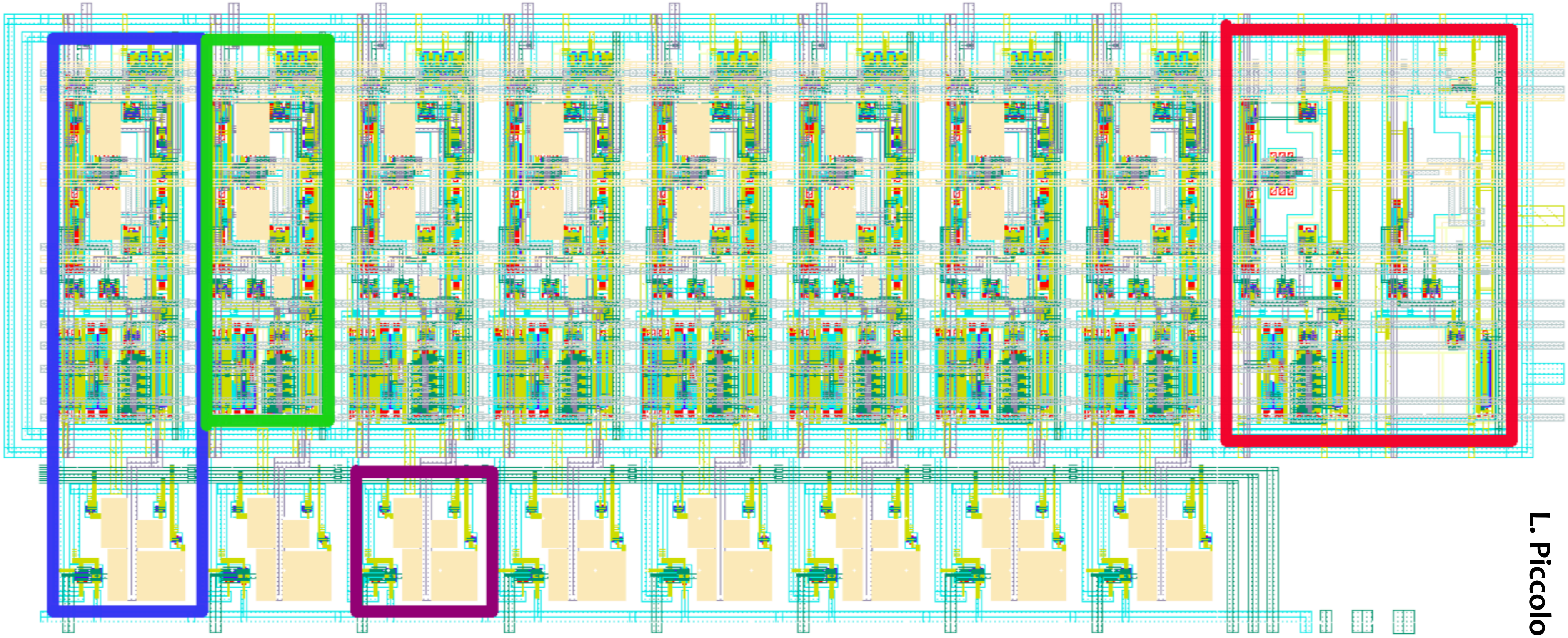
table @ C_s = 150 fF

Gain	199.2	mV/fC
T_{pk}	11.86	ns
σ_N	2.63	mV
SNR	95	
ENC	82	e–
Jitter = σ_N/Vr	62*	ps
*Consumption	2.5	μA
Area (LE D. incl.)	37x14	μm²

Power budget was intentionally kept at its minimum.
We think that there is room for a ~ factor x2
SR, however, is approaching saturation

L. Piccolo – INFN Torino

TIMESPOT-0: FE stage layout



single channel core cell charge injection bias cell

- 8 channels integrated
- Core channel consists in a CSA and a Leading Edge discriminator with offset compensation
- Whole cell sizes 60µm x 150µm (core cell area = 14 x 37 µm² without special care on area optimization)

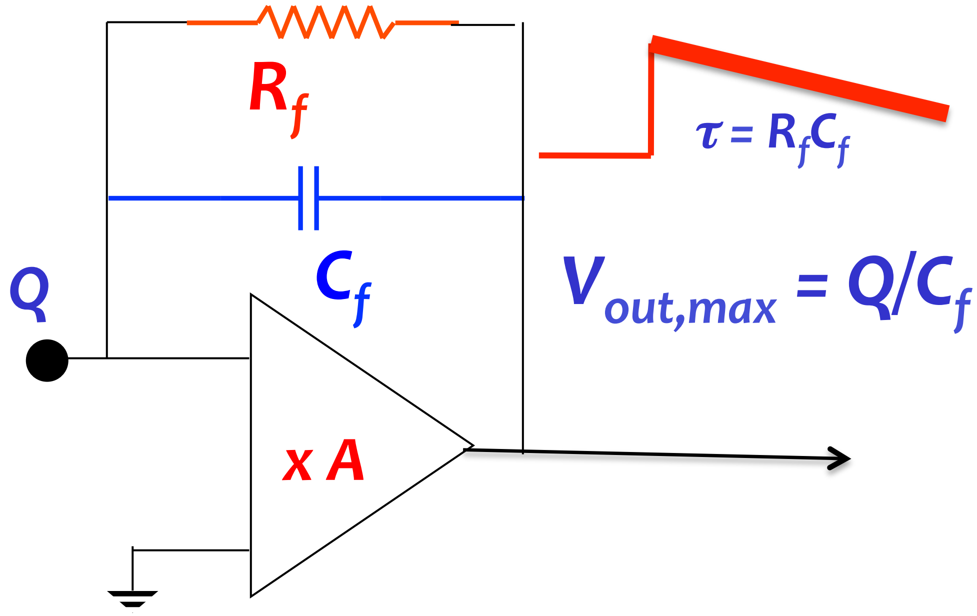
L. Piccolo – INFN Torino

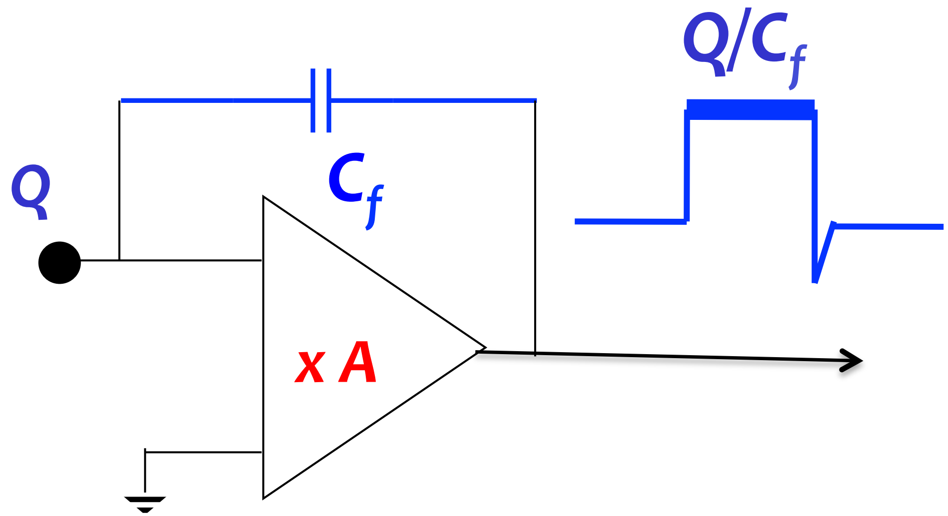
Alternatives to CSA-like amps?

CSA with large R_f :
High SR, but long decay time !

Highest SR → $R_f = \infty$,
Decay time is virtual ∞
→ force V level to zero by means of a dedicated switch

→ Chance of TW correction by ToT is lost
→ Solution suitable only either if TW is made negligible or a CFD is integrated in the pixel (more complexity and power)





Alternatives? (2)

A "perfect" transimpedance amplifier?

Low R_{in}. Current amplifier $I_{in} \rightarrow I_{out} = A \times I_{in}$
But an impedance stage is necessary: RC enters however the game

In order to "follow" the input, the amplifier bandwidth has to be large enough, risking to embark too much noise. Difficult solution for relatively small C_s ($BW_{amp} >> BW_{Sensor+network}$)

Specific solutions are being explored (TIMESPOT-1, 2020 – now under design)

Summary on amplifiers for pixels with timing

Target is to fully exploit the intrinsic sensor time resolution (~ 20 ps) within the given power budget (max 20 μA for front-end stage)

The dilemma: try to beat dispersion with a very steep amplifier response or accept it smoothly and try to compensate it afterwards?

The CSA-like solution with constant slope discharge appears as a good enough solution, difficult to beat, although it does not reach the ideal performance. In particular, it provides an effective way to back-correct for TW using the ToT. Specific algorithms at the pixel level must be developed to obtain real-time time measurements (additional power!).

Alternative solutions can be envisaged and are being explored. Specific system optimization within the given resources is necessary. A "universal" solution is not there!

Pixels with timing:
the TDC

benchmarks & limitations

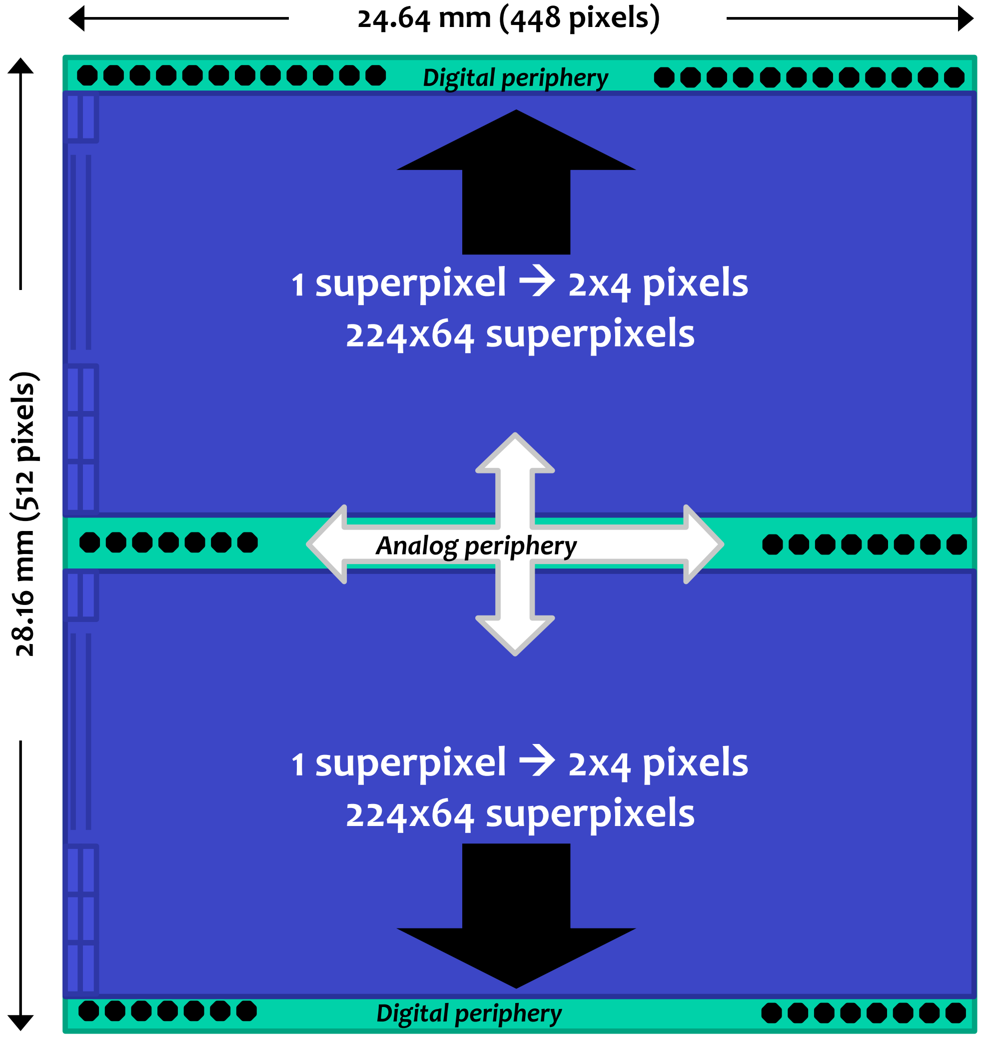
Reaching 20 ps rms on a TDC is not a terrible task.
Things are different within limited area and power budgets!

TIMEPIX4: Floorplan

Source: X. Llopart
IOP meeting on pixels with timing – October 2017

- Chip size 28.16mm x 24.64 mm
- 512 x 448 → 229376 pixels
- Pixel size 55μm x 55μm
- Analog Periphery (800 μm):
  - BandGap + Temperature sensor
  - Biasing DACs
  - Monitoring ADC
  - Analog supply
  - Digital supply
- 2 x Digital Periphery (400 μm):
  - 8 x 5.12Gbps serializers
  - PLL(s)
  - Analog supply
  - Digital supply
- 2 x Pixel matrix (13.28 mm x 24.64mm):
  - 256 x 448 pixels 55 μm x 51.875 μm
  - 5.68% smaller than 55 μm x 55 μm
  - RDL has to compensate up to 400 μm

CMOS 65-nm, under (advanced) stage of design



1 TDC shared among 8 FE channels

Counts < 0.2 GHz/cm²

200 ps resolution

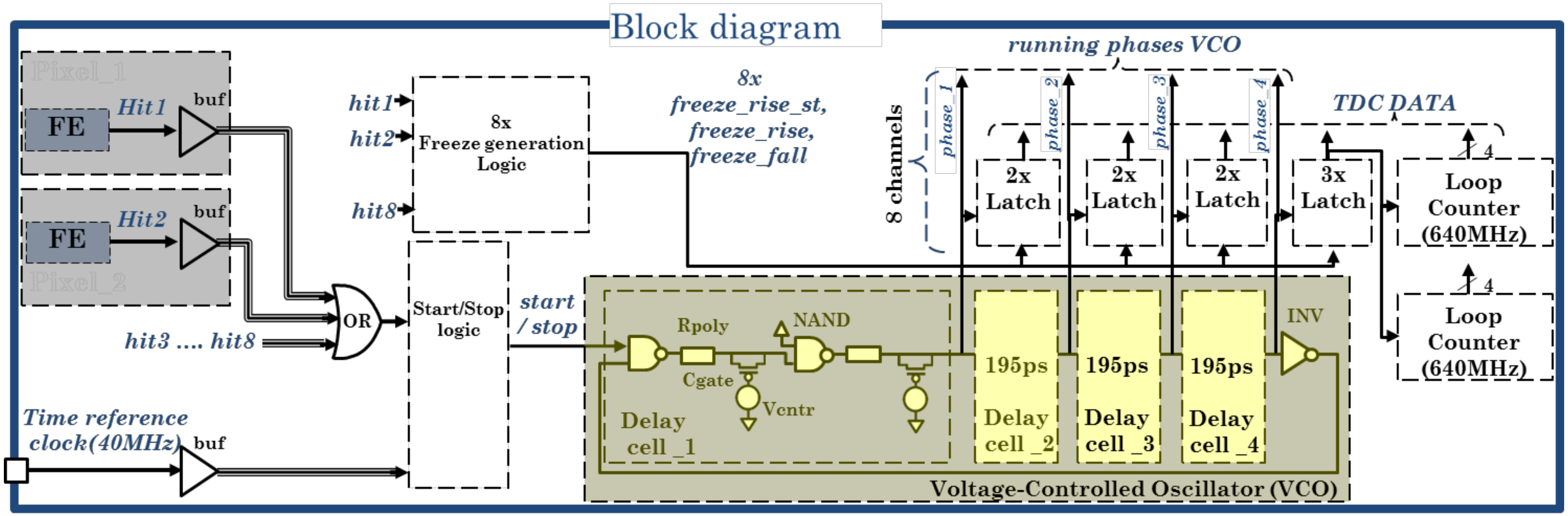
σ_{jitter} ~ 40 ps (5σ)

4 side abutable ! Using TSV

TIMEPIX4: on-pixel < 200ps time res.

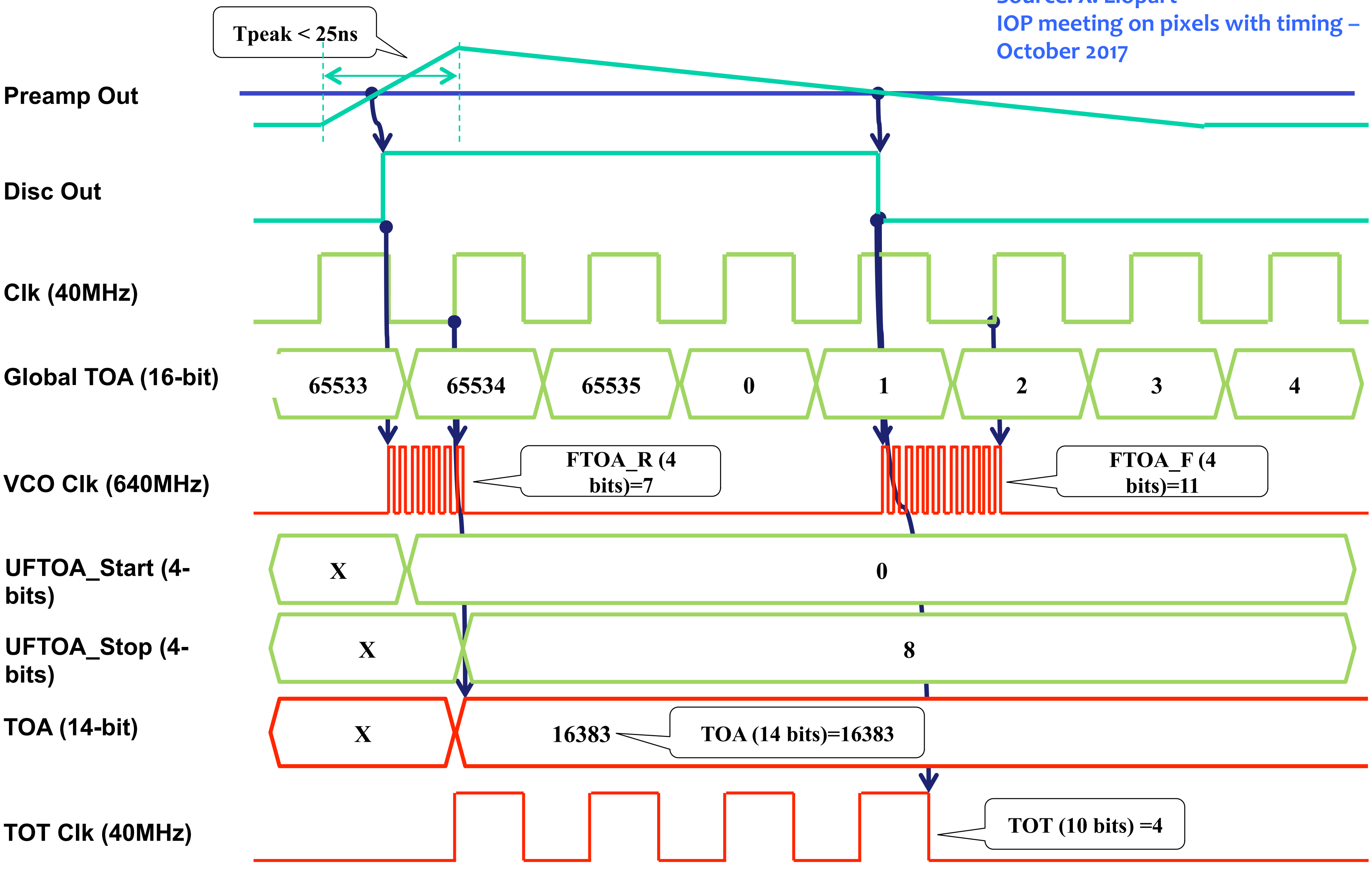
Source: X. Llopart IOP meeting on pixels with timing – October 2017

- Share a 640MHz VCO among 8-pixels:
  - Oscillation frequency locked (V_{ctrl}) with periphery PLL for PVT control
  - 1.56 ns resolution (as in Timepix3)
  - 195 ps obtained latching the internal VCO phases
- Column eDLL to distribute the 40MHz
  - Controlled skew on the stop signal (<100ps)
  - Minimizes noise from pixel matrix clock distribution



TIMEPIX4: ToA & ToT

Source: X. Llopart
IOP meeting on pixels with timing – October 2017



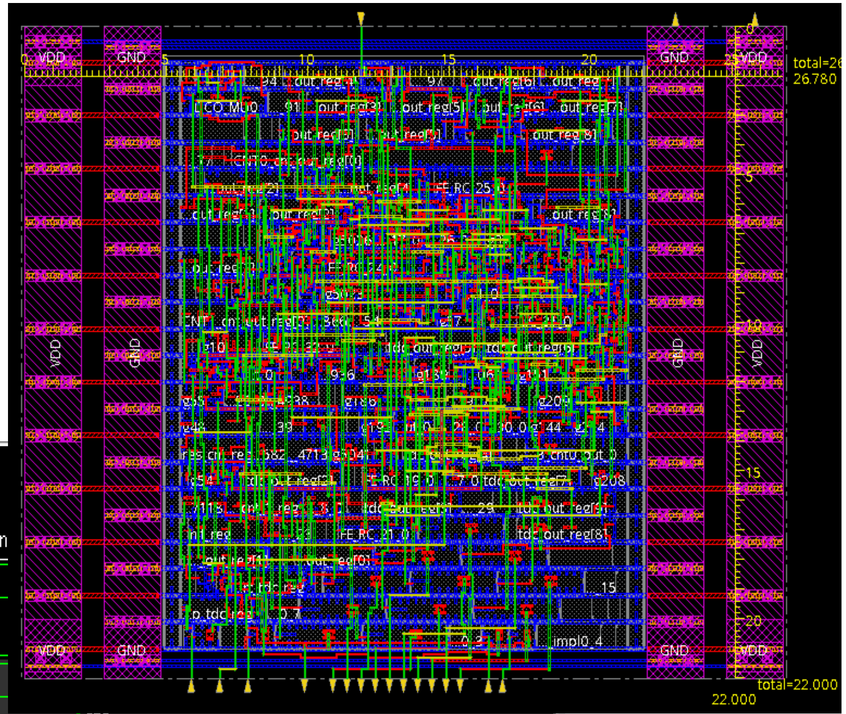
INFN
Istituto Nazionale di Fisica Nucleare

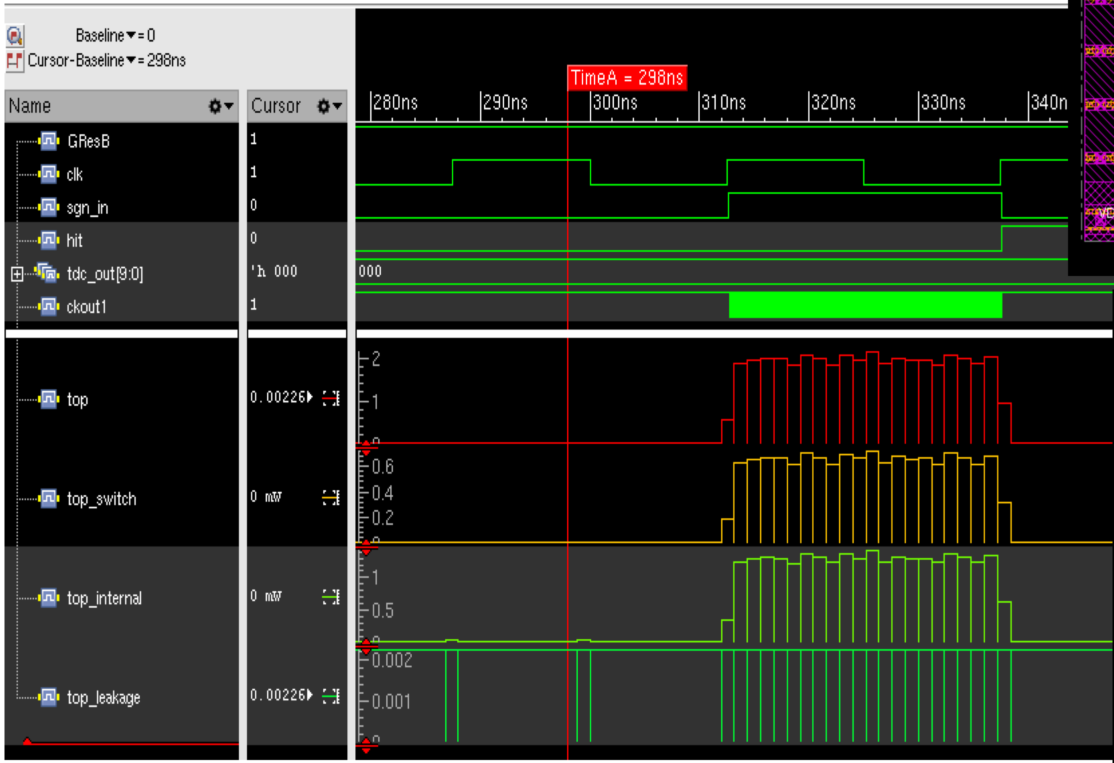
TIMESPOT-zero

CMOS 28-nm

TimeSPOT
TIME and SPace real-time Operating Tracker

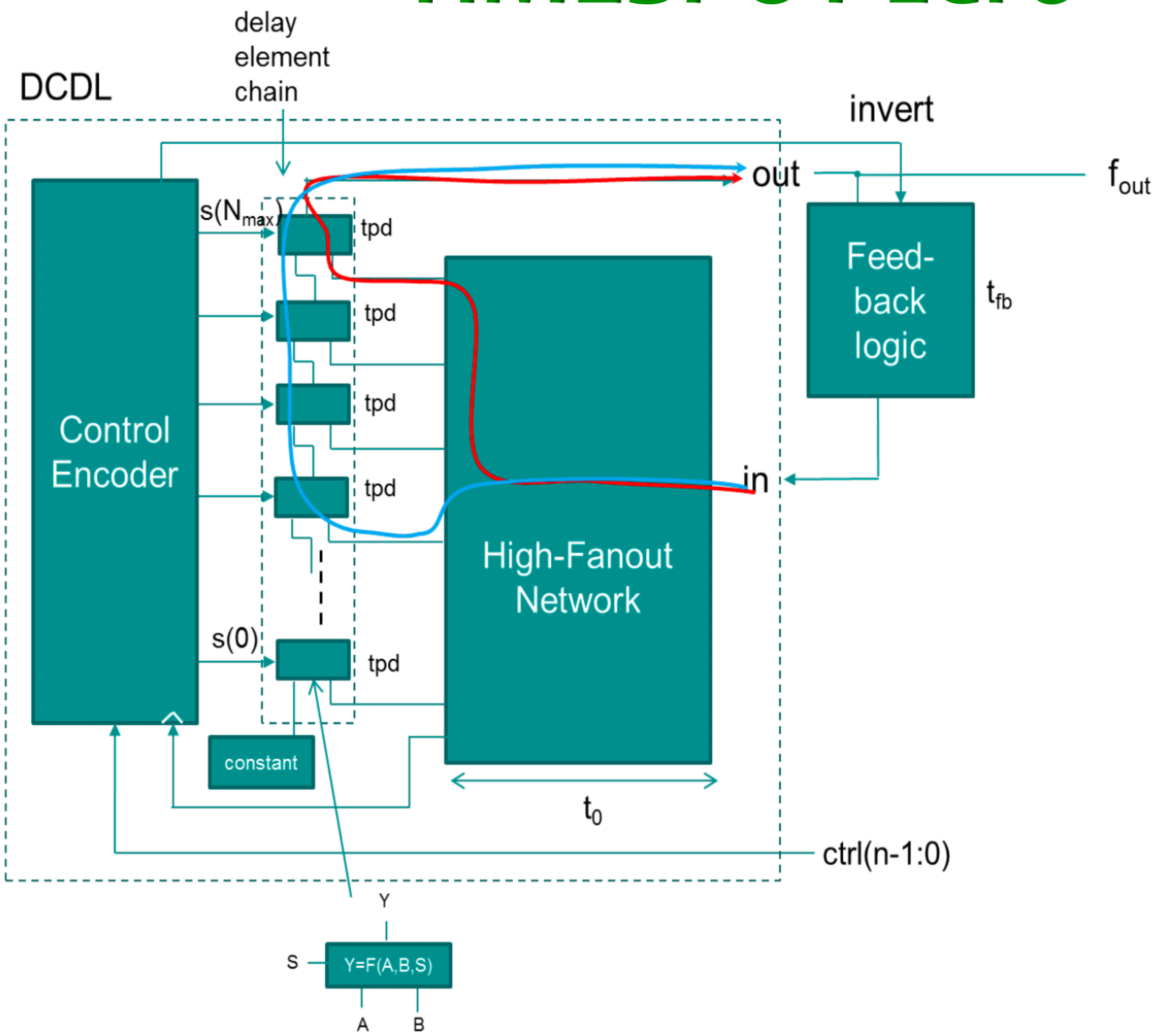
- The (two) TDC designs are based on a "ALL digital fully-synthesizable design"
- The DCO is standard-cell based
- DCO is enabled only on the occurrence of a hit for lower noise and consumption
- 1 TDC per pixel is possible





Master Clk	40	MHz
Resolution (LSB)	50	ps
Resolution(rms)	15	ps
NOB	10	bits
Area	**20x15**	μm^2
Power (conversion)	**1.5**	mW
Power (stand-by)	10	μW

TIMESPOT-zero



Fully Digitally Controlled Delay Line

Exploits the intrinsic propagation delays of the library gates

Fully synthesizable from schematic + clock distribution directives for place and route.

Easily migrated from 130 nm to 65 nm to 28 nm

Drawback: it feels the leakage current of high speed grade transistors in 28-nm (high power also in stand-by conditions)

So-called Giordano's DCO – patented by our group.
See for example: S. Cadeddu et al., *High Resolution Synthesizable Digitally Controlled Delay Lines*, IEEE TNS vol 62 No. 6, Dec 2015

Conclusions

Endowing pixel circuits with high resolution timing facilities is a hard task. The task is even harder in real-time systems

Usually, system limitations (power, in particular) oblige to important compromises in performance

Some good solutions exist in principle, but no device having the complete set of specifications exists yet

Passionate work is ongoing in this years to conceive a new concept of tracking detector and realize it within one decade or so

Many thanks for your attention !