CMOS Active Pixel Sensors for Particle Physics

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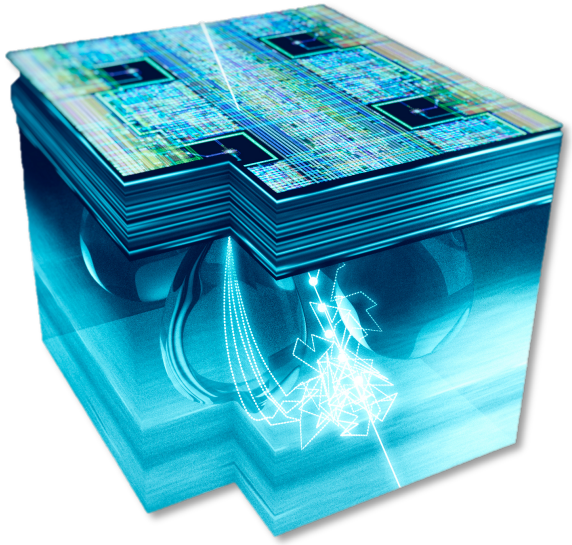
XXIX Giornate di Studio
SUI RIVELATORI
SCUOLA FRANCO BONAUDI



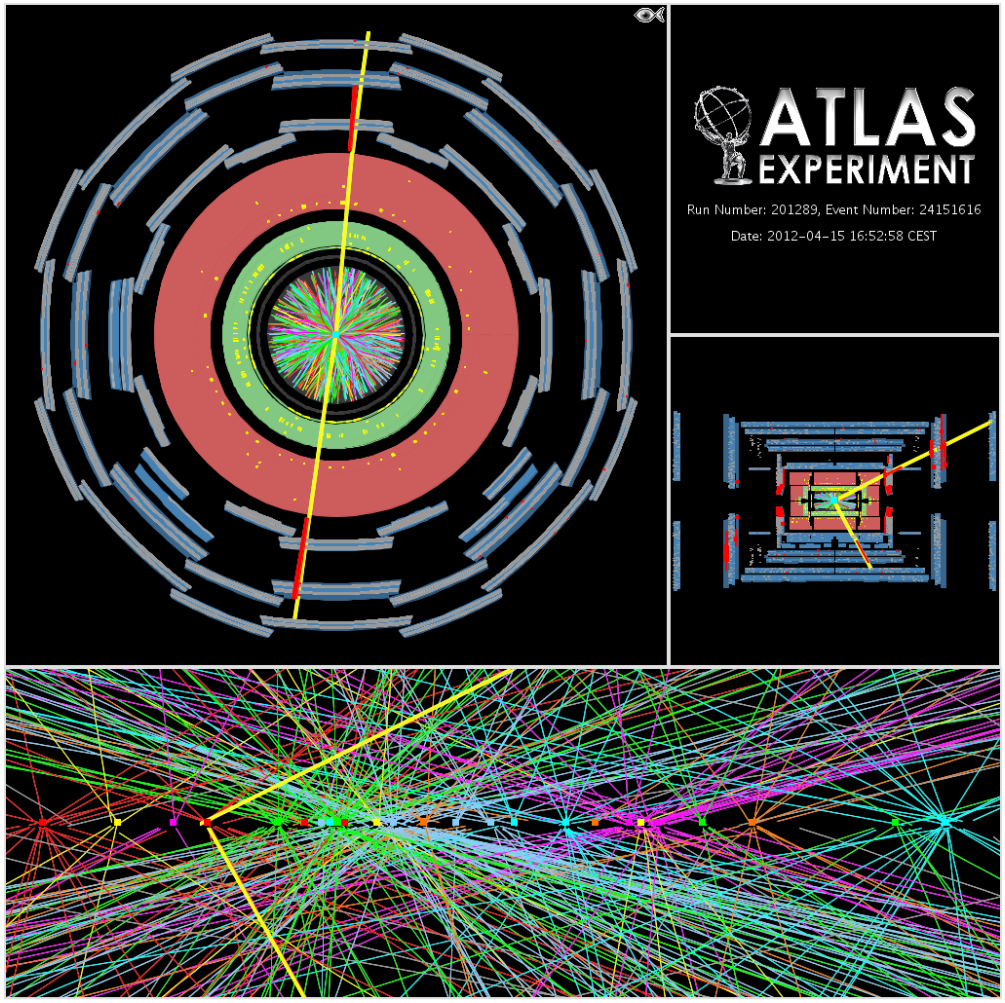
Outline

1. Prelude
   - silicon tracking detectors in HEP experiments
   - Silicon trackers – a brief historical excursus
2. Silicon properties – a brief reminder
3. Silicon detectors – basic principles
4. CMOS Active Pixel Sensors – advent and basic principles
5. First application of CMOS to Vertex Detectors for HEP
6. Fully Depleted MAPS – improve speed and radiation hardness
7. Novel Developments

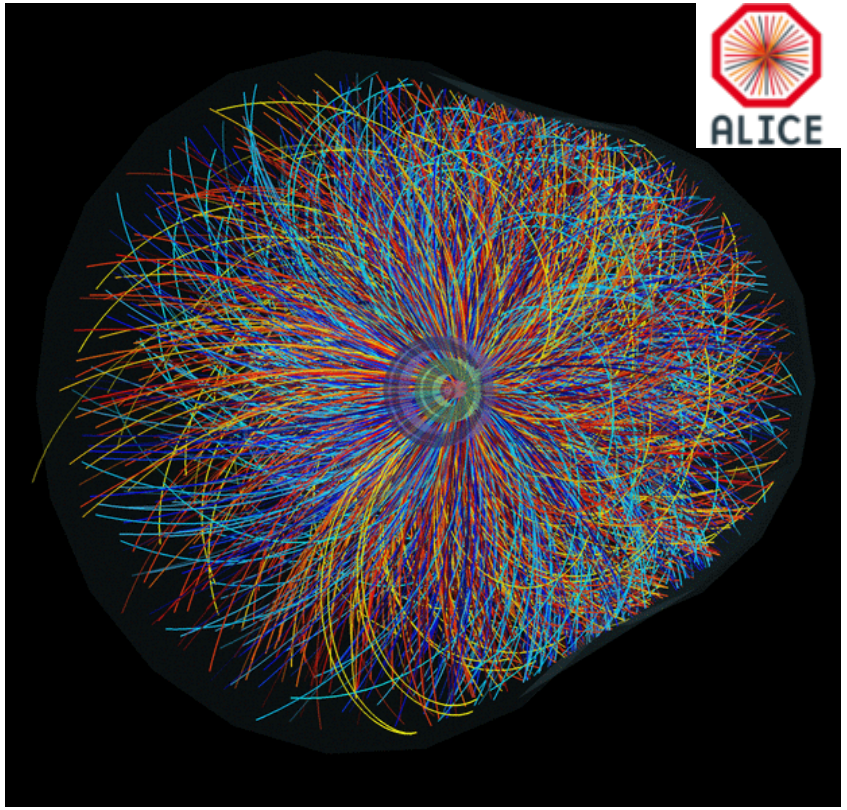
Prelude

Tracking Detectors in HEP Experiments

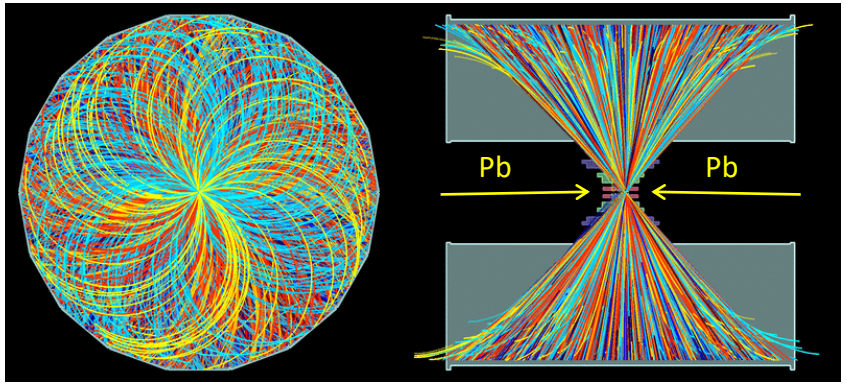
Silicon Trackers – Key to solve complex events close to IP



LHC pp collisions: a candidate Z boson event in the dimuon decay with 25 reconstructed vertices (ATLAS, April 2012)

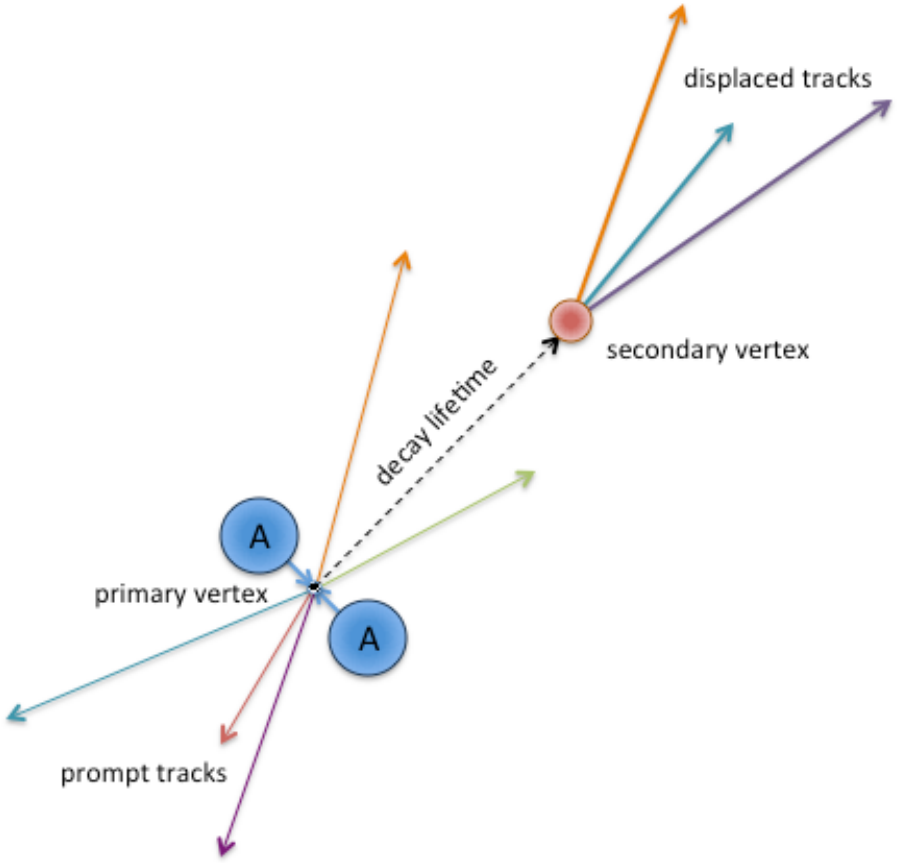


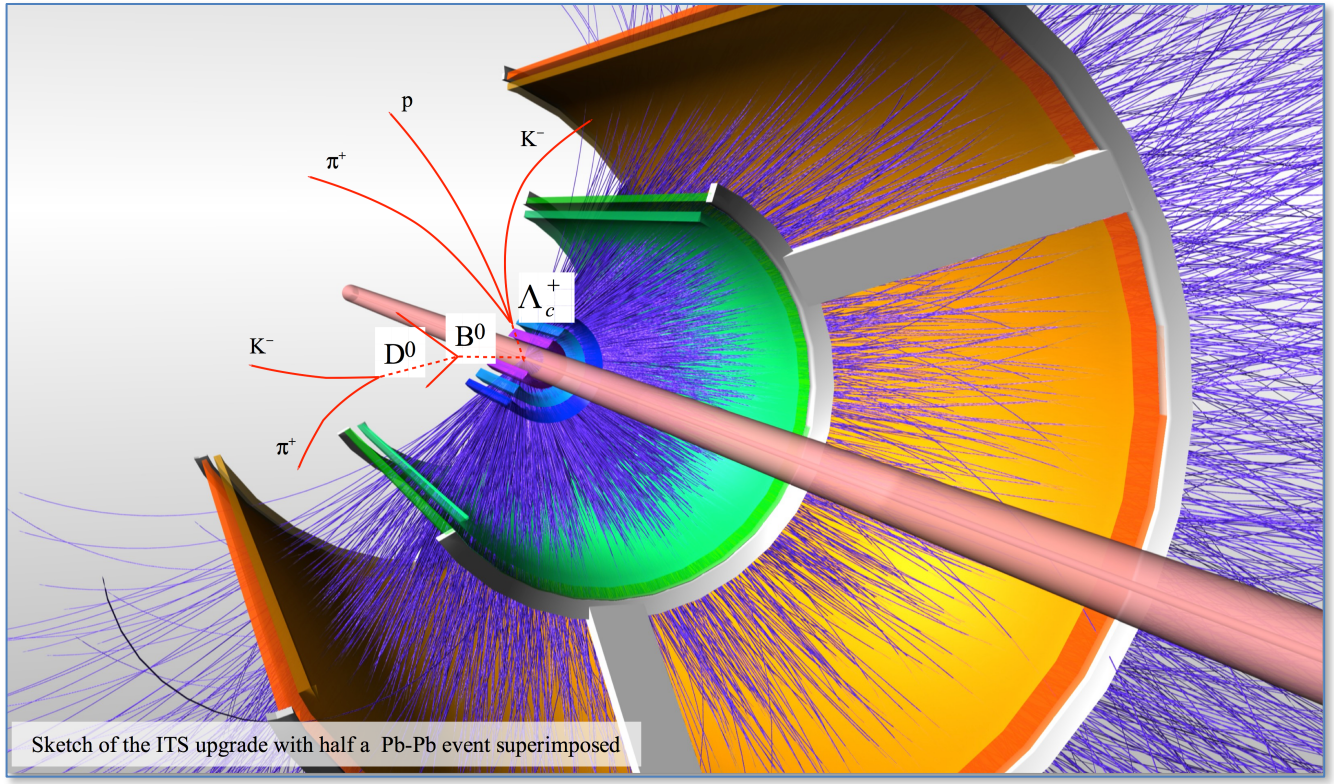
LHC Pb-Pb collision (ALICE, Sep 2011)



Measurement of the decay topology of short-lived particles

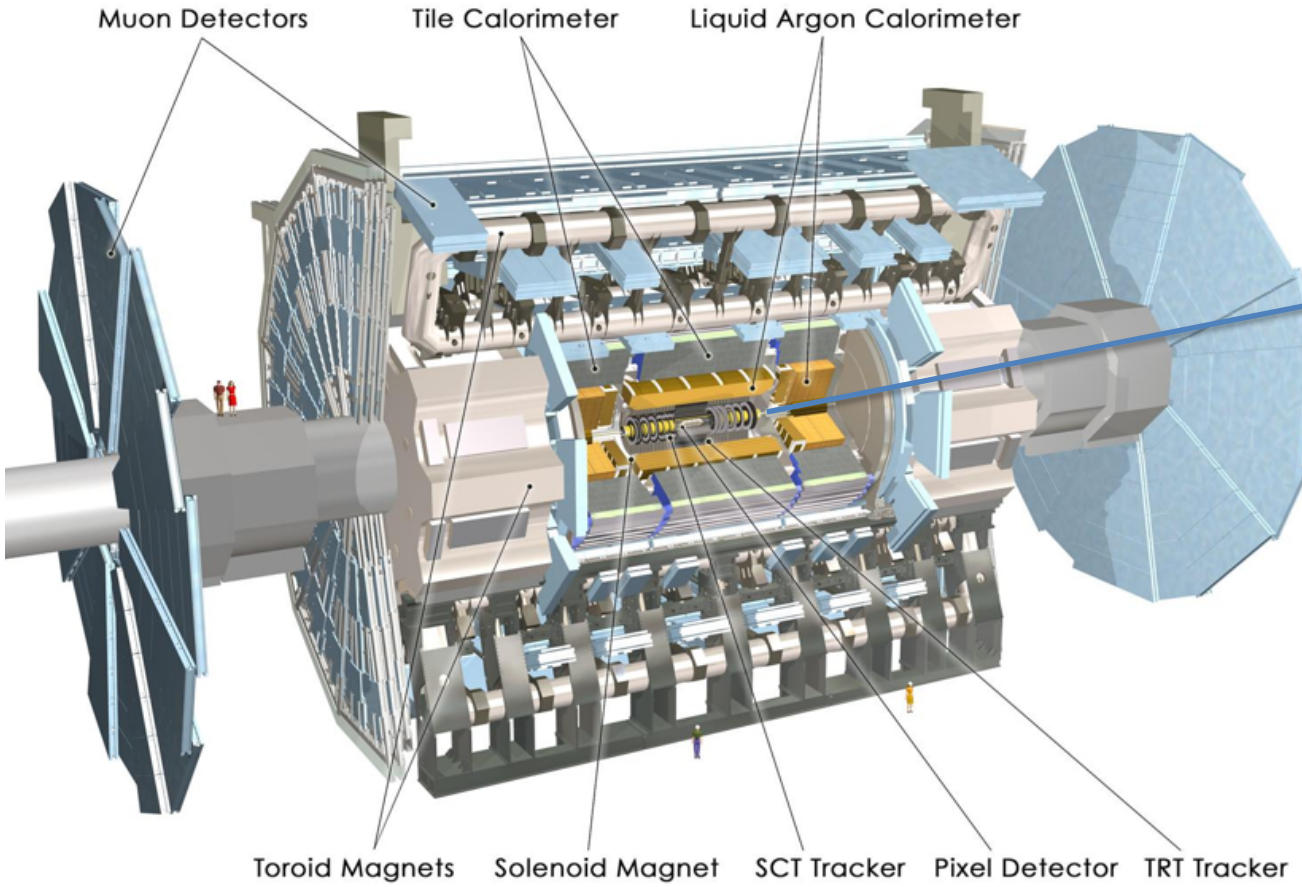
The first detection layers, the closest to the IP, are crucial for the measurement of the interaction vertex (primary) and the decay vertex of short-lived particles (secondary)

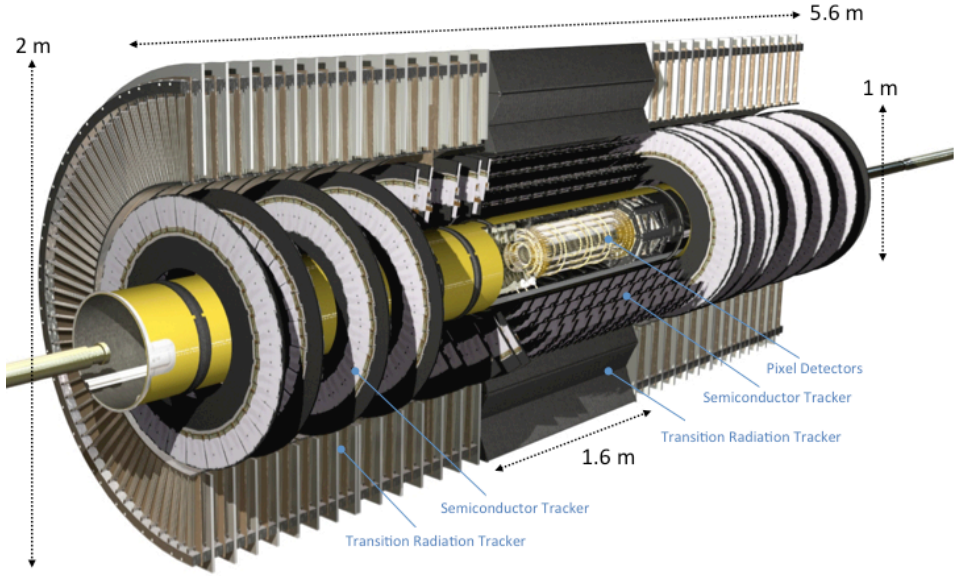




Typical (proper) decay length of charm and beauty hadrons: ≈100μm and ≈500μm respectively

Central Trackers at the LHC Experiments





ATLAS Tracker

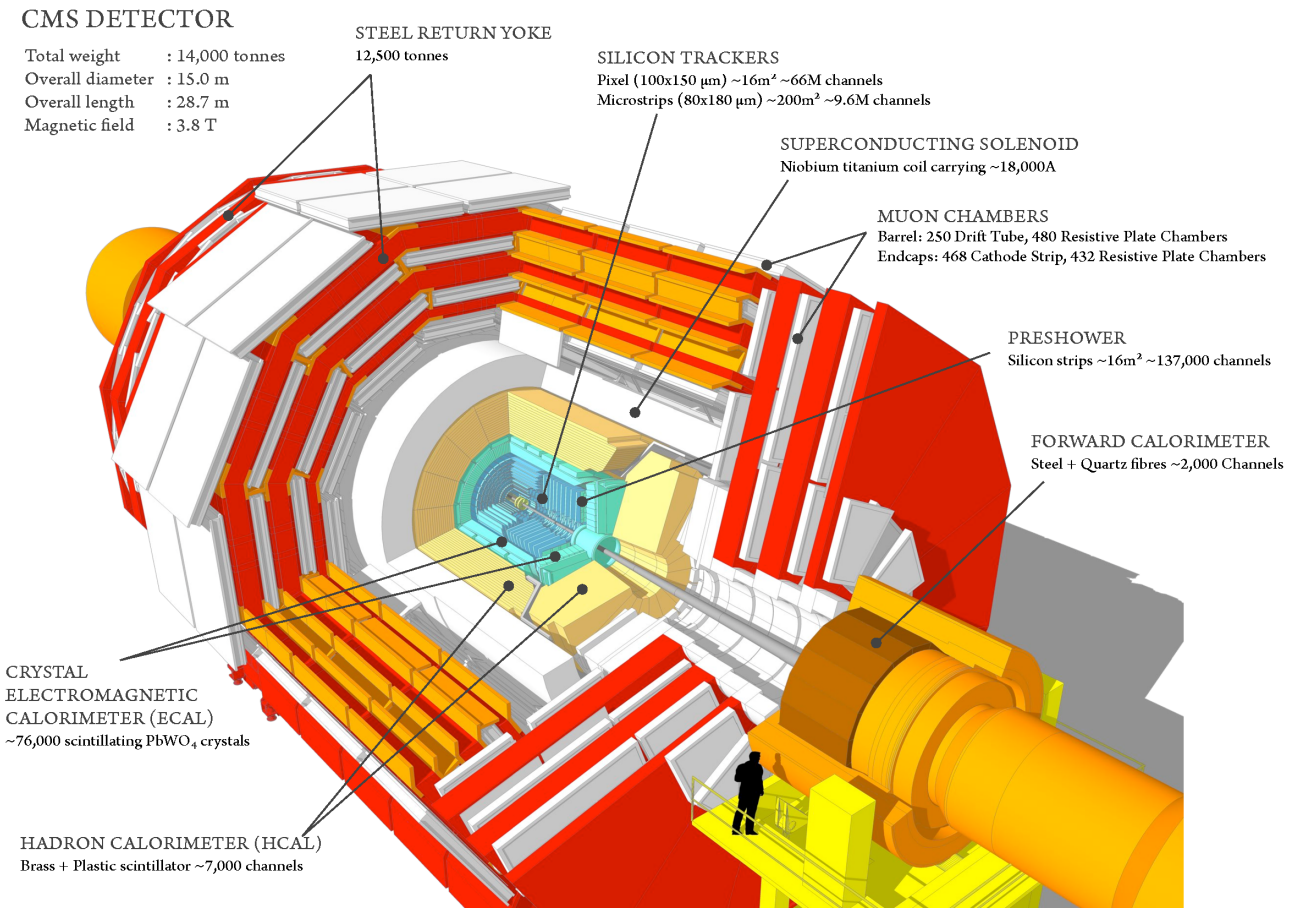
Si-pixel, Si strip, TRT (gas, transition radiation)

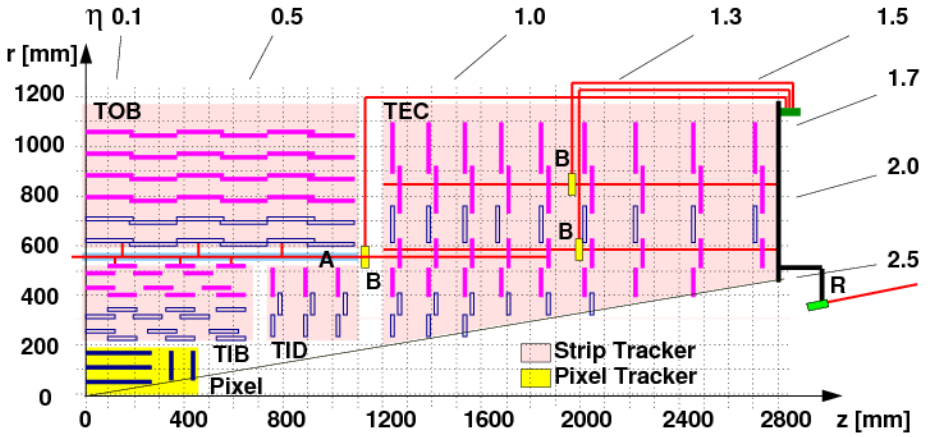
Phase-I upgrade: one more Si-pixel layer (IBL)

Phase-II upgrade: Si pixel + Si Strip (entirely new)

≈ 200 m^2 silicon strips

Central Trackers at the LHC Experiments





CMS Tracker

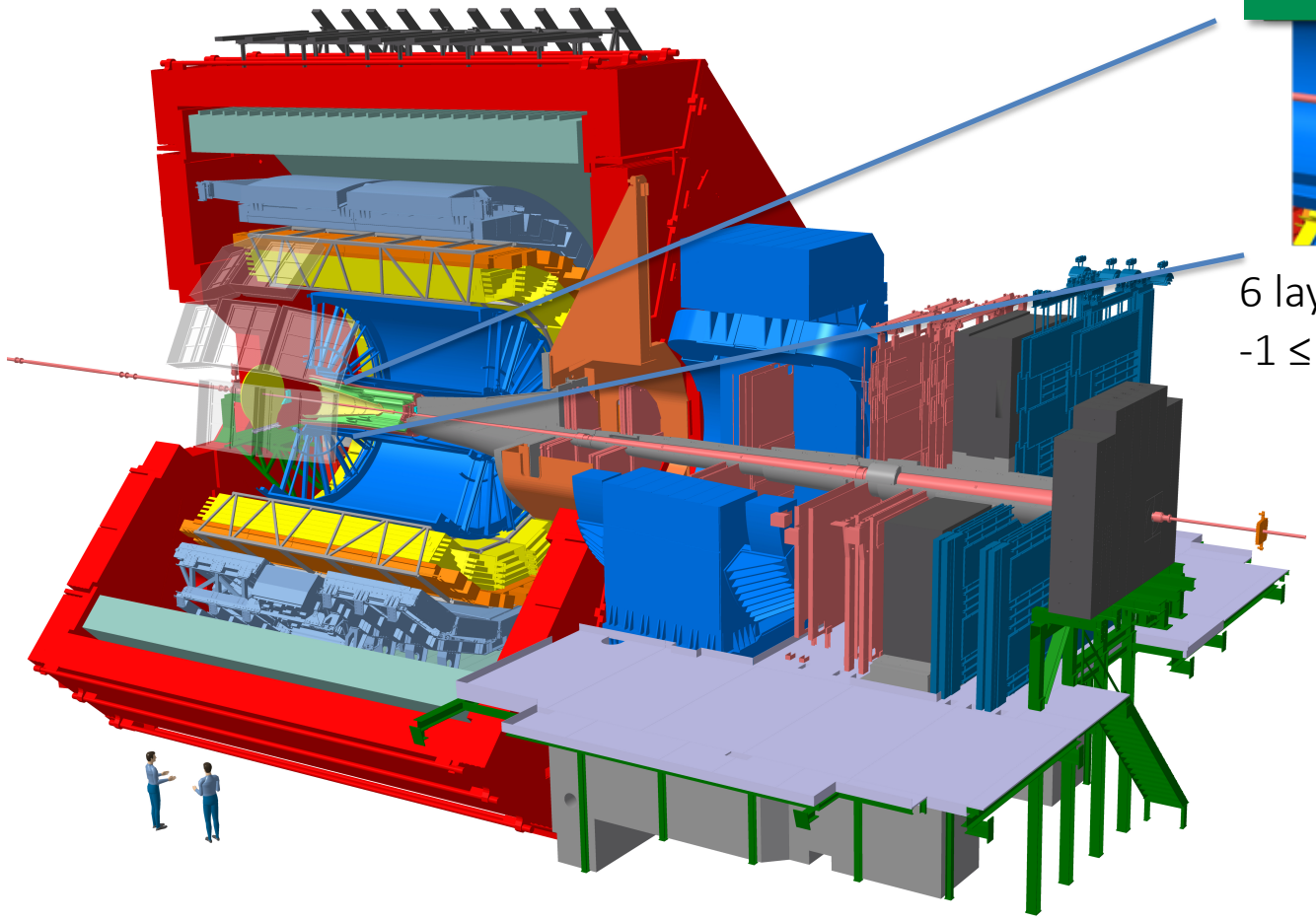
Si-pixel, Si strip ⇒ **All silicon**

Phase-I upgrade: replacement of Si-pixel

Phase-II upgrade: Si pixel + Si Strip (entirely new)

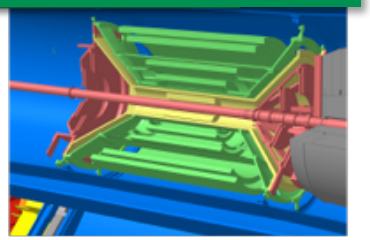
≈ 200 m^2 silicon strips

Central Trackers at the LHC Experiments



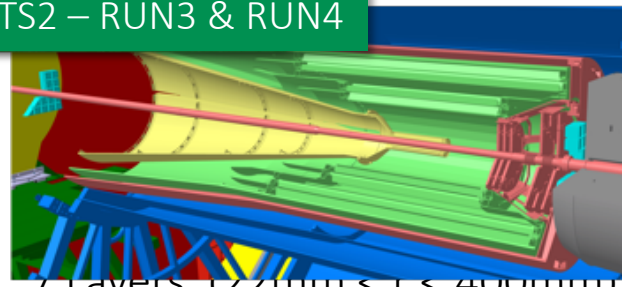
ALICE Inner Tracking System (ITS)

ITS1 – RUN1 & RUN2



6 layers (39mm < r < 440mm)
$-1 \leq \eta \leq 1$

ITS2 – RUN3 & RUN4



7 layers (22mm < r < 400mm)
$-1.3 \leq \eta \leq 1.3$

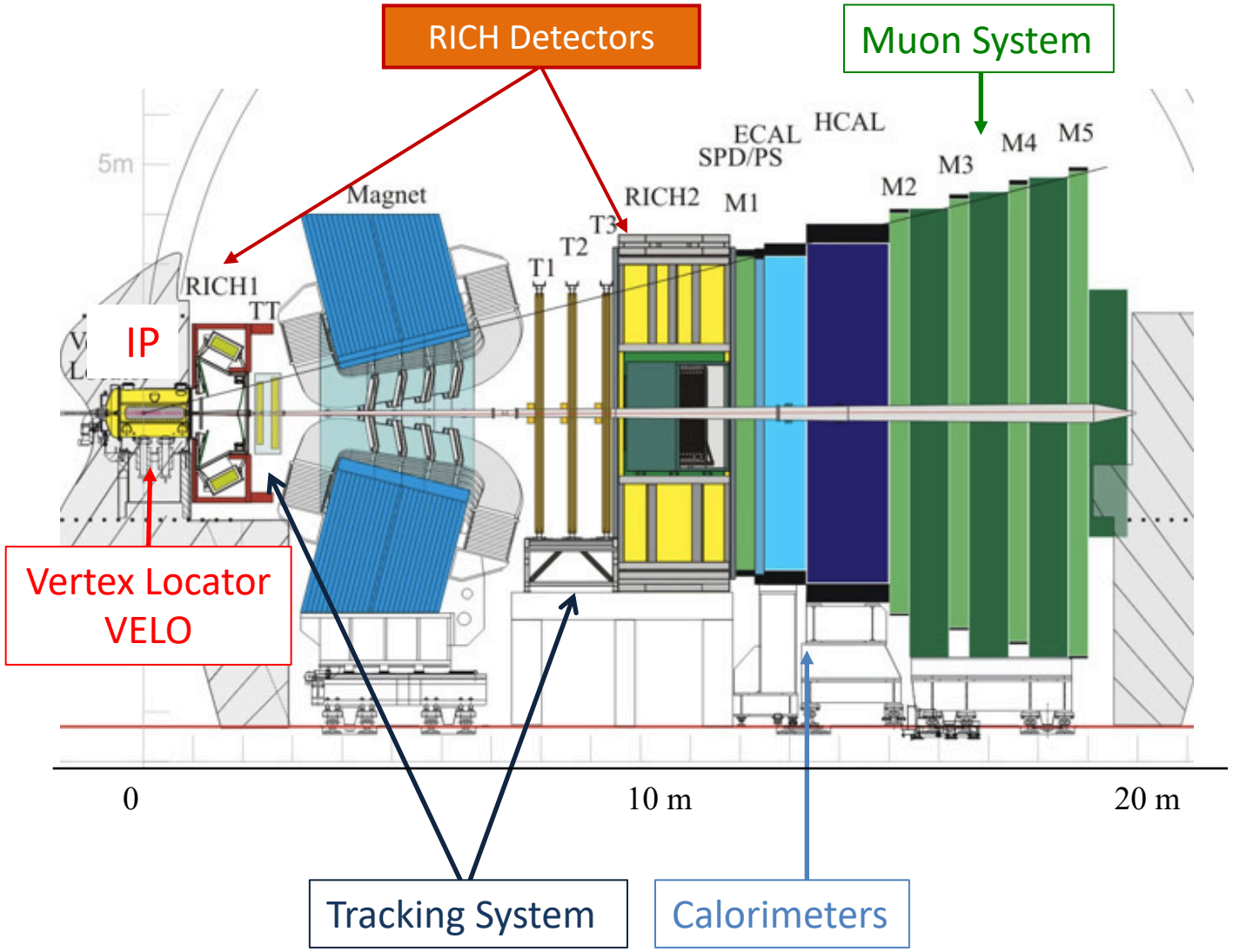
ALICE Tracker

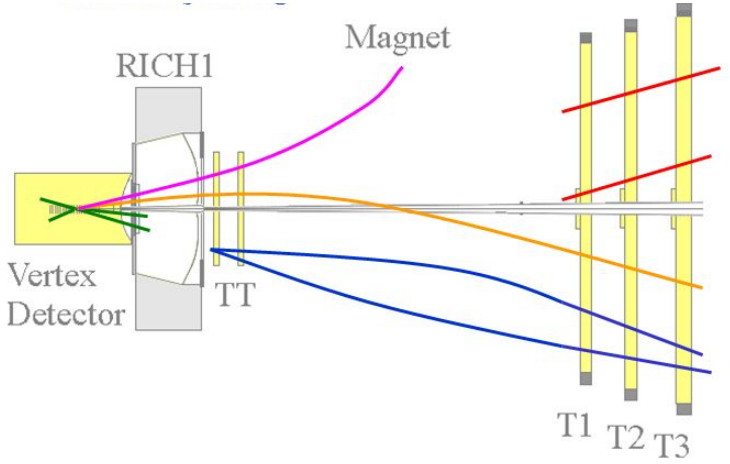
Si pixel, Si drift, Si strip, TPC (gas), TRD (gas, trans. rad.)

Phase-I upgrade: MAPS + TPC & TRD (new readout)

10 m^2 silicon pixels

Central Trackers at the LHC Experiments





LHCb Tracker

Si strips (VELO), silicon+straw tubes

Phase-I upgrade: Si pixel, scintillating fibers

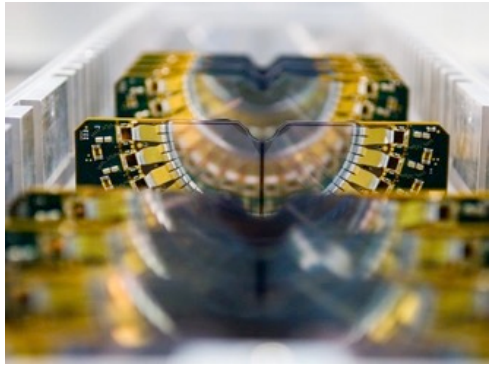
Pixels to cope with higher particle rates

Silicon detectors at the hart of all LHC experiments

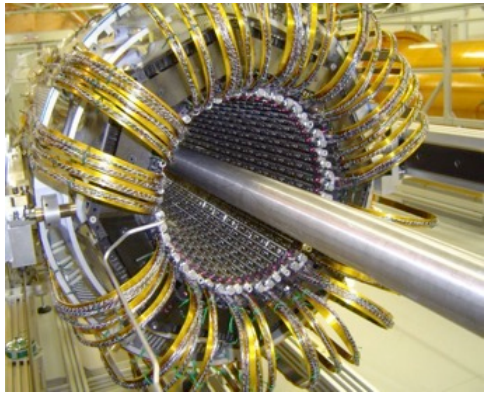
Complex systems operated in a challenging high track density environment

Innermost regions usually equipped with pixel detectors

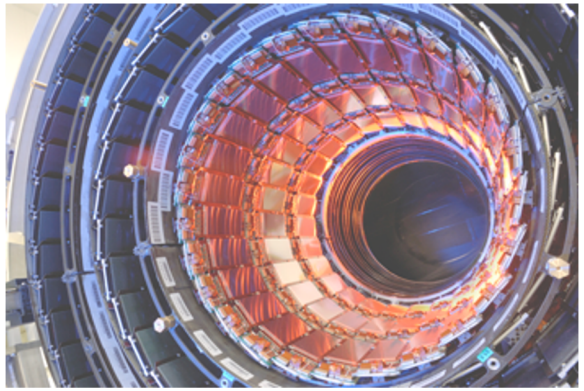
ALICE Pixel Detector



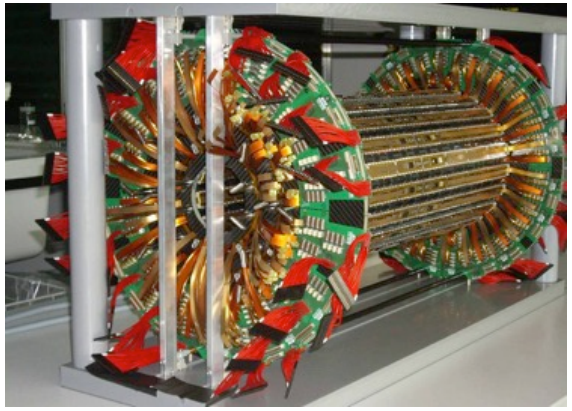
LHCb VELO



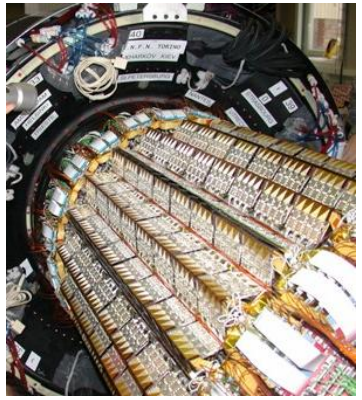
ATLAS Pixel Detector



CMS Strip Tracker IB

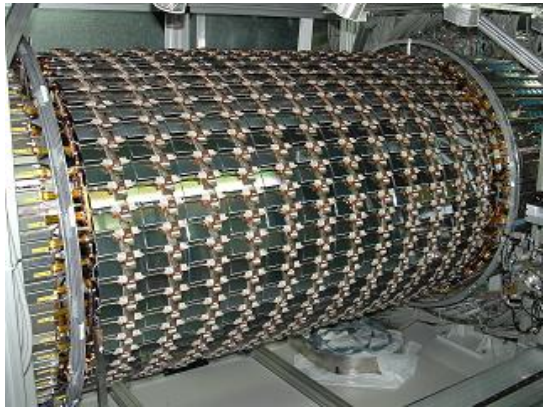


CMS **Pixel** Detector



ALICE Drift Detector

ALICE Strip Detector



ATLAS SCT Barrel

Prelude

Silicon Trackers

A Brief Historical Excursus

The rise of silicon detectors in HEP

Towards end of 1970's: intensive R&D on devices which could measure short-lived particles (10^{-12} - 10^{-13} s)

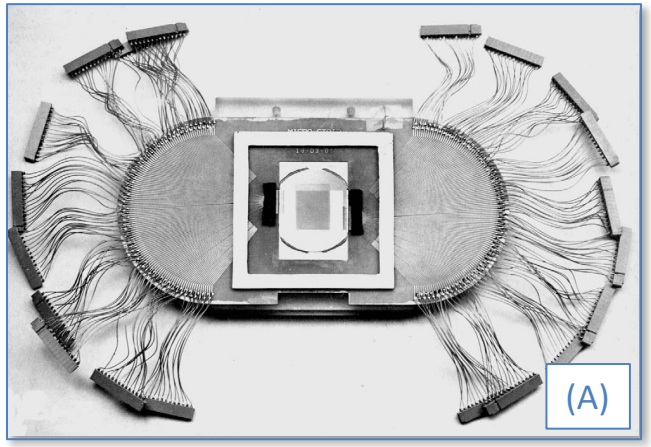
R&D at CERN(A) and Pisa(B) demonstrated that strip detectors (100-200μm pitch):

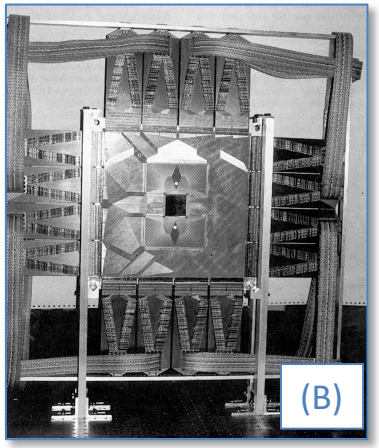
- high detection efficiency (>99%), good spatial resolution (~20μm) and good stability
- precise vertex reconstruction

However: fabrication of these devises was very tricky, thus limiting their availability

1980 – fabrication of silicon detectors using standard IC planar process (PIN diode ➔ μstrip detector)

J. Kemmer, et al., *"Development of 10-micrometer resolution silicon counters for charm signature observation with the ACCMOR spectrometer", Proceedings of Silicon Detectors for High Energy Physics, Nucl. Instr. and Meth. 169 (1980) 499.*





First use of silicon strips detectors by NA11(CERN SPS) and E706 (FNAL)

(A) NA11 (1981): 6 planes (24 x 36mm^2): resistivity 2-3 kΩcm, thickness 280μm, pitch 20μm

(B) E706 (1982): 4 planes (3x3 cm^2) + 2 planes (5x5cm^2)

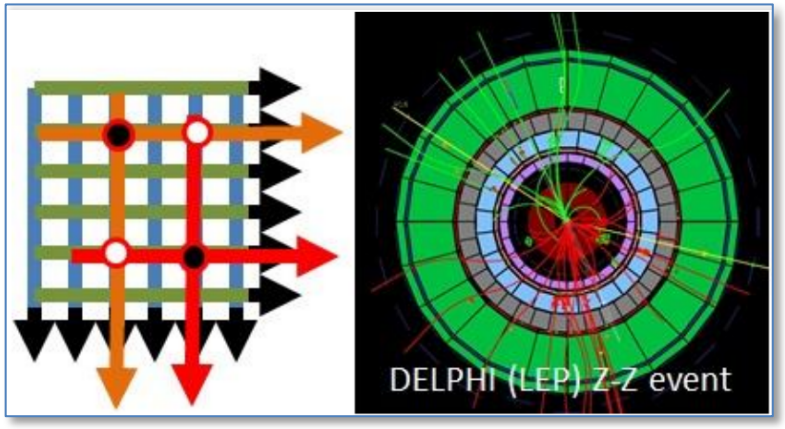
Erik Heine, Joseph Kemmer and Gherard Lutz: 2017 EPS prize for "Outstanding Contributions to HEP" (pioneering the development of silicon μstrip)

The rise of silicon detectors in HEP

The next step forward came with the advent of the VLSI technology that allowed coupling ASIC amplifier chips directly to the detectors

1990s - LEP, first silicon vertex detectors were installed in DELPHI and ALEPH experiments, then OPAL and L3

1989 - first DELPHI vertex detector, consisting of two layers of single-sided strip detectors



Projective geometry ➔ ambiguity at high multiplicities (high occupancy)

This started to become apparent already at DELPHI:

- High number of ambiguities ➔ reconstruction efficiency suffered a lot, especially in the forward direction

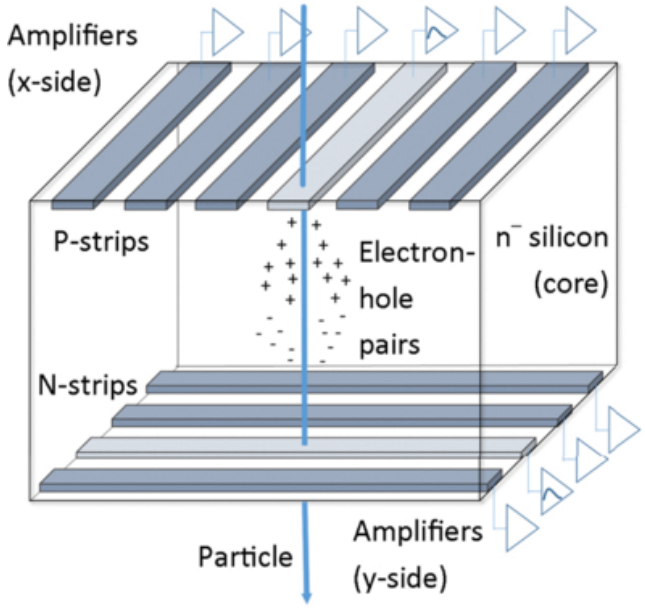
Not usable close to IP in hadron colliders (LHC) or HI experiments at SPS

Another problem at (very) high particle load ➔ degradation of the sensor by the high radiation load

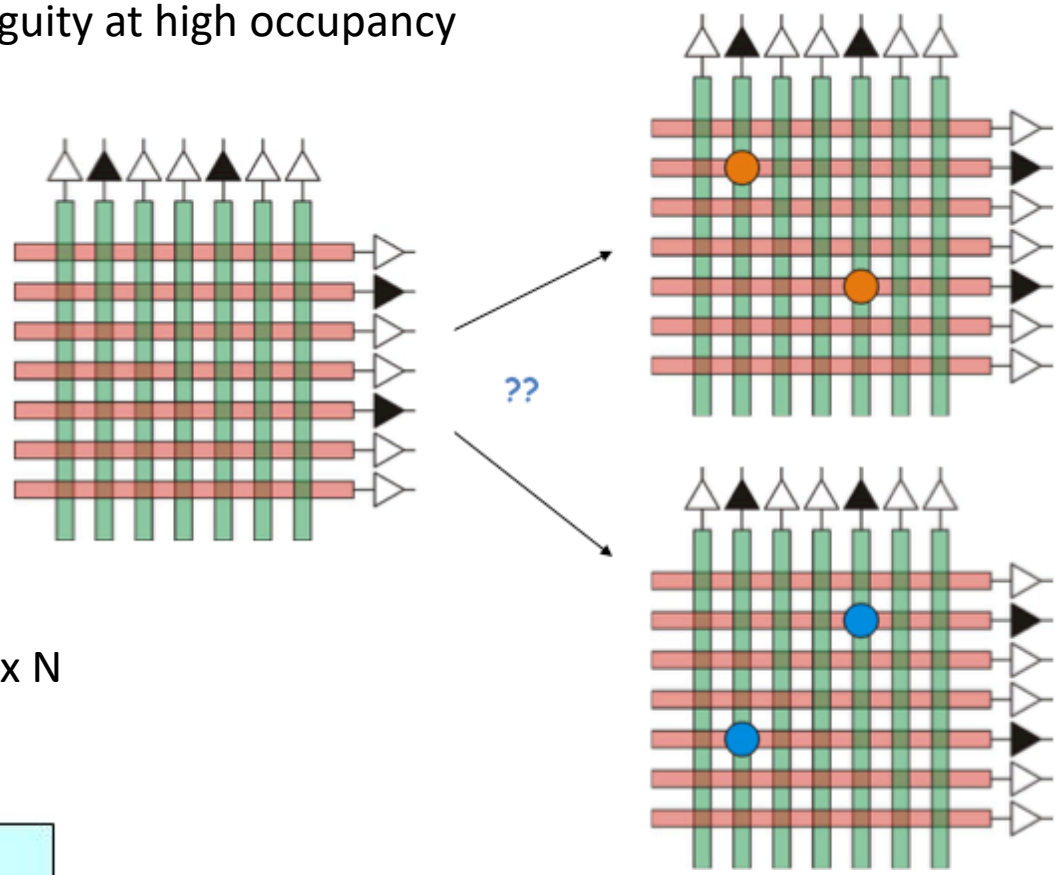
This implies starting with a very large signal-to-noise ratio, which can only be obtained with detector with small capacitance

Silicon Strips – Ambiguity at High Occupancy

Double Sided Strip Detector (DSSD)

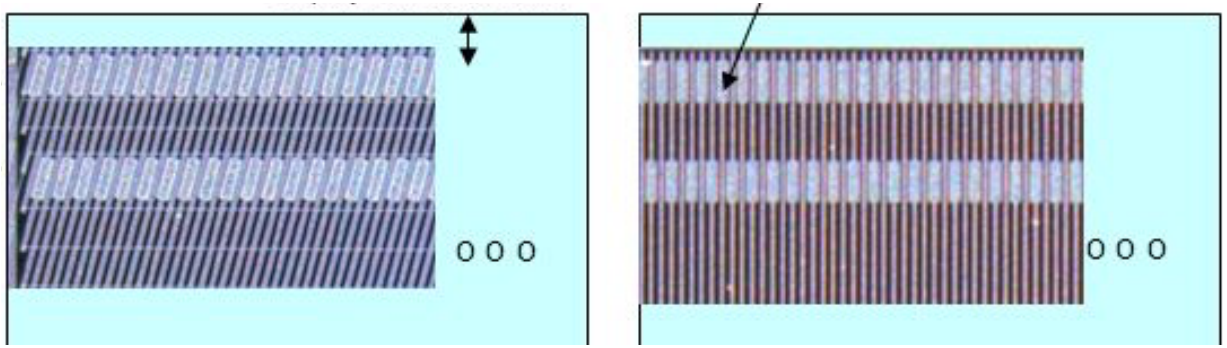


Ambiguity at high occupancy



Nr. channels = 2 x N

Double sided silicon strips for the CBM (FAIR)

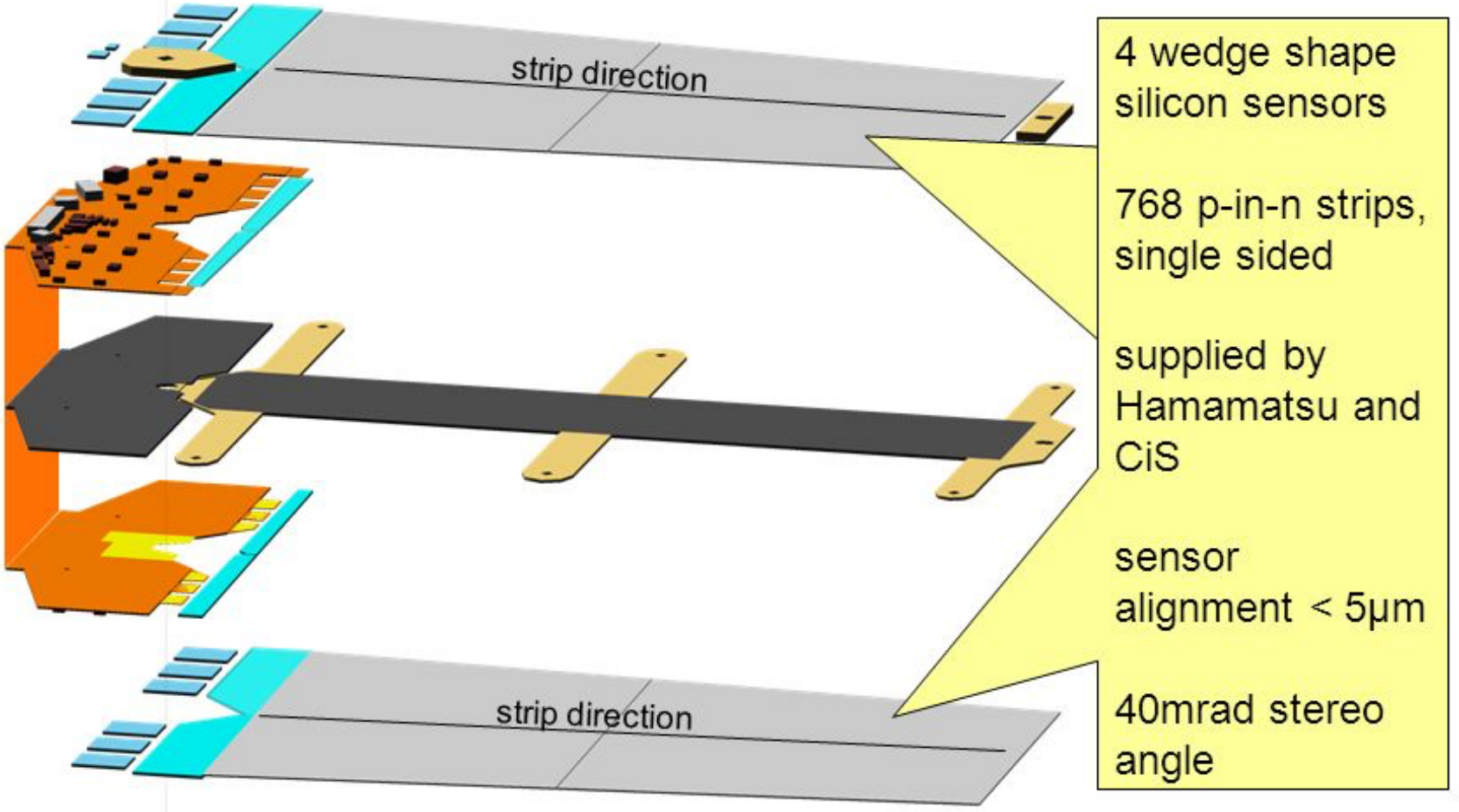


n-side – strips parallel to edge (beam line)
p-side – stereo angle 15 degree

Single Sided Strip Sensors back-to-back (recap lecture 1)

Double Sided Strip Module

ATLAS Endcap Module Design



The Inception of Silicon Pixel Detectors

"The silicon micropattern detector: a dream?"

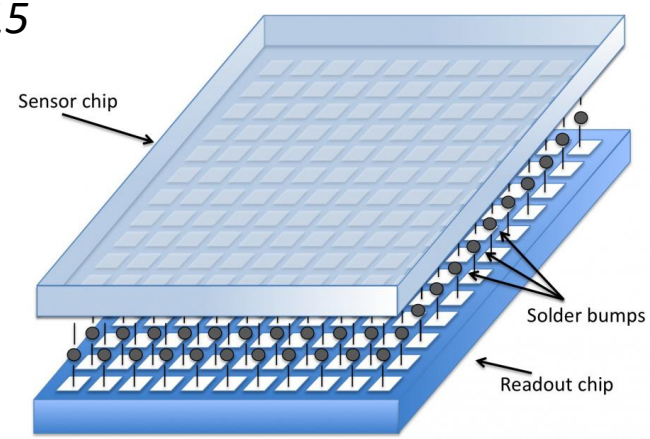
E.H.M Heijine, P. Jarron, A. Olsen and N. Redaelli , *Nucl. Instrum. Meth. A 273 (1988) 615*

"Development of silicon micropattern detectors"

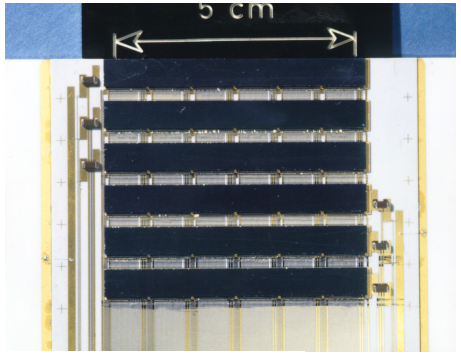
CERN RD19 collaboration, *Nucl. Instrum. Meth. A 348 (1994) 399*

1995 – First Hybrid Pixel detector installed in WA97 (CERN, Omega facility)

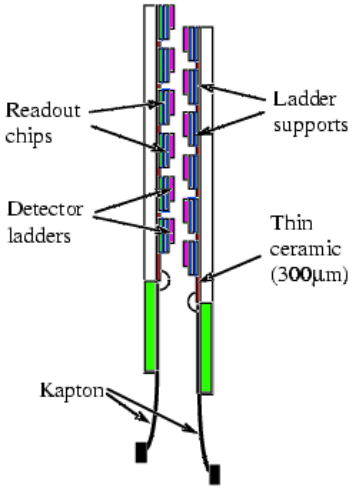
1996/97 – First Collider Hybrid Pixel Detector installed in DELPHI (CERN, LEP)



Hybrid pixel detector



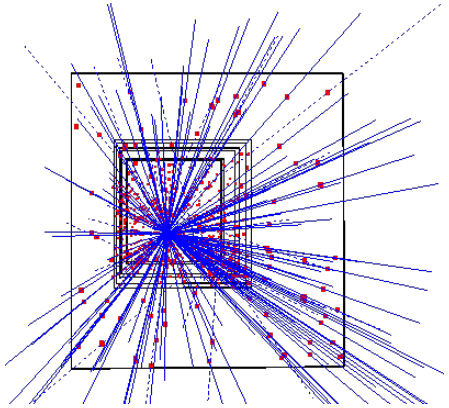
E. Heijne, E. Chesi



Work carried out by RD19 for WA97 and NA57/CERN

CERN – WA97 Experiment (1995)

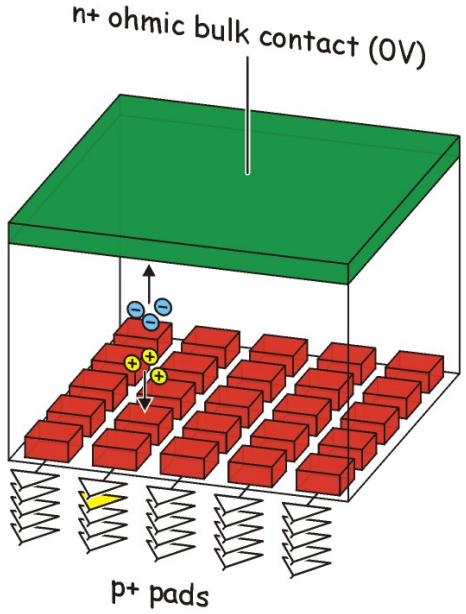
- 5 x 5 cm^2 area
- 7 detector planes
- ~0.5 M pixels
- Pixel size 75 x 500 μm^2
- 1 kHz trigger rate
- Omega2 chip



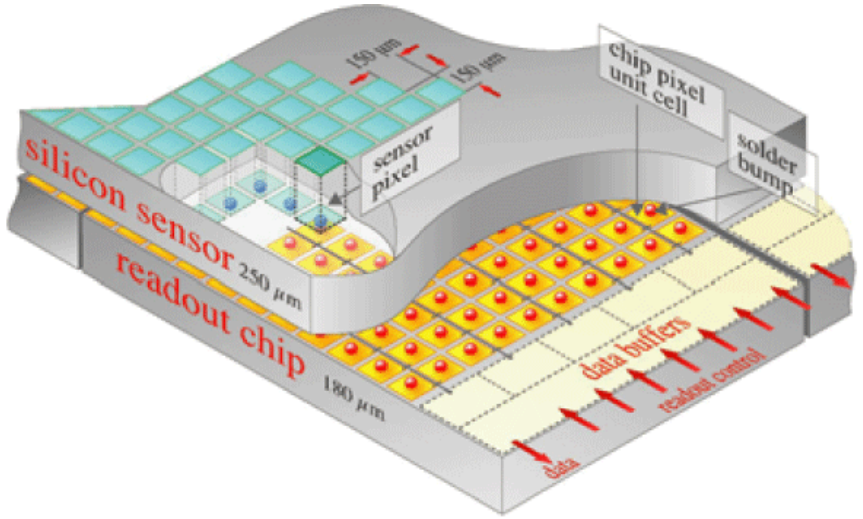
No-field, Pb-Pb, 153 reconstructed tracks

Pixel Chip

Pixel Sensor



Pixel Sensor Bump Bonded to the Readout Chip



Pixel detectors

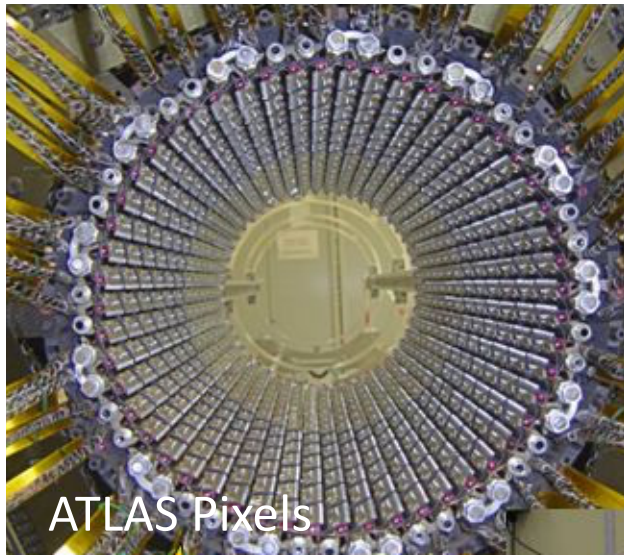
- Truly two-dimensional sensitivity
- No two-hit ambiguity
- Single-sided process

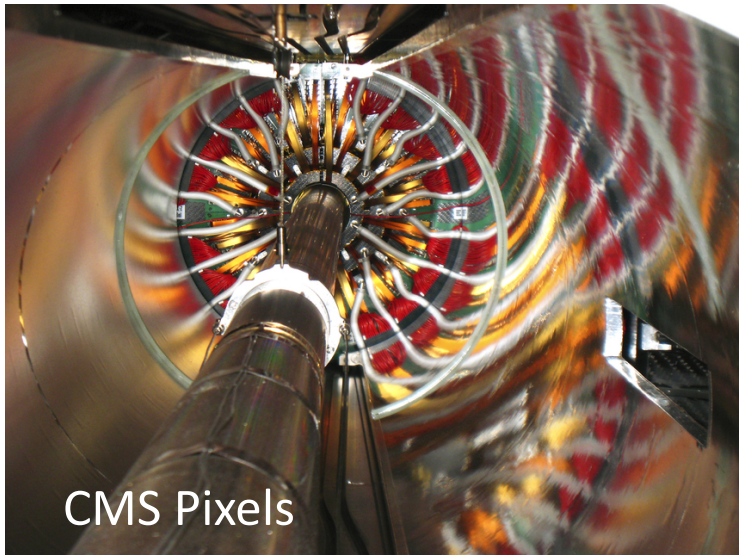
- But nr. Channels N^2
- Minimum pitch limited by bump bonding technology

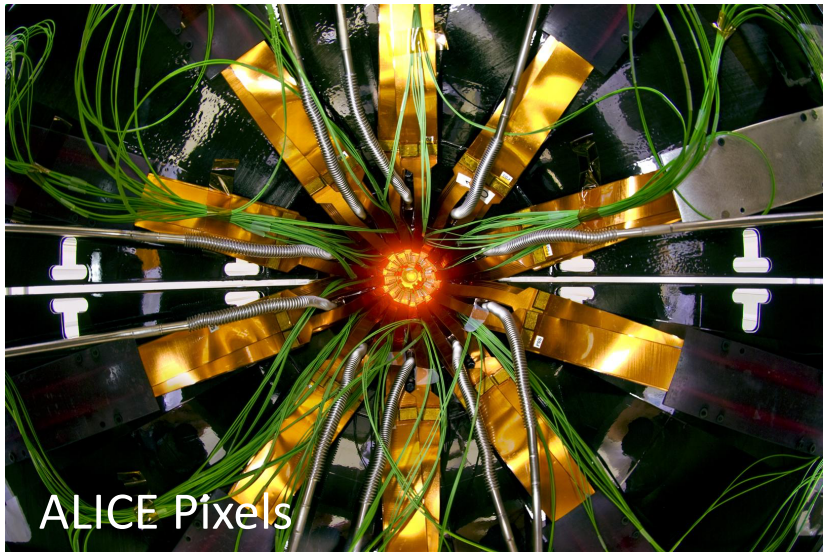
  ⇨ position resolution > 10μm

Pixel Detectors at the LHC

10 years after the first use in WA97… hybrid pixel detectors at the heart of the LHC experiments



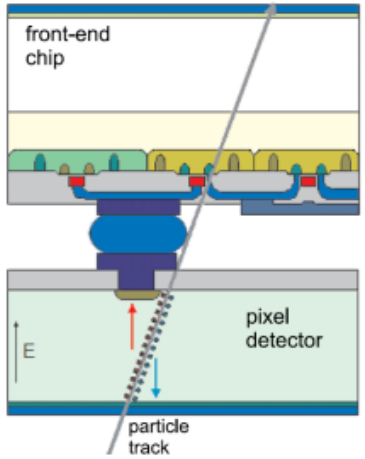




Parameters	ALICE	ATLAS	CMS
Nr. layers	2	3	3
Radial coverage [mm]	**39** - 76	**50** - 120	**44** – 102
Nr of pixels	9.8 M	80 M	66 M
Surface [m^2]	0.21	1.7	1
Cell size ($r\phi$ x z) [μm^2]	50 x 425	50 x 400	100 x 150
Silicon thickness (sens. + ASIC) - x/X_0 [%]	0.21 + 0.16	0.27 + 0.19	0.30 + 0.19

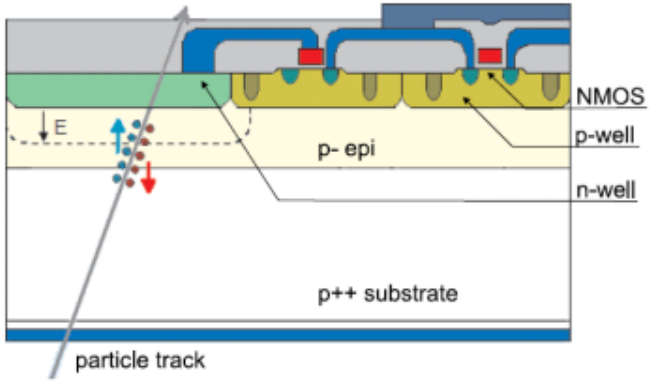
Beyond Hybrid Pixel Detectors …

Hybrid Pixel Detector



N. Wermes (Univ. of Bonn)

Monolithic Pixel Detector



N. Wermes (Univ. of Bonn)

Since the very beginning of pixel development (CERN RD 19):

dream to integrate sensor and readout electronics in one chip

Motivation to reduce: cost, power, material budget, assembly and integration complexity

Several major obstacles to overcome:

- CMOS generally not available on high resistivity silicon (needed as bulk material for the sensor)
- Full CMOS circuitry not possible within the pixel area (only one type of transistor ➔ slow readout)

MAPS exist in many different flavors: **CMOS**, HV CMOS, DEPFET, SOI

The following will cover only CMOS Active Pixel Sensors (CMOS MAPS) = **CMOS Active Pixel Sensors (CMOS APS)**

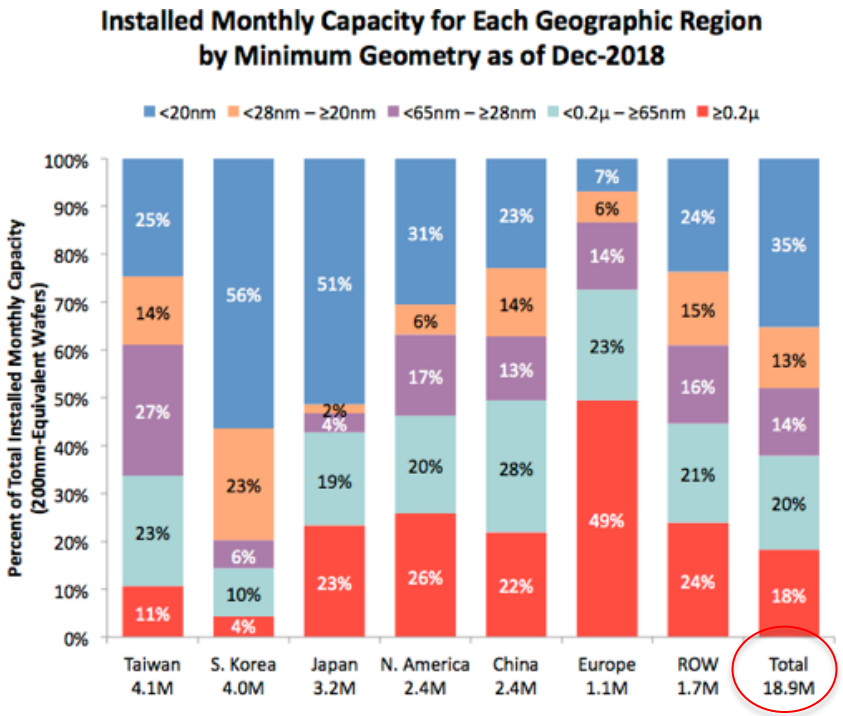
Silicon Properties
A Brief Reminder

Silicon CMOS Industry

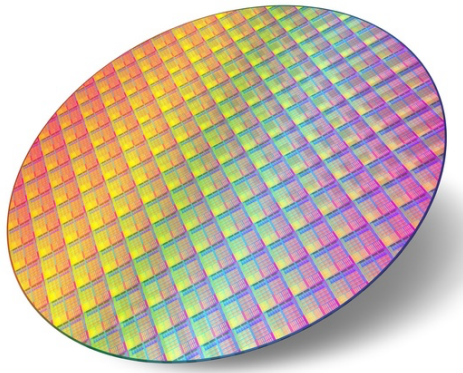
Monocrystalline silicon

main semiconductor used for the fabrication of Integrated Circuits

Monocrystalline, high purity single crystals (Czochralski)



CMOS sub-micron fabs



~3.5$ / cm^2

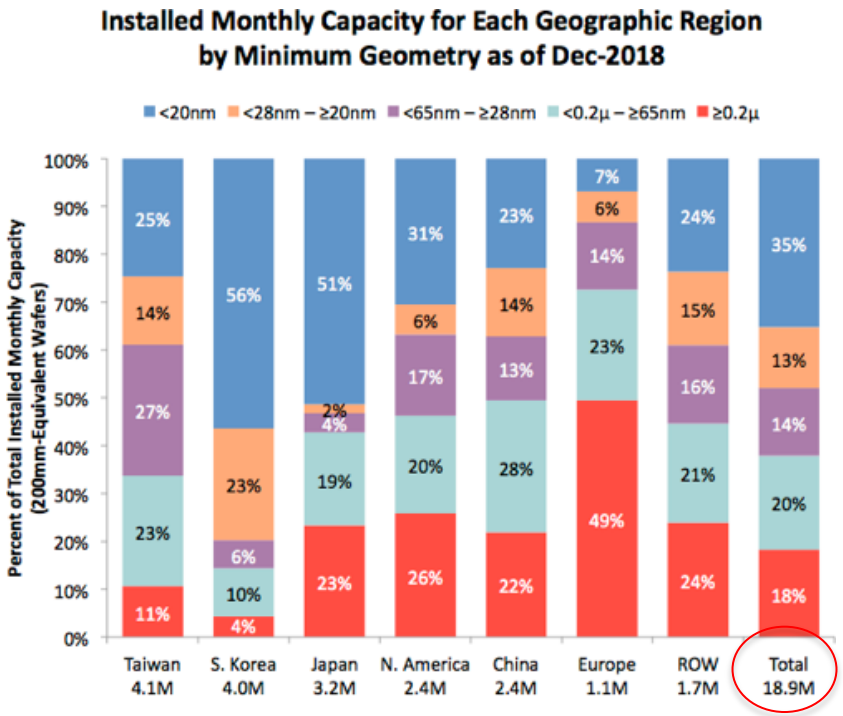
220 Million wafers / year → ~ 14 x 10^6 m^2

Silicon CMOS Industry

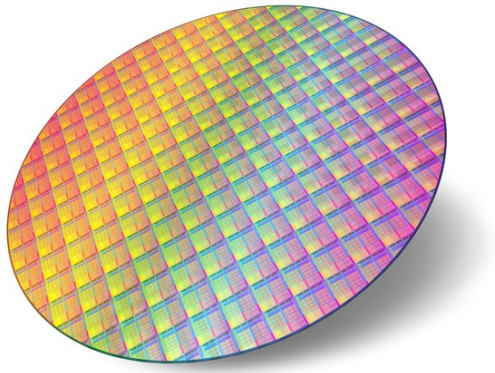
Monocrystalline silicon

main semiconductor used for the fabrication of Integrated Circuits

Monocrystalline, high purity single crystals (Czochralski)



CMOS sub-micron fabs



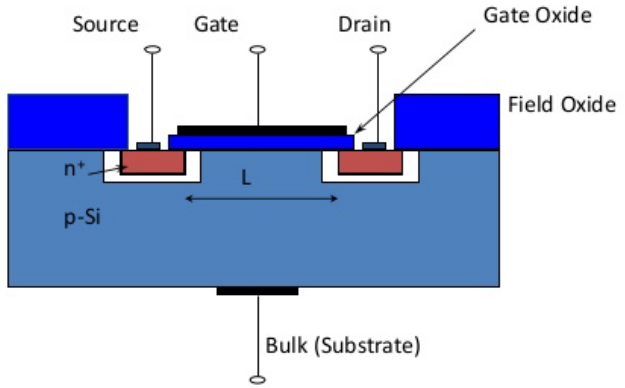
~3.5$ / cm^2

220 Million wafers / year

~ 14 x 10^6 m^2

Metal Oxide Semiconductor Field Effect Transistor

MOSFET Structure



Technology Node

Transisotor meanimum feature size

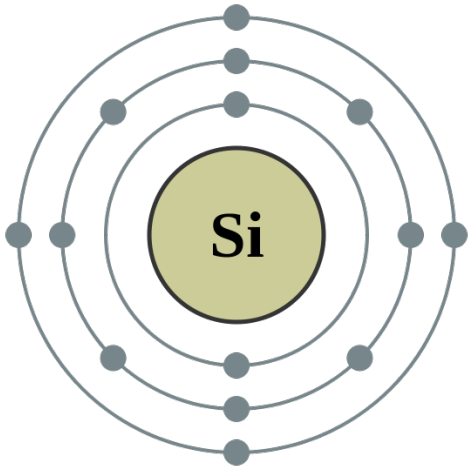
Example

For a "28nm CMOS process"

28nm is the channel length of a minimum-size transistor

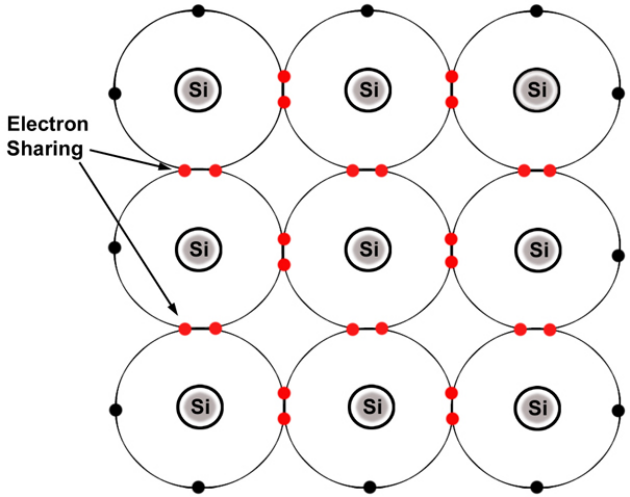
Silicon Properties – Lattice Structure

Silicon Atom (Si)



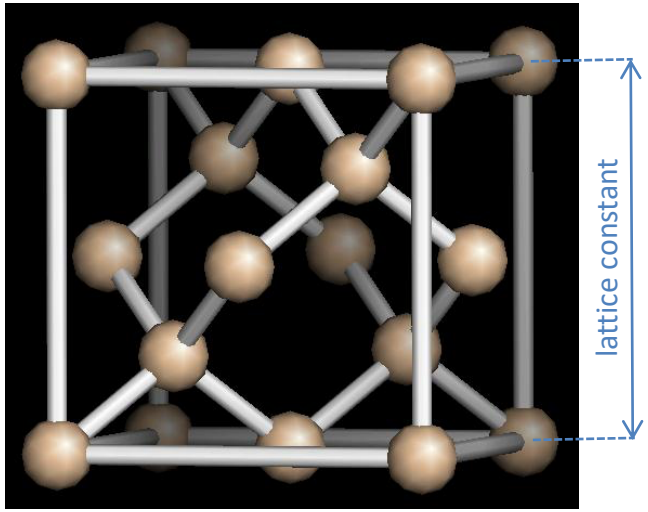
- Z = 14 (2,8,4)
- Group IV
- 4 valence electrons

2D representation of Si crystal



Shared electrons of a covalent bond

Silicon lattice – diamond crystal structure



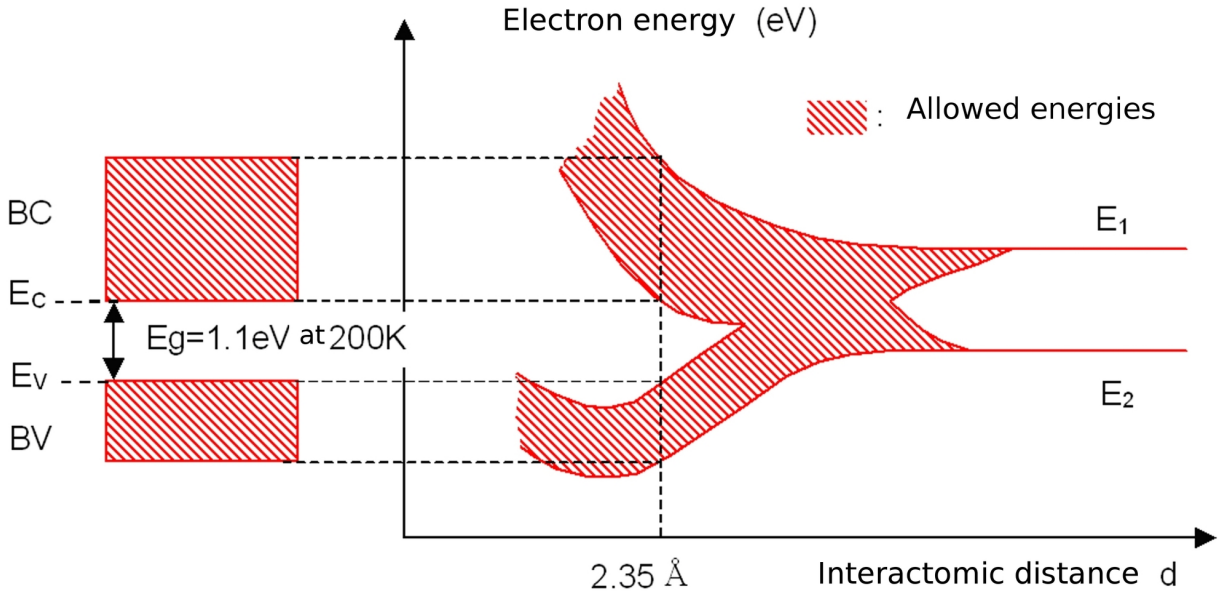
Crystal structure

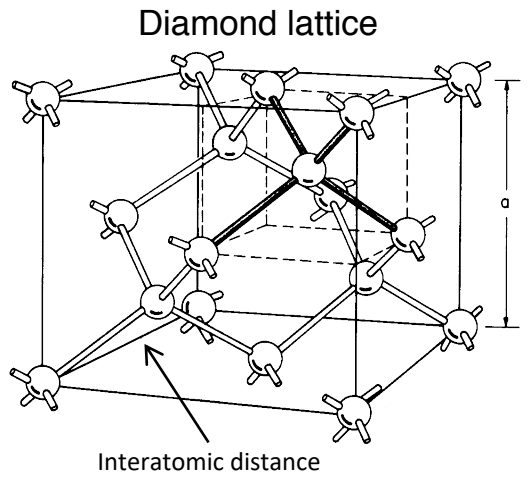
- diamond cubic (tetrahedral)
- lattice constant 5.43 A

Each atom is surrounded by 4 equidistant nearest neighbors

Silicon Properties – Lattice Structure

For a single atom the electrons can only occupy certain energy levels





When N atoms are moved closer, until they reach the equilibrium inter-atomic distance d, the energy levels split into N levels (N-fold degenerate) very close to each other. If N is large (which is the case in a crystal) they eventually form a continuous energy band.

In a crystal the discrete atomic levels form energy bands

Material Basic Properties

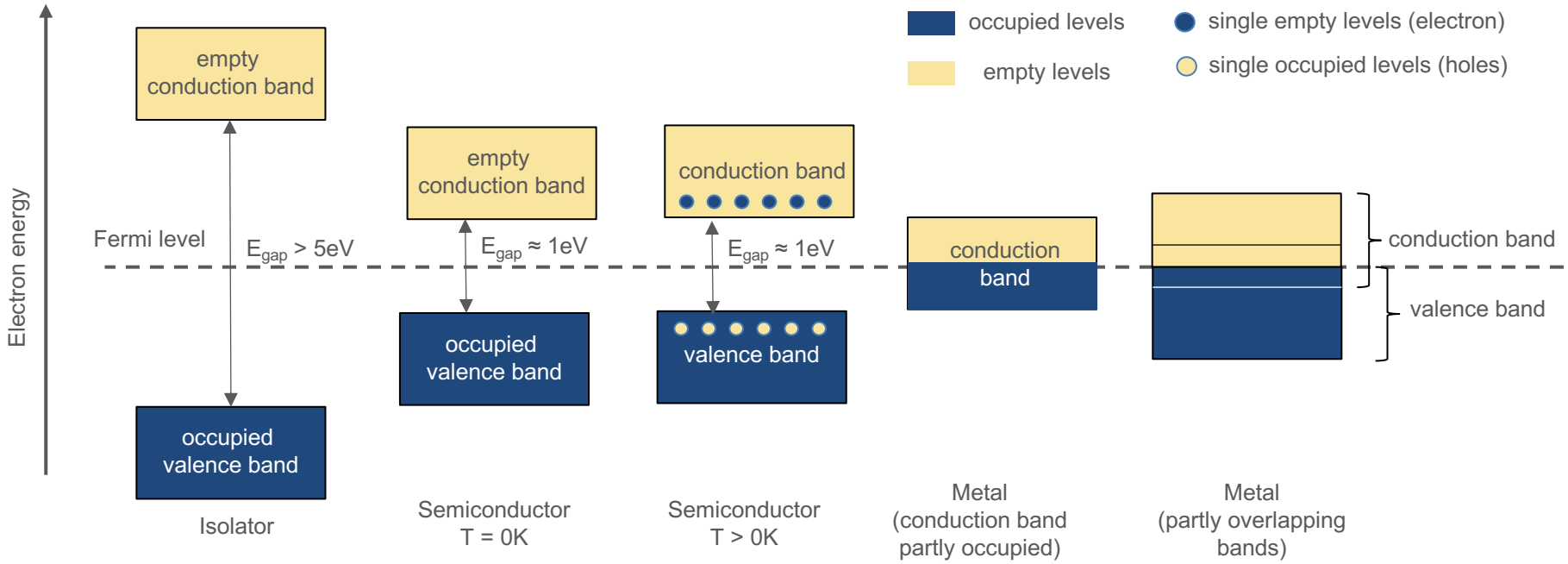
Solid state materials

classification

isolators (large band gap)

semiconductors (small band gap)

metals (conduction band partially filled or overlaps with valance band)

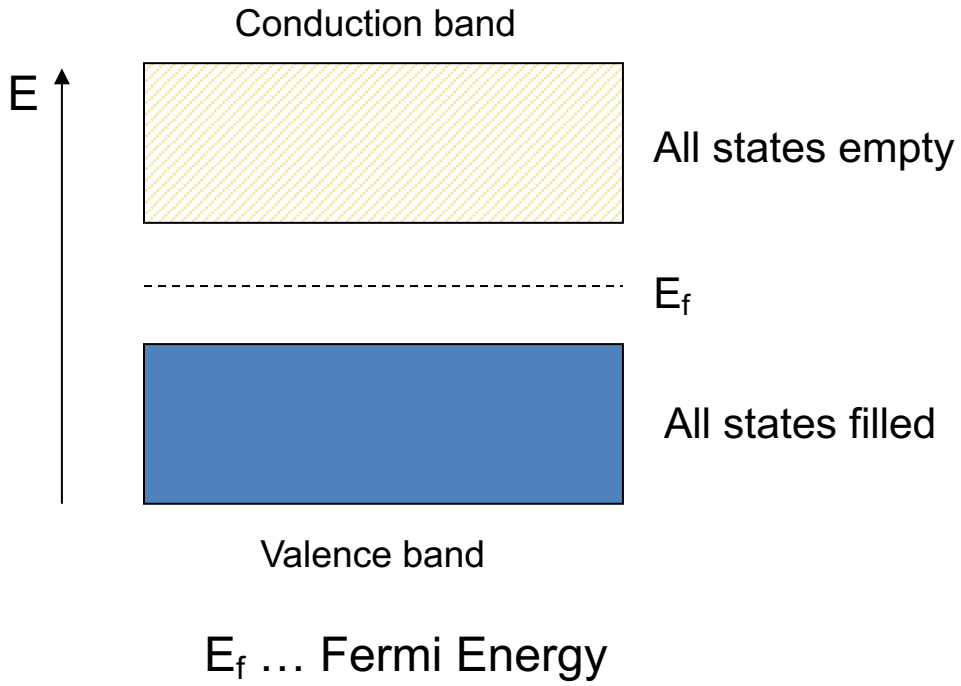


Band gap at 300K: **Si = 1.12eV**, Ge = 0.67eV, GaAs = 1.42eV, Diamond = 5.5eV Band gap Si at 0K: 1.17eV

Note: in reality the band structure is more complex, depending on crystal momentum, crystal orientation, etc.

Semiconductor Basic Properties

At absolute zero (-273.15° C)



E_f … Fermi Energy

If an electrical field is applied to the crystal no current can flow as this would require an electron to acquire energy. This is not possible because no higher energy states in the valence band are available.

At higher temperatures

Electrons can gain energy due to thermal excitation

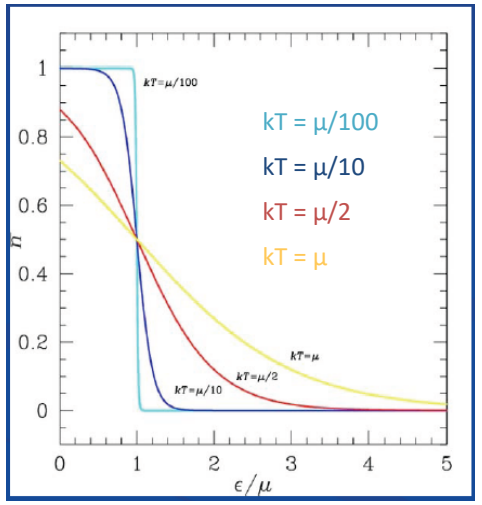
Probability that an electronic state is occupied by an electron follows the Fermi-Dirac statistics

$$F(E) = \frac{1}{1 + e^{(E-E_F)/kT}}$$

k ... Boltzmann constant

E_F is the energy at which the probability of occupation is 1/2.

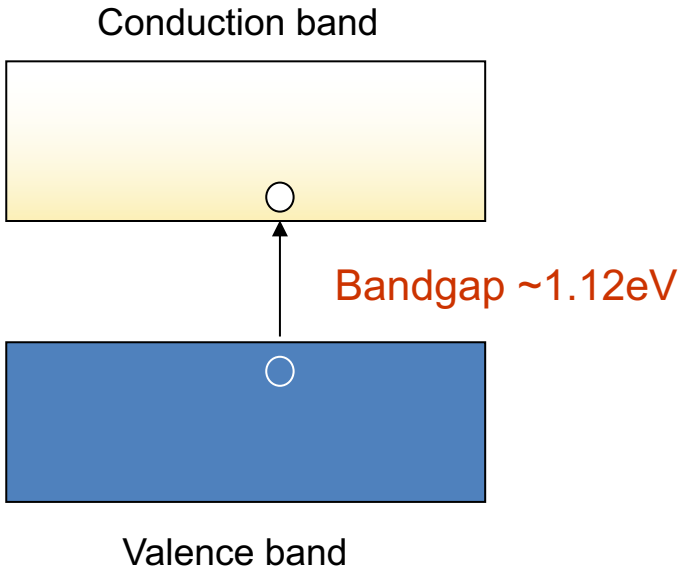
$\varepsilon = E$, $\mu = E_f$,



Fermi-Dirac distribution. States with energy ε below the Fermi energy (μ) have higher probability n to be occupied, and those above are less likely to be occupied.

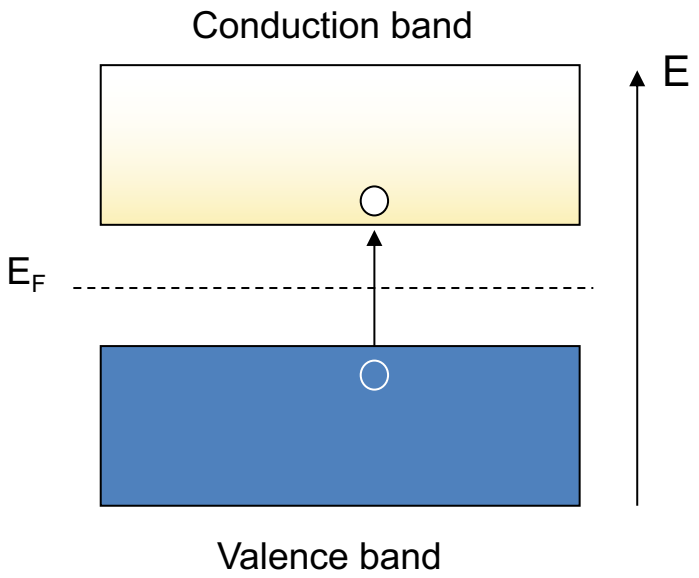
Silicon Basic Properties

How much energy is required to generate an electron-hole pair in silicon?



Due to phonon scattering the average energy required to generate an electron-hole pair is 3.62 eV at room temperature.

Electrons and holes

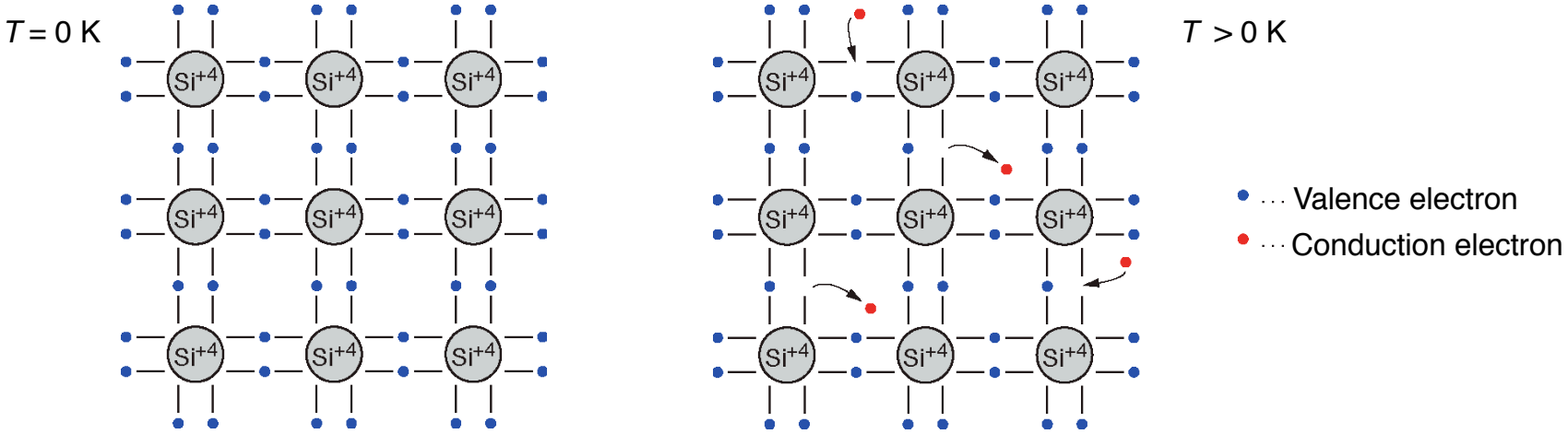


An electron moving to a state in the conduction band leaves an unoccupied state in the valence band = hole

Silicon Basic Properties

The creation of an electron-hole pair can also be seen in respect with chemical bonding: an electron is broken free from the covalent bond between two Si-atoms

Example of column IV elemental semiconductor



- Each atom has 4 closest neighbors, the 4 electron in the outer shell are shared and form covalent bonds
- At low temperature all electrons are bound (no conductivity)
- At higher temperature thermal vibrations of the reticle break some of the bonds ⇨ free e^- cause conductivity (electron conduction)
- The remaining open bonds attract other e^- creating a vacancy (hole) ⇨ The holes change position creating conductivity (hole conduction)

Silicon Basic Properties

Intrinsic semiconductor: contains only small amounts of impurities compared to the thermally generated electrons and holes

$n_e = n_h = n_i$ n_i = intrinsic carrier density

$$E_F = E_i = \frac{E_C + E_V}{2} + \frac{kT}{2}\ln\left(\frac{N_V}{N_C}\right)$$

E_F lies very close to the mid band gap at RT

N_V, N_C := effective densities of states in the valence band and conduction band

- Due to the small band gap electrons already occupy the conduction band at room temperature
- Electrons from the conduction band may recombine with holes
- A thermal equilibrium is reached between excitation and recombination: charge carrier concentration $n_e = n_h = n_i$

$$n_i = \sqrt{N_c N_v}\cdot e^{\left(-\frac{E_G}{2kT}\right)} \propto T^{\frac{3}{2}}\cdot\exp\left(-\frac{E_g}{2kT}\right)$$

N_V, N_C: effective densities of states in the valence band and conduction band

At RT: N_V=1.04x10^{19} cm^{-3}, N_C=2.8x10^{19} cm^{-3}

⇨ n_i (Si at RT) = 1.45 x 10^{10} cm^{-3}

Compared to ≈ 1 x 10^{22} cm^{-3} atoms in a silicon crystal

only every ≈ 10^{12}th atom is ionized at RT

Silicon Properties – Drift Velocity and Mobility

Free charge carriers can be seen as free particles - they are not associated with a lattice site

- Mean kinetic energy: 3/2 kT
- Mean velocity at RT: ~ 10^{11} µm/s

The charge carriers scatter on **lattice imperfections** due to thermal vibrations, **impurity atoms** and **lattice defects**

If no electric field is applied, the average displacement due to random motion is zero

Applying an electric field **E**:

Charge carriers will be accelerated in between random collisions in the direction determined by the electric field.

Average drift velocity (*):

$$v_e = -\mu_e E$$

μ_e electron mobility

$$\mu_e = \frac{e\tau_e}{m_e}$$

$$v_h = -\mu_h E$$

μ_h hole mobility

$$\mu_h = \frac{e\tau_h}{m_h}$$

m_e, m_h … effective mass

τ_e, τ_h: mean free time between collisions for e and h

(*) Holds for small fields E ("acceleration" is small compared to the thermal velocity).
If the electric field is high enough so that the carrier energies are larger than the thermal energies, the drift velocities become independent of the electric field.

Silicon Properties – Carrier Mobility

In the linear region of v(E) the charge carrier mobilities are

μ_e=1350 cm^2/Vs μ_h=480 cm^2/Vs

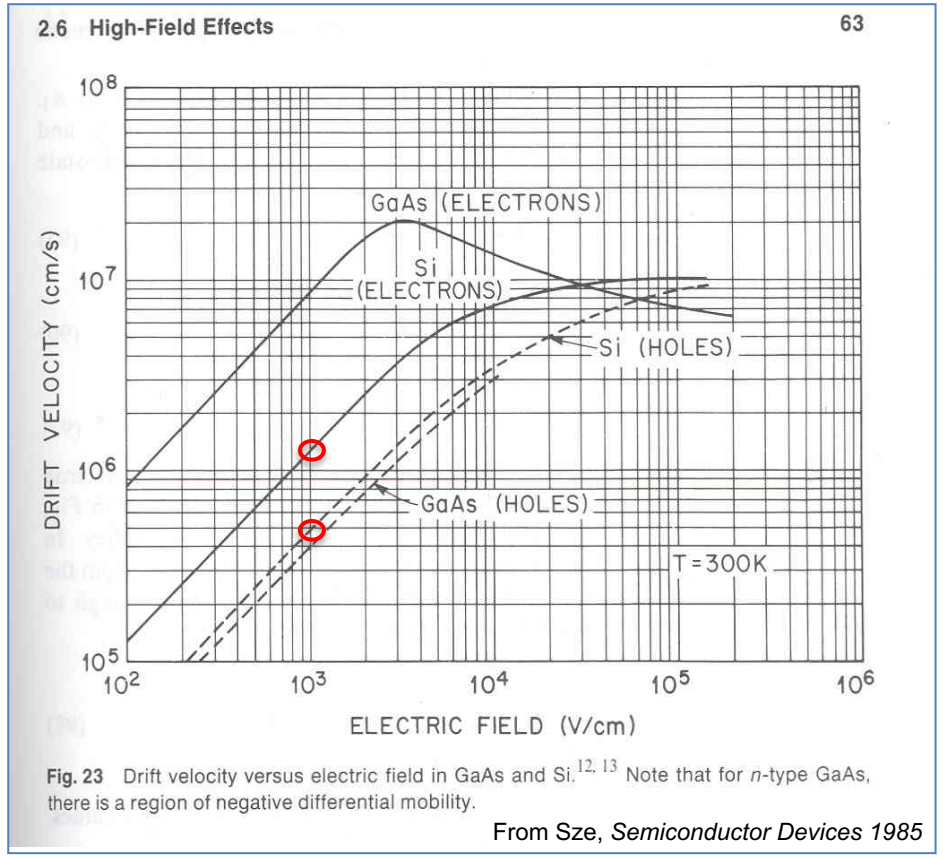
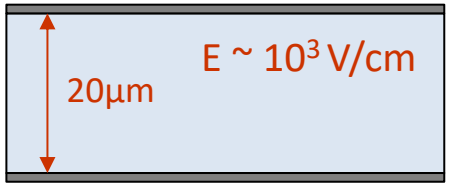


Fig. 23 Drift velocity versus electric field in GaAs and Si.[12, 13] Note that for *n*-type GaAs, there is a region of negative differential mobility.

From Sze, *Semiconductor Devices 1985*

2V is applied over 20µm



v_e ~ 10^{10} µm/s

v_h ~ 0.3 x 10^{10} µm/s

Charge collection time (e)

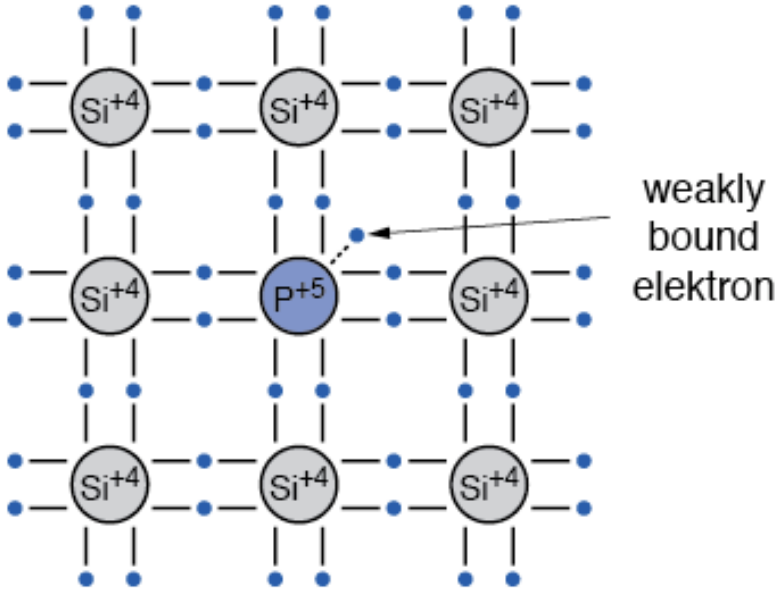
T_e ~ 2ns

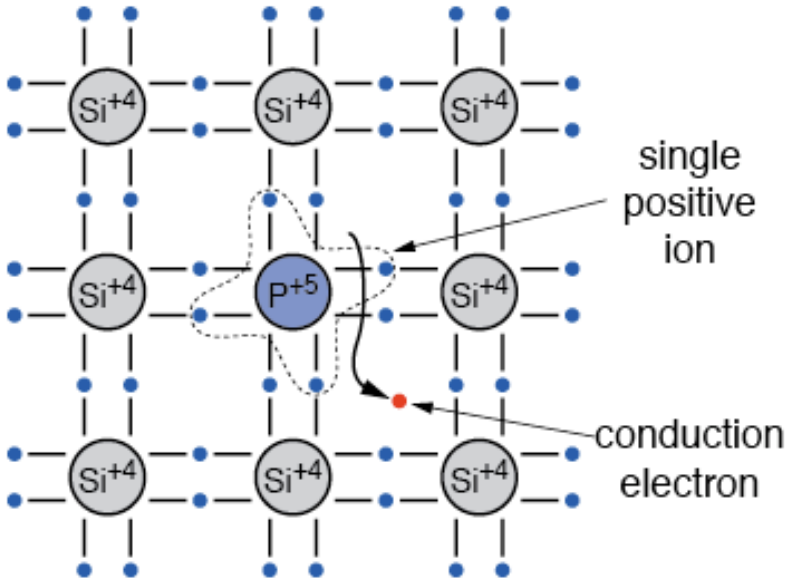
Adding Impurities to Intrinsic Silicon – n-doping

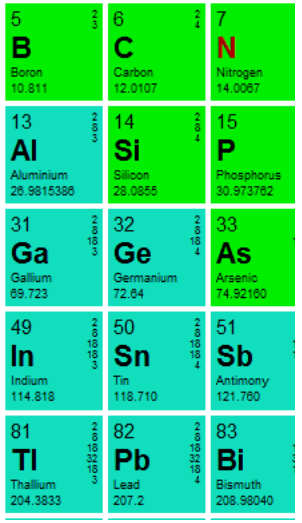
Silicon n-type

Doping with an element of the V group (e.g. P, As, Sb). The 5th valence electron is weakly bound

- The doping atom is called donor
- The released electron can contribute to electrical conduction and leaves a positively charged ion

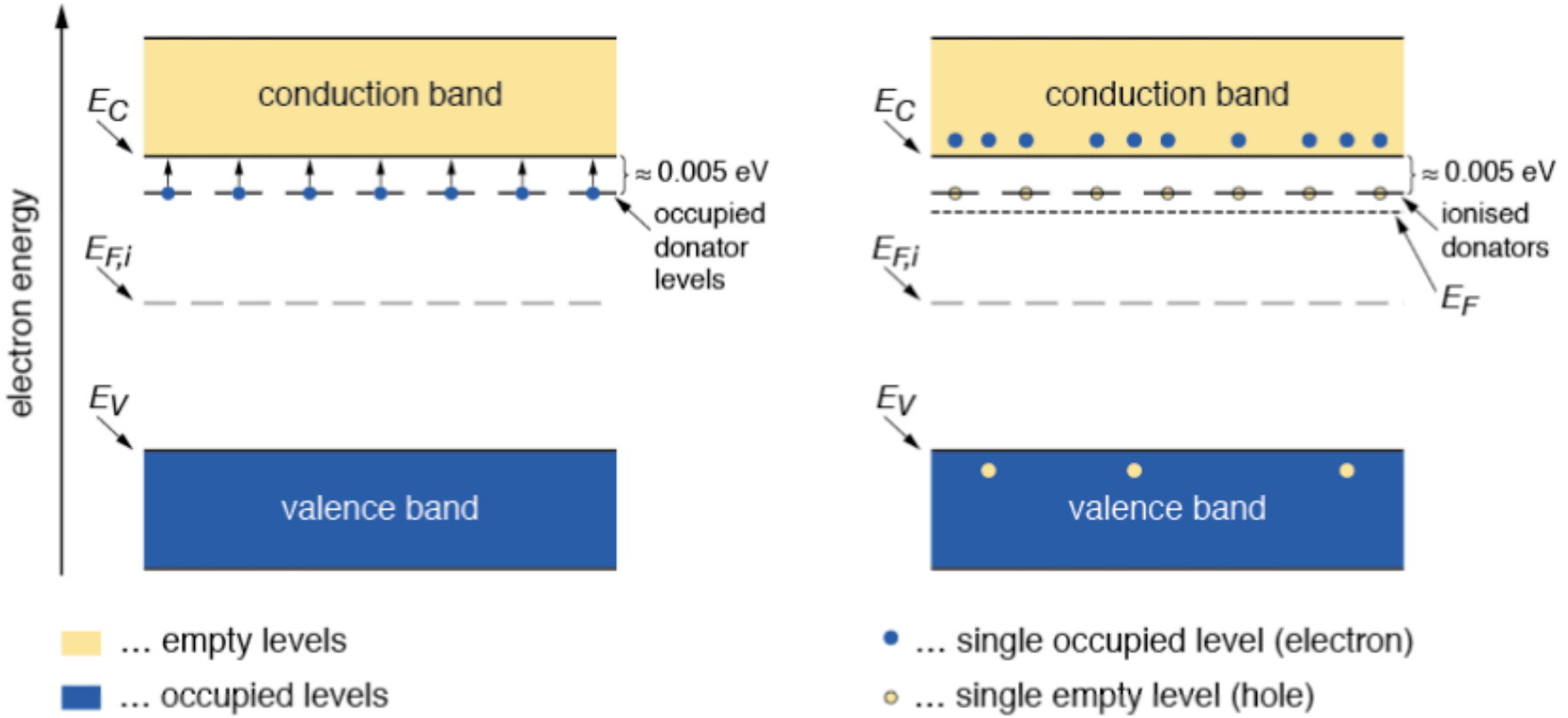






Adding Impurities to Intrinsic Silicon – Band Model n-doping

- The energy level of the donor is just below the edge of the conduction band
- At RT most electrons are raised to the conduction band
- The Fermi level E_F moves up

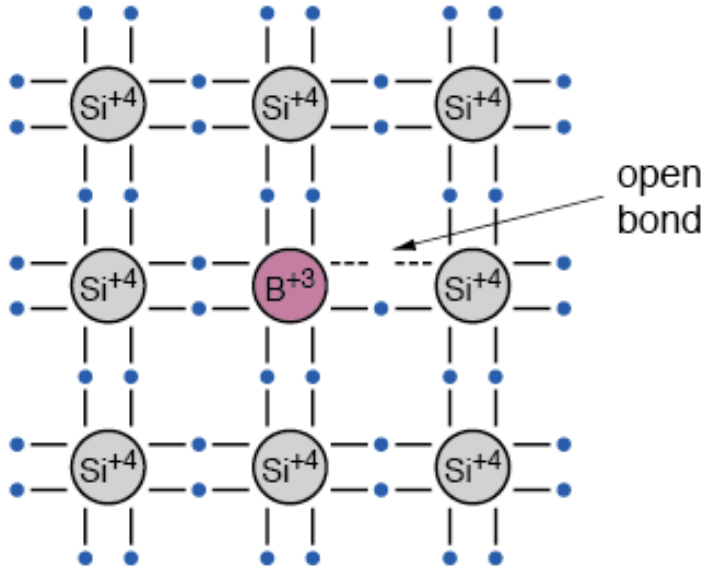


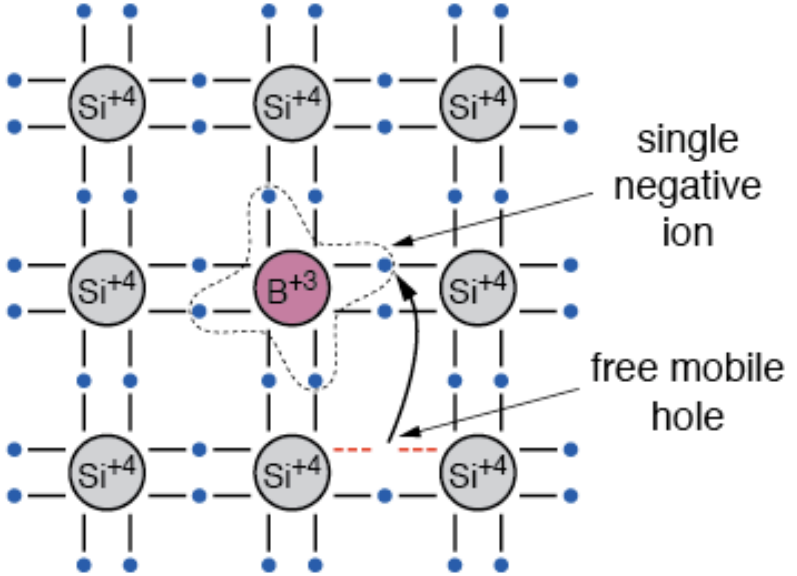
Adding Impurities to Intrinsic Silicon – p-doping

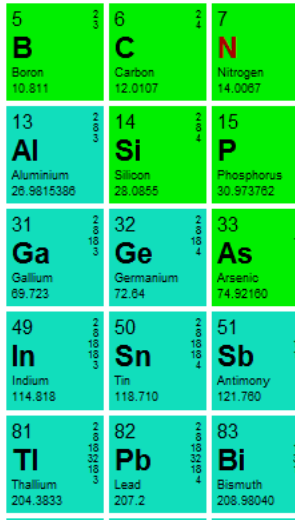
Silicon p-type

Doping with an element of the group III (e.g. B, Al, Ga, In). One valence bond remains open. This open bond attracts electrons from their neighbor atoms

- The doping atom is called acceptor
- The acceptor atom in the lattice is negatively charged. The hole acts as a free mobile charge

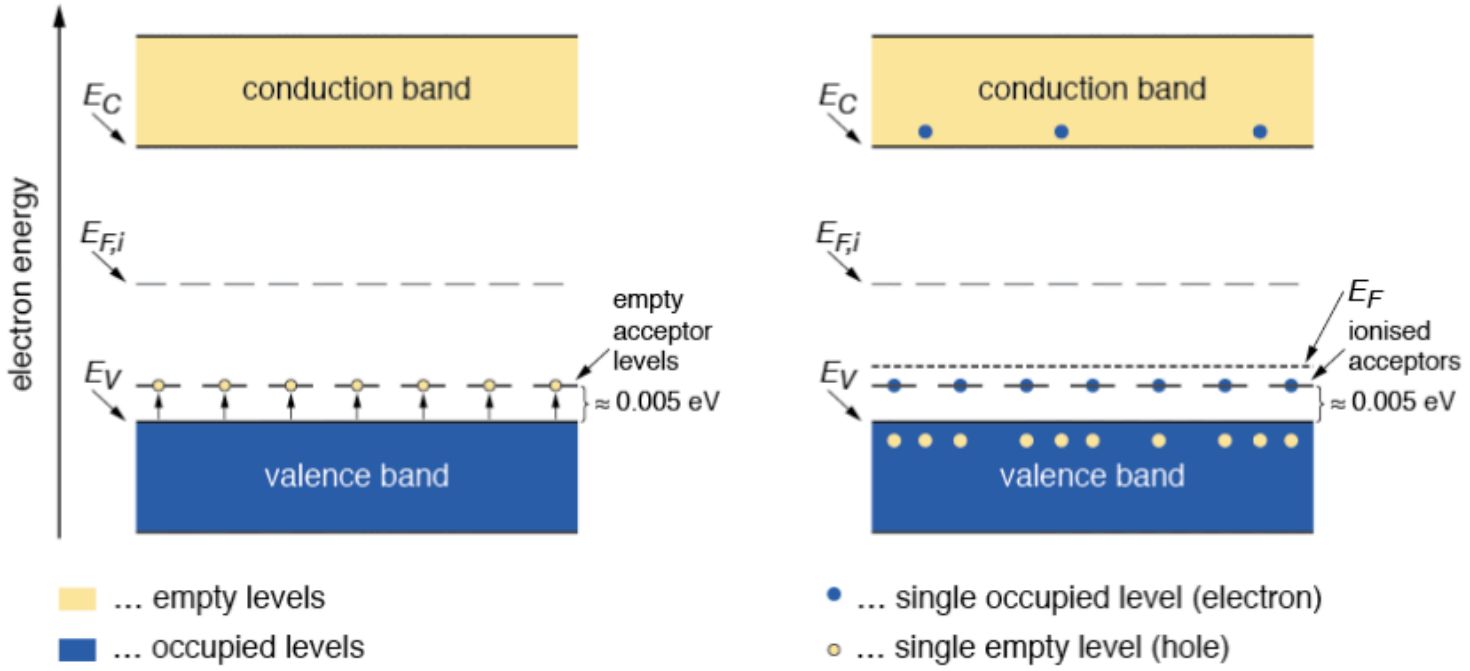






Adding Impurities to Intrinsic Silicon – Band Model p-doping

- The energy level of the acceptor is just above the edge of the valence band
- At RT most levels are occupied be electrons leaving holes in the valence band
- The Fermi level E_F moves down



Silicon Properties – Resistivity

Depends on concentration of free charge carriers and their mobility

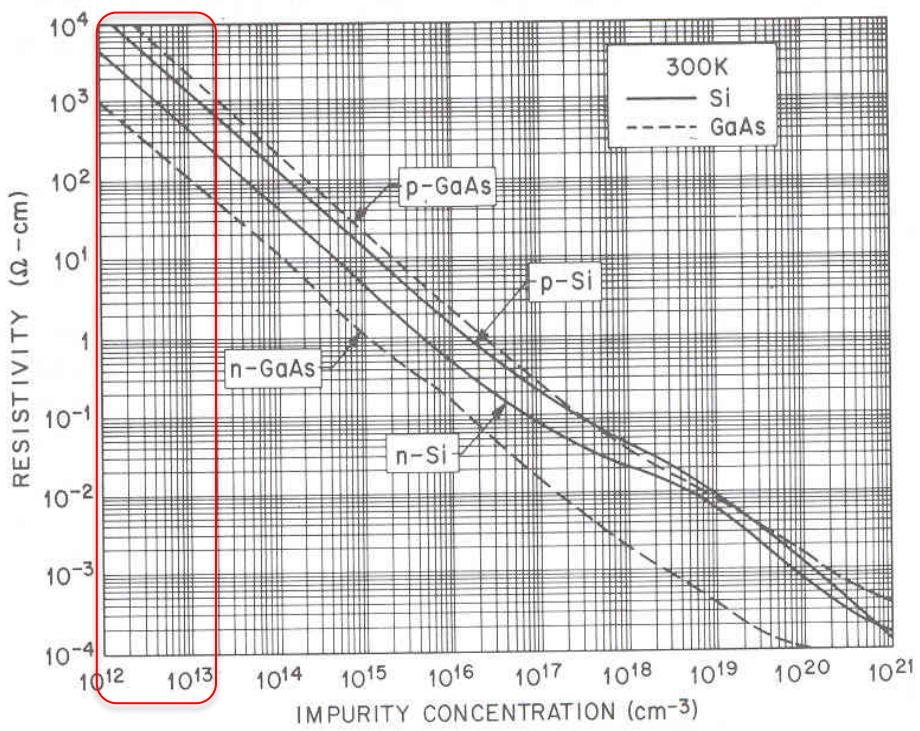


Fig. 7 Resistivity versus impurity concentration[4] for Si and GaAs.

From Sze, *Semiconductor Devices 1985*

$$\rho = \frac{1}{q(\mu_e n + \mu_h p)}$$

⇨ resistivity of intrinsic silicon ~ 235 kΩ cm

⇨ a silicon for pixel detectors ~ 1-10 kΩ cm

⇨ silicon substrate for CMOS IC ~ 0.1 – 10 Ωcm

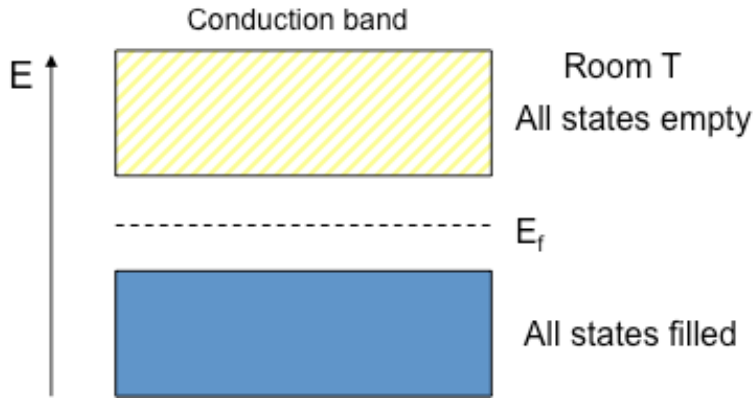
Semiconductor Detectors
Basic Principles

The Ideal Semiconductor Detector

One of the most important parameters of a detector is the signal to noise ratio (SNR)

A good detector should have a large SNR. However, this leads to two contradictory requirements:

- Large Signal
  ⇨ Low ionization energy ⇨ small band gap
- Low noise
  ⇨ very few intrinsic charge carriers ⇨ large band gap



An optimal material should have $E_g \approx 6eV$

In this case the conduction band is almost empty at room temperature and the band gap is small enough to create a large number of e^-h^+ pairs by ionization.

A material with such characteristic is the diamond. However even artificial diamond (e.g. CVD diamonds) are too expensive for large area detectors.

Diamond band gap ≈ 5.5eV (RT)
Intrinsic charge carrier density
$n_i \approx 10^{-27}$ cm^{-3} (T=300K)

Intrinsic Silicon – A Very Poor Detector

How does Silicon perform as detection medium?

- Mean ionization energy $I_0 = 3.62\ eV$
- Mean energy loss for a MIP in intrinsic silicon at $T = 300\ K$: $dE/dx = 3.87\ MeV/cm$
- $n_i = 1.45 \times 10^{10}\ cm^{-3}$

Assuming a detector with a thickness of 300 μm

⇨ Signal of a MIP in such a detector

$$\frac{dE/dx \cdot d}{I_0} = \frac{3.87 \cdot 10^6\ eV/cm \cdot 0.03cm}{3.62eV} \approx 3.2 \cdot 10^4\ e^- h^+$$

Assuming a detector with a surface A = 1 cm^{-2}

⇨ Intrinsic charge carrier density (T = 300 K)

$$n_i \cdot d \cdot A = 1.45 \cdot 10^{10}\ cm^{-3} \times 0.03cm \times 1cm^{-2} \approx 4.35 \cdot 10^8\ e^- h^+$$

Number of $e^- h^+$ pair generated by ionization (signal) is four orders of magnitude smaller than the number of electrons generated thermally (noise) at room temeperature!!!

How to suppress the charge carriers? ⇨ Depleted zone in reverse biased pn junctions

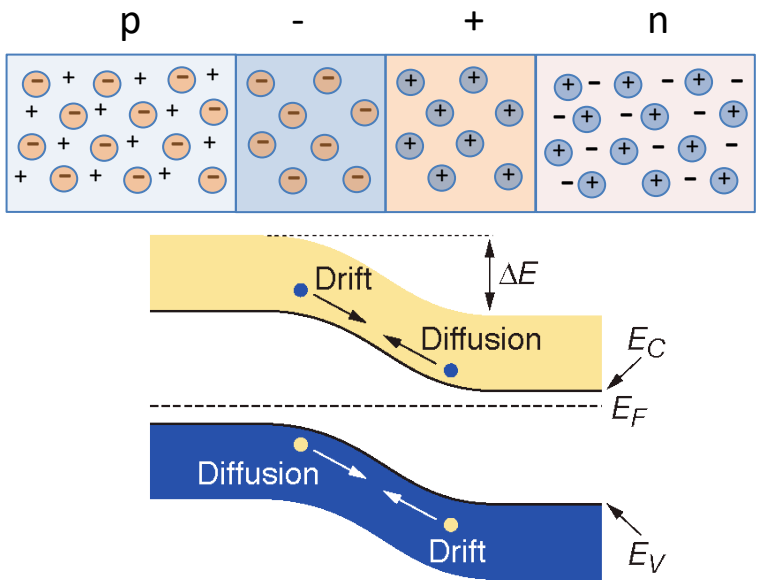
How to Build a Detector – The p-n Junction

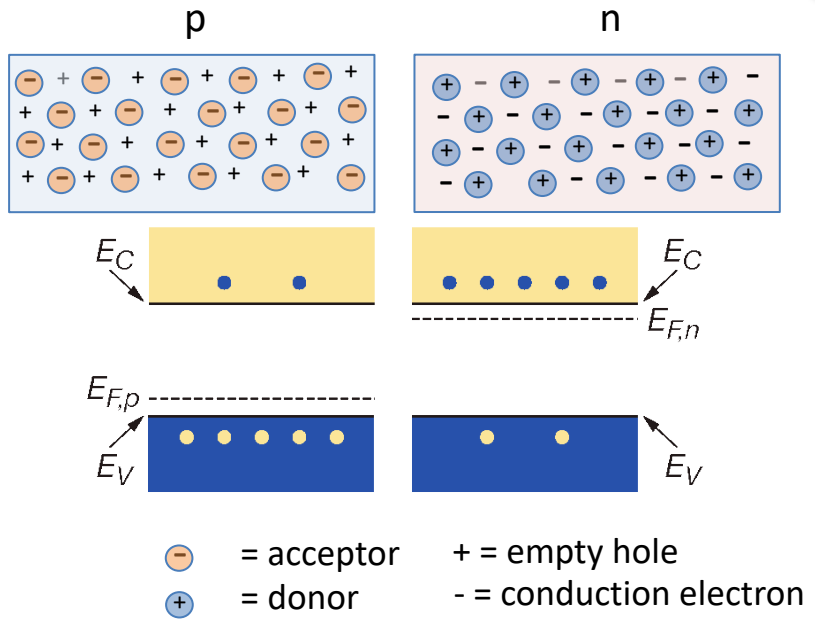
Charge carrier diffusion

At the interface of an n-type and p-type semiconductor the difference in the Fermi levels (carriers concentration) cause diffusion of the majority carriers to the other type until thermal equilibrium is reached. The Fermi levels are equal.

Opposite carriers recombine

Space charges remain in the junction region





Generate an electric field, which counteract the diffusion

Depleted region, the stable charge region free of charge carriers

The corresponding potential is called built-in-voltage V_{bi}

$$V_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2}$$

kT ~ 26 mV (at RT)

A More Realistic Detector – The p⁺n Reversed Biased Junction

Build a more Realistic Detector

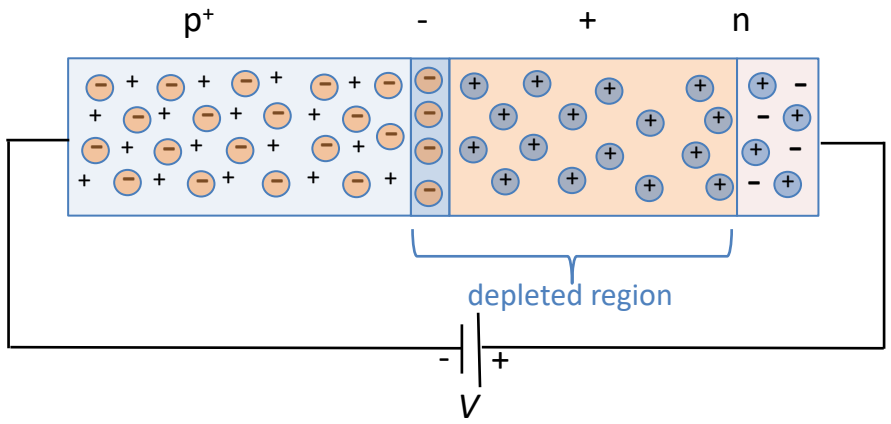
Thin highly doped (**p⁺**) and **n-well** doped bulk, and apply an external voltage to deplete the bulk volume of free charge carriers

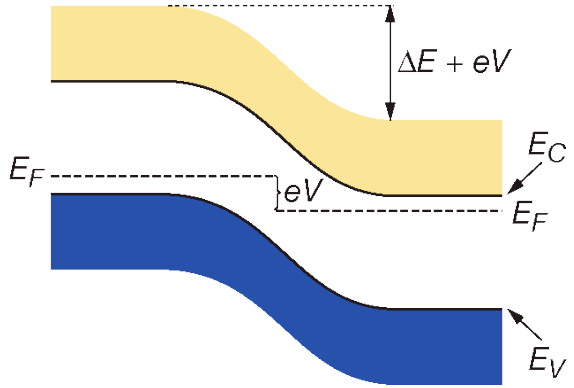
Applying a negative potential difference V between the side p and the side n (reverse bias voltage) the depleted region becomes larger

The potential barrier becomes higher by ***eV*** and diffusion across the junction is suppressed.

The current across the junction is very small ("leakage current")

p⁺n junction scheme





Depletion width W

$$W = \sqrt{\frac{2\varepsilon_s (V_{ext} - V_{bi})}{qN_D}}$$

ε_s = product of rel. permittivity of silicon and of vacuum

This is a reverse biased junction (diode)

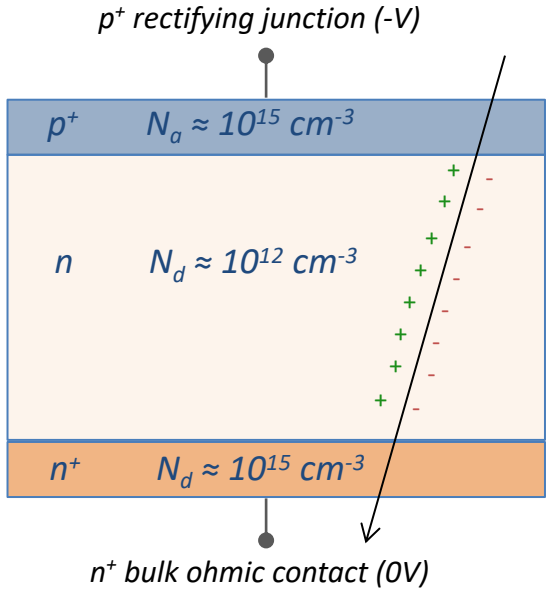
A More Realistic Detector – The p⁺n Reversed Biased Junction

p⁺n diode detector

- Reverse bias (positive voltage on n-bulk wrt p⁺ side)
- Increase reverse voltage to fully deplete the entire bulk of free charge carriers

⇨ **Full volume is sensitive to a passing particle (ionization chamber)**

- Highly n-doped layer to provide ohmic contact (n⁺)



Effective doping concentrations

- $N_a = 10^{15}$ cm^{-3} in p⁺ region
- $N_d = 10^{12}$ cm^{-3} in n bulk

Without applying any external voltage

- W_p = 20 nm, W_n = 23 μm

Applying an external voltage of 100V

- W_p = 400 nm, W_n = 363 μm

Voltage at which full thickness of the diode is depleted

$$V_{fd} = \frac{e}{2\varepsilon_s}(N_D - N_A)d^2$$

d ..thickness

N_D-N_A=N_{eff}…effective doping concentration

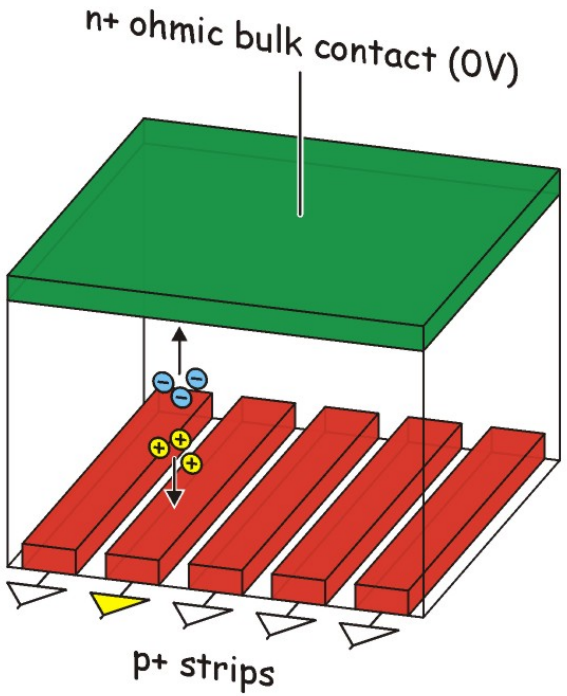
e.g. $N_D = 10^{12}$/cm^3 , $N_a = 10^{15}$/cm^3, d = 300μm

(ε_s = 11.7 x 8.8 x 10^{-12} F/m)

V_{fd} ~ 80 V

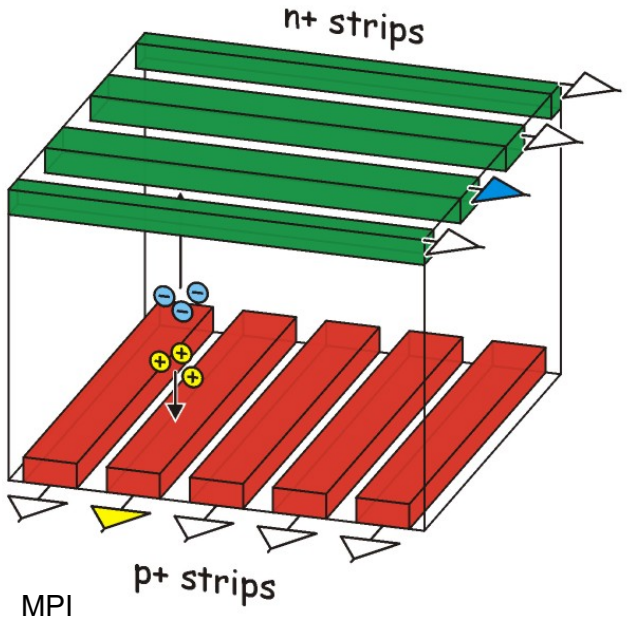
Silicon Strips and Pixels (recap lecture 1)

Single sided strip detector



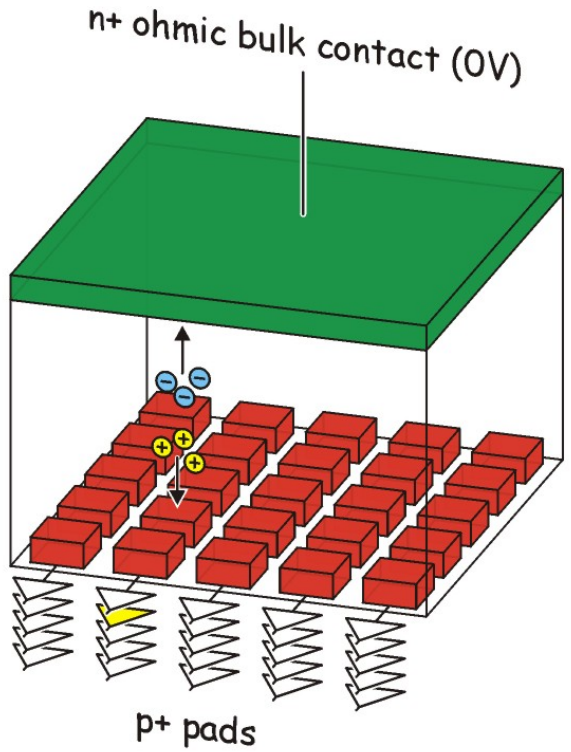
MPI

Double sided strip detector



MPI

Pixel Detector



MPI

CMOS Active Pixel Sensors

Advent and basic Principles

Digital Imaging Revolution

Digital imaging began with the invention of the Charge-Coupled Device (CCD) in 1969

Start of the the digital imaging revolution

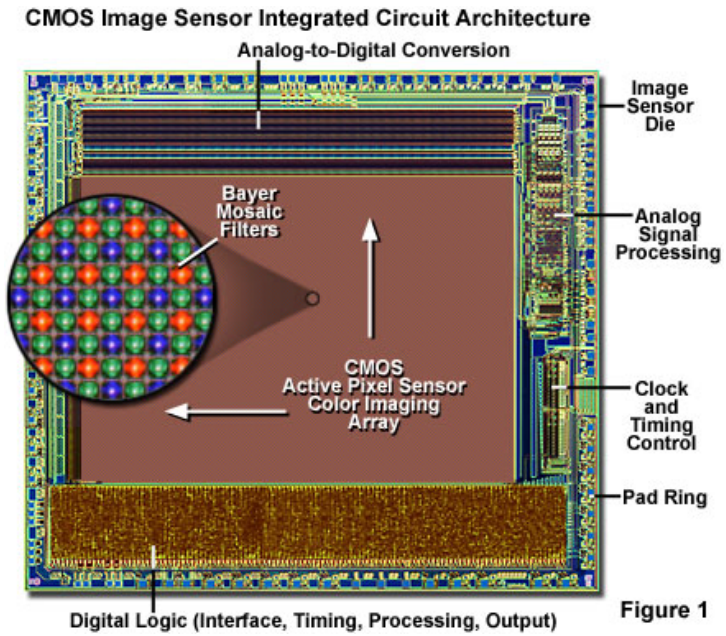
Boyle and Smith's invention improved commercial and consumer products for decades and is one of the most important technological innovations of the past half-century

Since its inception, digital imaging has progressed through improvements in CCDs and with the emergence of Complementary Metal-Oxide Silicon (CMOS) Image Sensor technology

Since 10 years CMOS has become the leading imaging technology driving the second golden age …

Nobel Prize in Physics 2009
Willard S. Boyle and George E. Smith *"for the invention of an imaging semiconductor circuit - the CCD sensor."*

CMOS Image Sensor (CIS)



Source: Olympus (optical microscopy)

(Re)-invented in the early '90

- All-in-one: Electronic Camera On Chip
- Standard CMOS technology
  - ⇨ lower production cost significantly
  - ⇨ simpler integration of complex functionalities
- Very small pixels (today ~1μm, 40M pixel)
- Single low-supply and much lower power consumption
- Increased speed (column- or pixel- parallel processing)

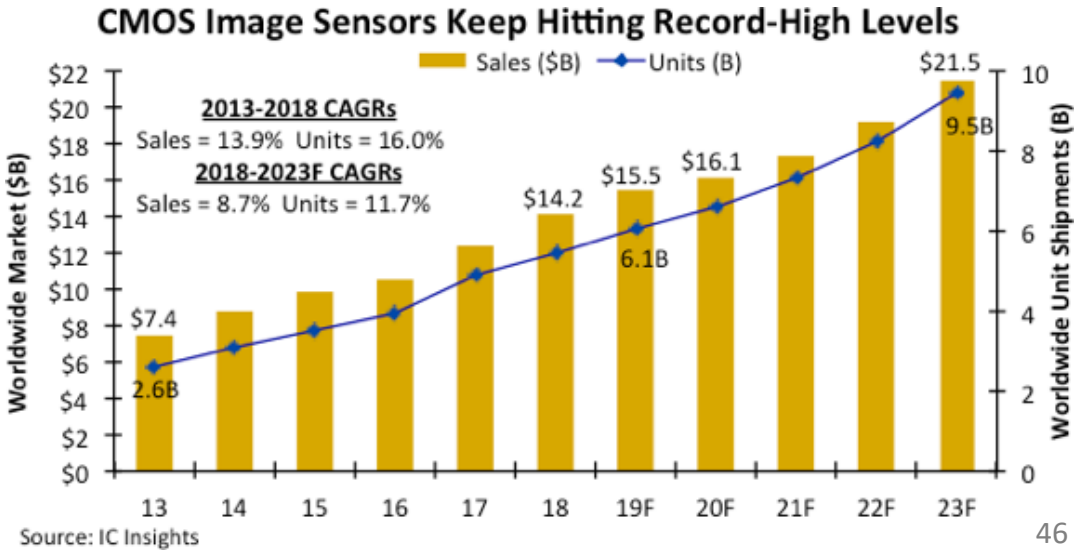
camera phones, vehicles, machine vision, human recognition and security systems

⇨ drive CMOS image sensors development and sales

cellular camera phones account for 62% of the sales

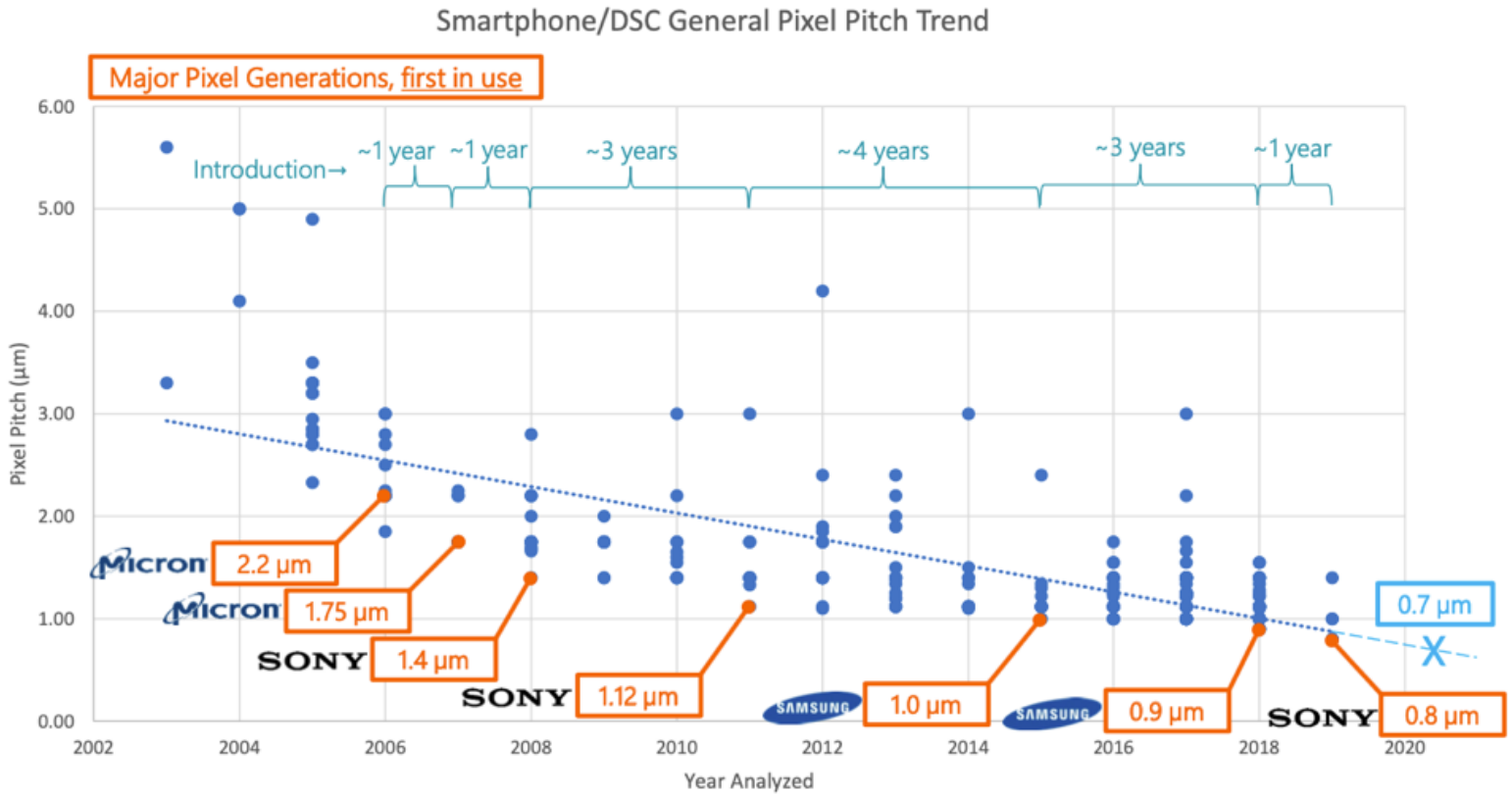
90% of the total image sensor sales in 2017

it was 74% in 2012, 54% in 2007



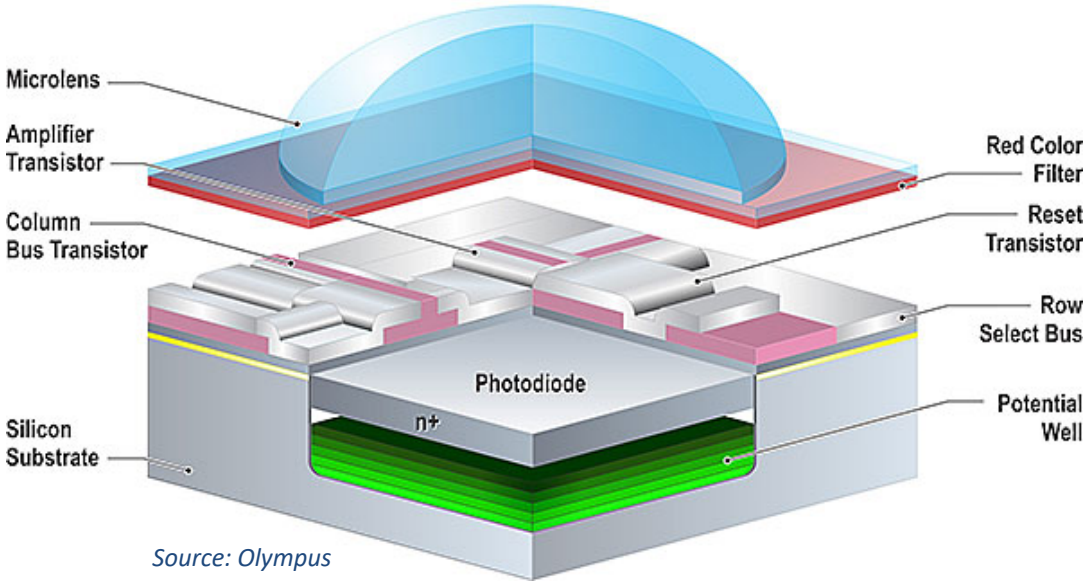
Pixel Scaling Trend

There is no Moore's Law equivalent for pixel development, however there have been natural pixel generations, a metric derived from optical system and array resolution requirements

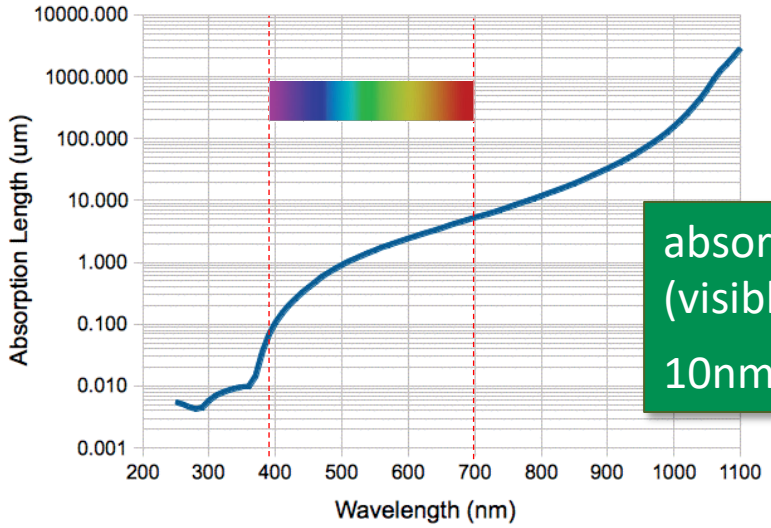


Source: R. Fontaine, IISW 2019, USA

Structure of a CIS Pixel

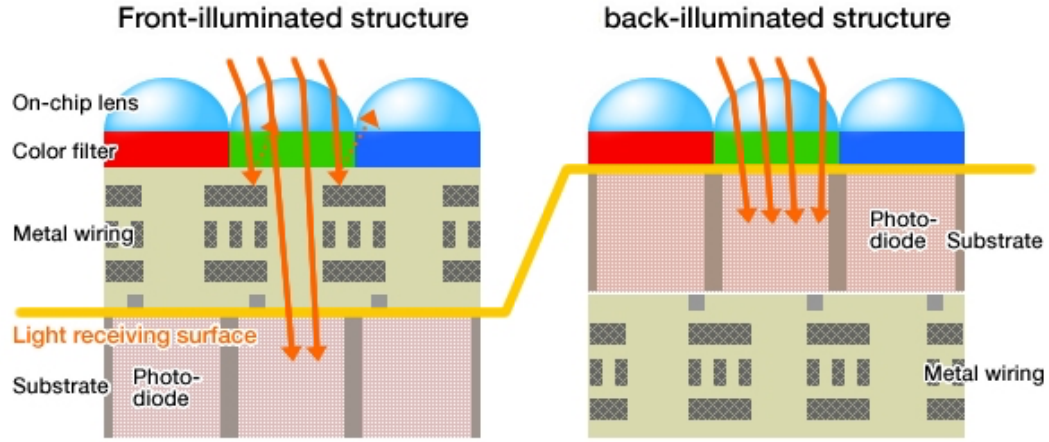


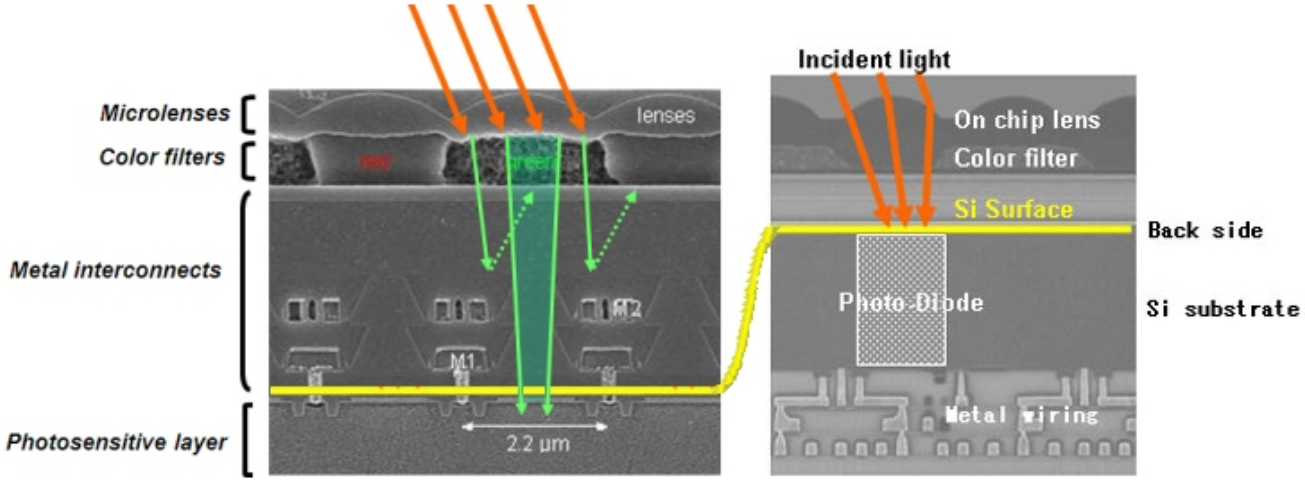
Source: Olympus



absorption depth (visible light):

10nm – 5µm

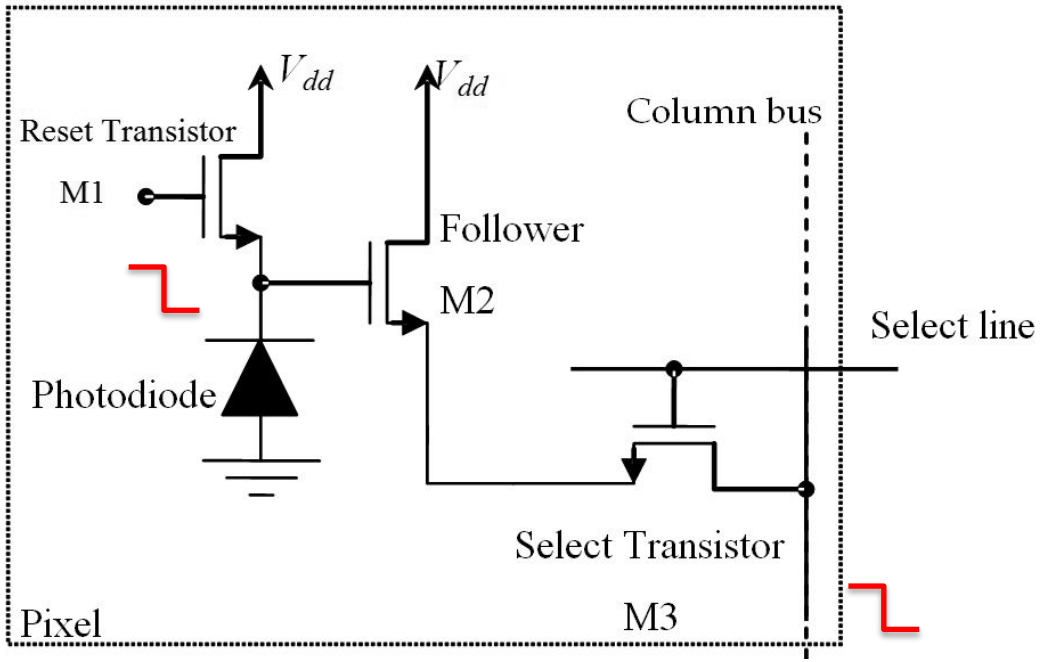




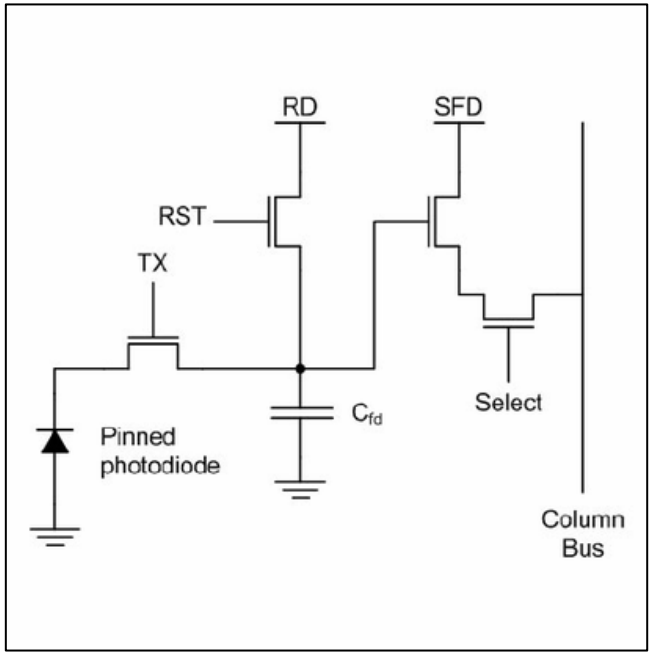
Structure of a CIS Pixel

The photodiode usually occupies 20-30% of the pixel surface … the rest if occupied by the in-pixel electronics

3T Pixel



4T Pixel



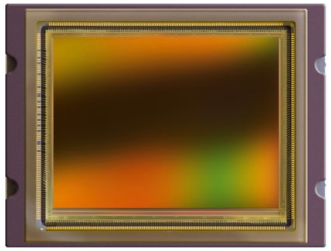
"integration time" = "exposure time", time between two consecutive reset pulses

Today, more complex structures (5T, 6T, …) are also commonly used

CMOS Image Sensors (CIS)

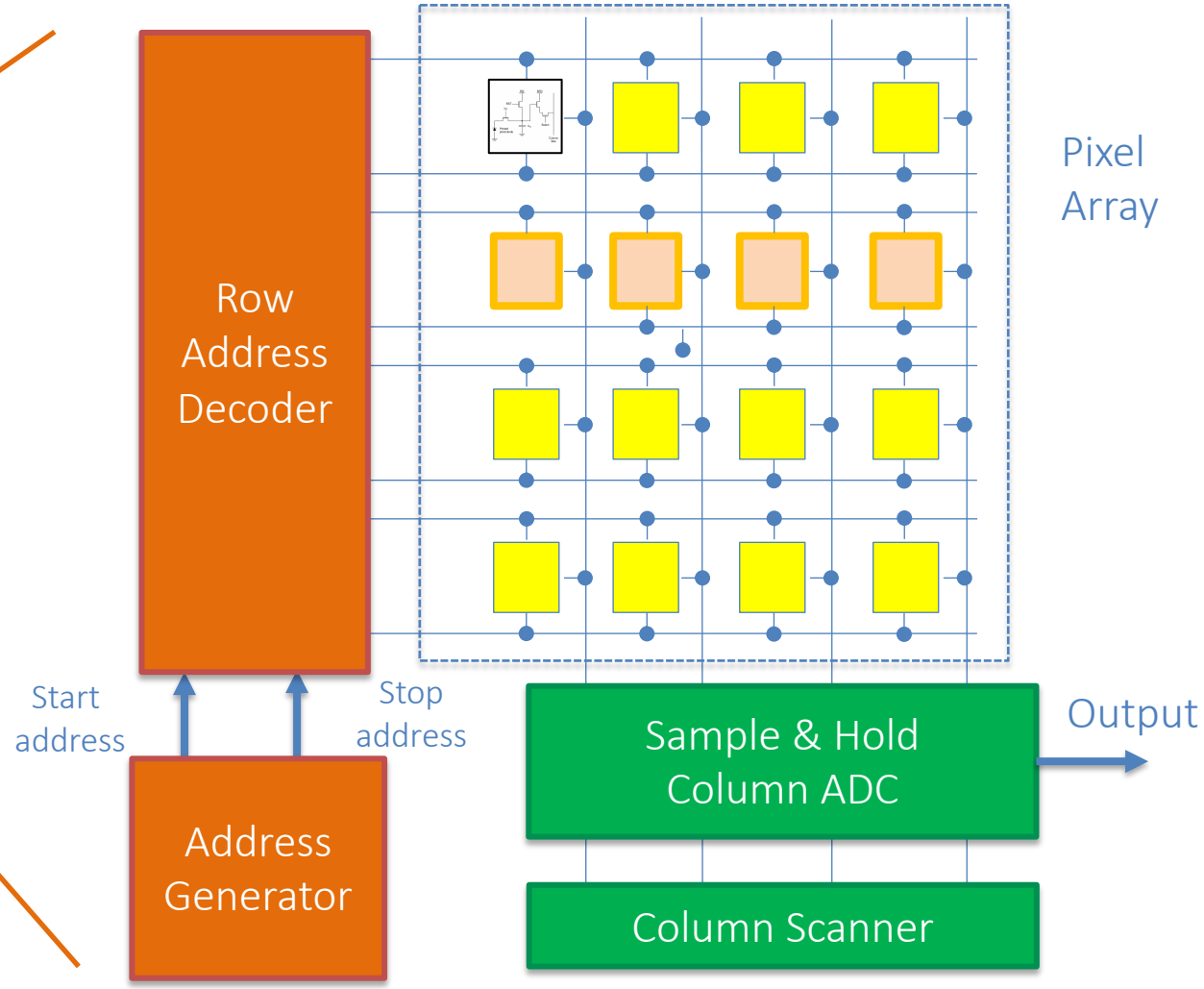
Rolling Shutter or Global shutter

Typical CMOS Image sensors supports column- or pixel-parallel readout



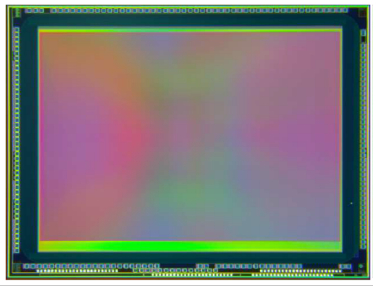
Global Shutter

Rolling Shutter

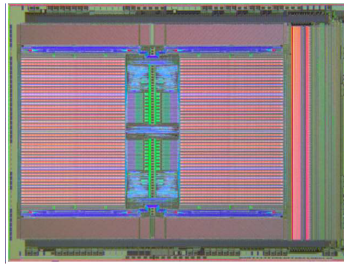


CMOS Image Sensors (CIS)

Industry's first 3-layer Stacked CMOS Image Sensor with DRAM for Smartphones *(presented at ISSCC, Feb 2017)*



Pixel array



DRAM + row drivers

Source: Sony/ISSCC

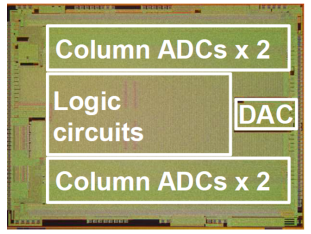
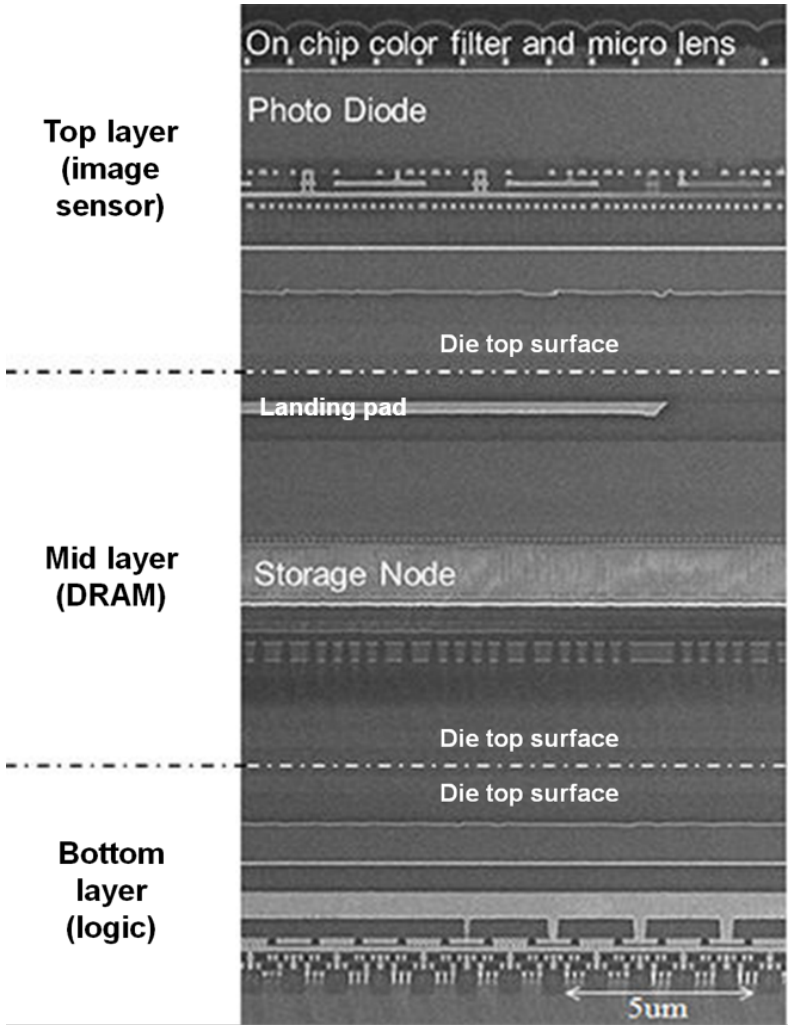
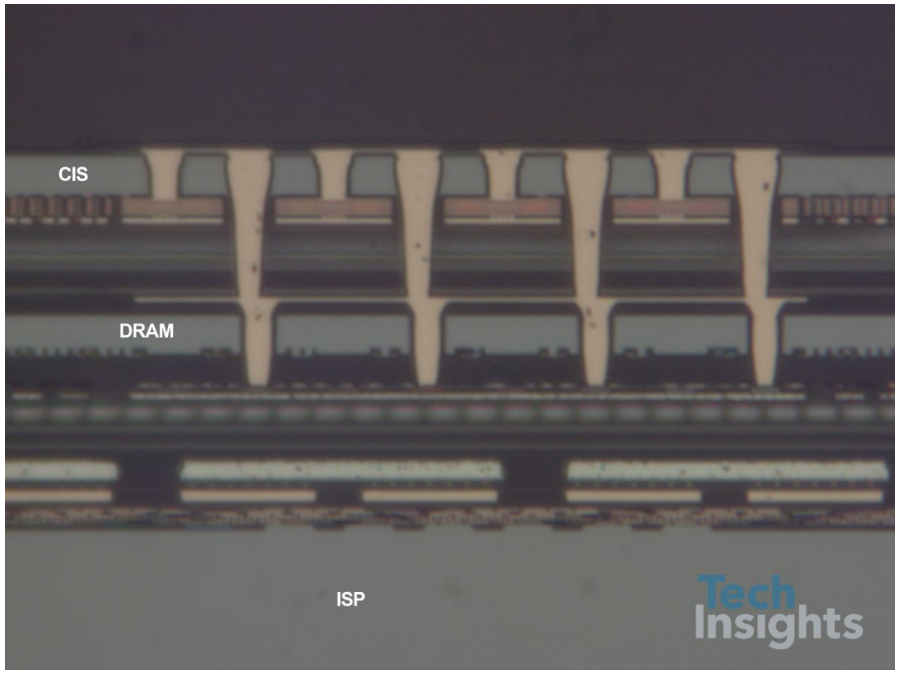


Image processor



Source: Sony



Advanced 3D assembly techniques make distinction between hybrid (separate sensor and readout chip) and monolithic more vague

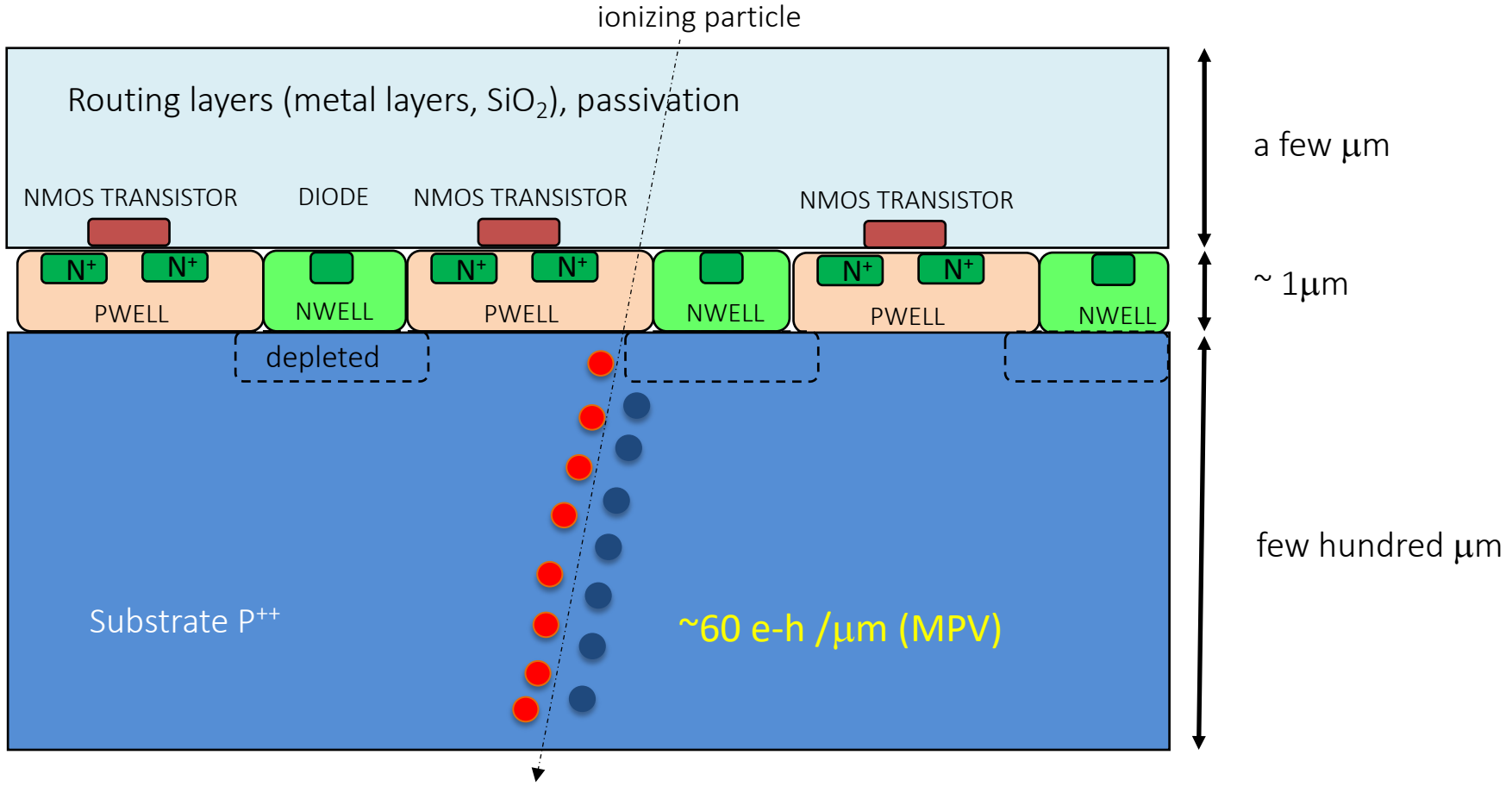
Detection of charged particles in CMOS APS

In a standard CMOS image sensor (in the early days) the photodiode is implanted in low-resistivity silicon

Depletion region is shallow, charge collection efficiency is low

Moreover the detector element covers only a small fraction of the pixel area

… not suitable for the measurement of single charged particles



Detection of charged particles in CMOS APS

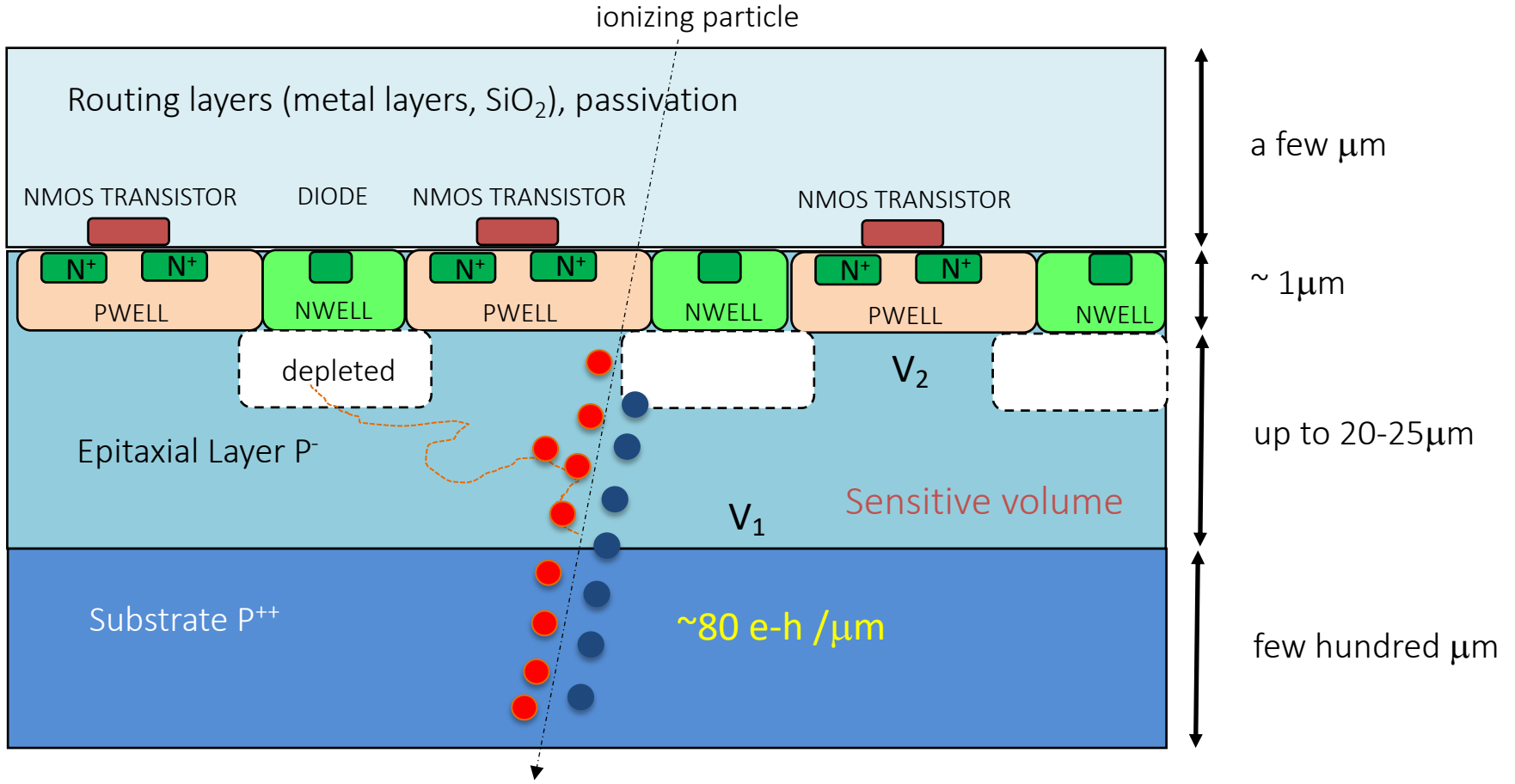
Use of an epitaxial layer with doping few order of magnitude smaller than one of the p++ substrate

Potential barriers exist at its boundaries

$$V_1 = \frac{kT}{q} ln \frac{N_{sub}}{N_{epi}}$$

$$V_2 = \frac{kT}{q} ln \frac{N_{PWELL}}{N_{epi}}$$

which keep minority carriers confined in the epi-layer ....



… till they reach the depleted region underneath the NWELL collection electrode

Detection of charged particles in CMOS APS

Doping of epitaxial layer few order of magnitude smaller than that of the p-well or the p++ substrate

Potential barriers exist at its boundaries

$$V_1 = \frac{kT}{q} ln \frac{N_{sub}}{N_{epi}}$$

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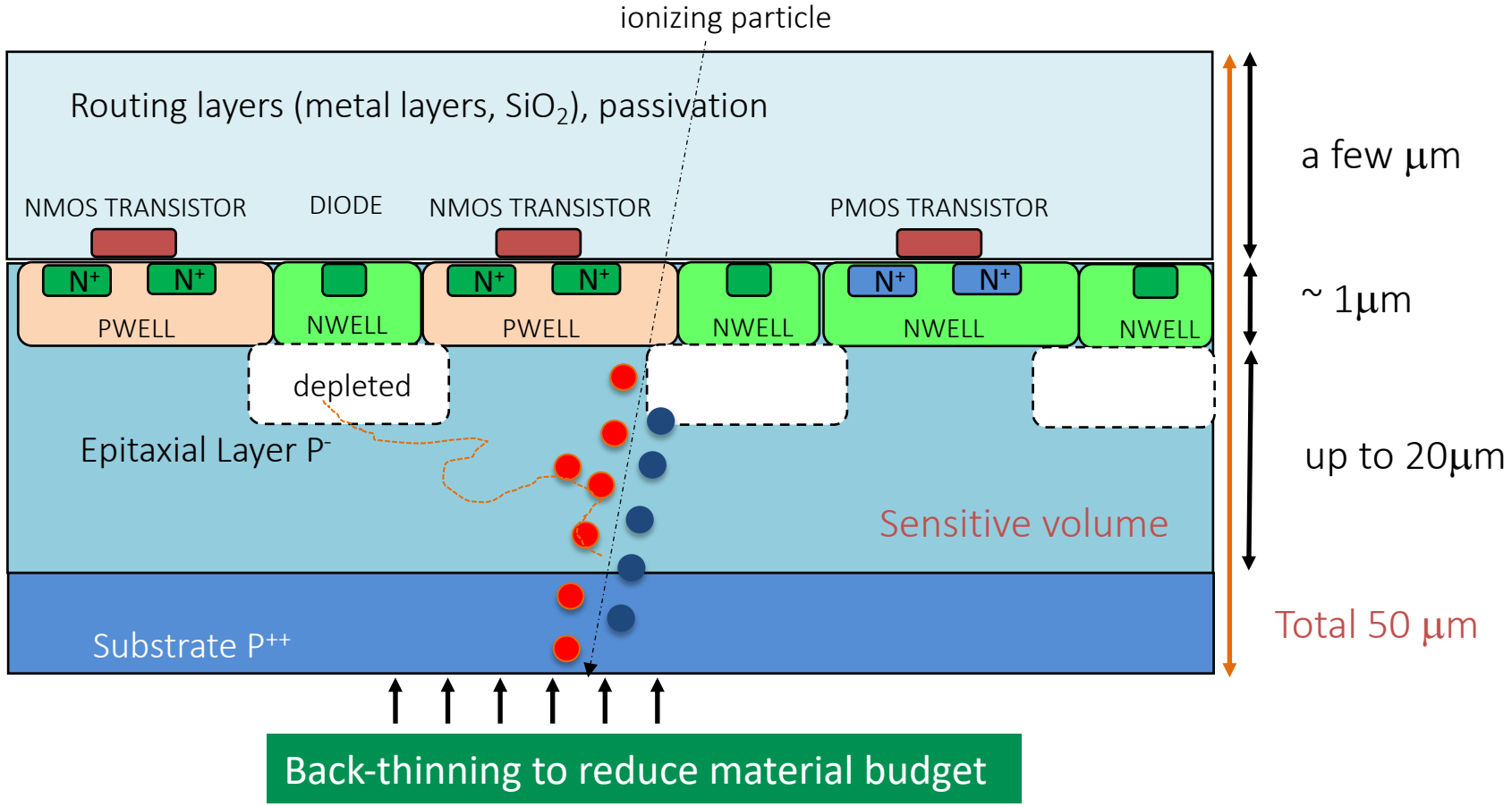

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Detection of charged particles in CMOS APS

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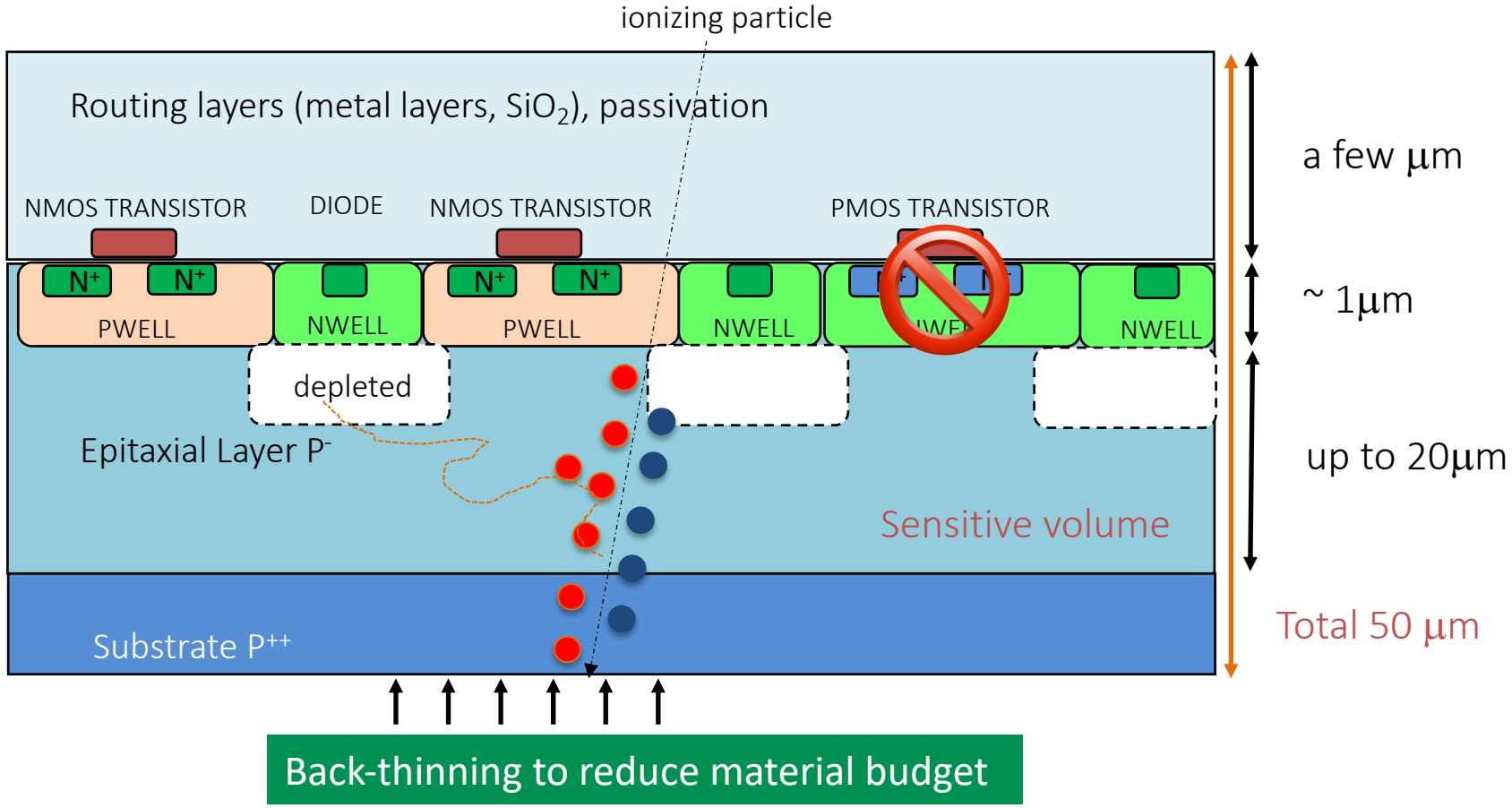


… till they reach the depleted region underneath the NWELL collection electrode

The inception of CMOS MAPS for charged particle tracking

ELSEVIER

Nuclear Instruments and Methods in Physics Research A 458 (2001) 677–689

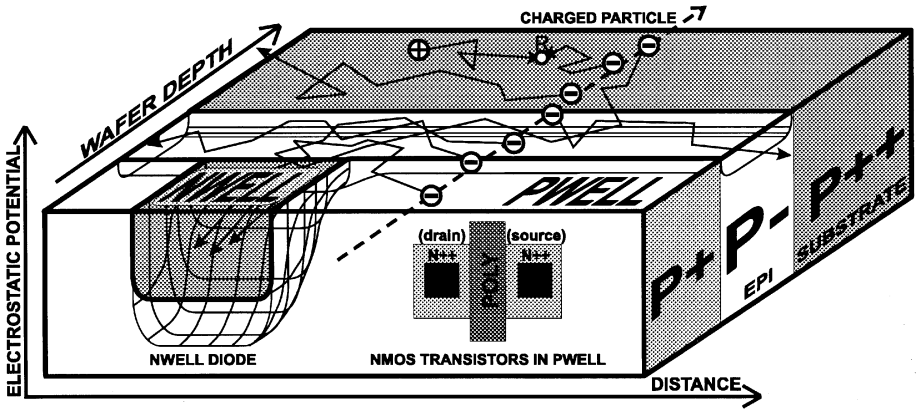
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A

www.elsevier.nl/locate/nima

A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta[a,*], J.D. Berst[a], B. Casadei[a], G. Claus[a], C. Colledani[a], W. Dulinski[a], Y. Hu[a], D. Husson[a], J.P. Le Normand[a], J.L. Riester[a], G. Deptuch[b,1], U. Goerlach[b], S. Higueret[b], M. Winter[b]

[a]*LEPSI, IN2P3/ULP, 23 rue du Loess, BP20, F-67037 Strasbourg, France*
[b]*IReS, IN2P3/ULP, 23 rue du Loess, BP20, F-67037 Strasbourg, France*



In a standard CMOS image sensor the photo diode is integrated in low-resistivity silicon:

⇨ Standard CMOS substrate

⇨ Depletion region is shallow, charge collection efficiency is low

Moreover the detector element covers only a small fraction of the pixel area

Integration of a sensor in 0.6μm CMOS process

- Twin (P and N) tubs
- Implanted in lightly doped (P^-) epitaxial silicon layer
- Grown on top of the highly doped (P^{++}) substrate

The charge collection diode is made of the junction between the NWELL and the P-type epitaxial layer

Development of CMOS APS – MIMOSA series

p-type crystalline epitaxial layer hosts n-well charge collector

Signal is generated in a high-resistivity (> 1 kΩcm) epi-layer ~20μm thick (larger values possible)

Early versions with thin and low resistivity epi-layer

R&D mostly with AMS 0.6μm and 0.35μm technology

Only one transistor type in the active area (NMOS)

⇨ 2T or 3T in-pixel circuit

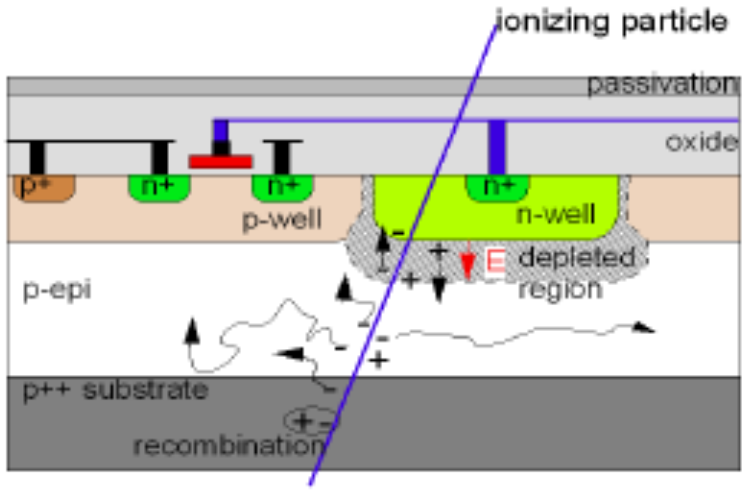
⇨ Rolling shutter architecture for matrix analogue readout

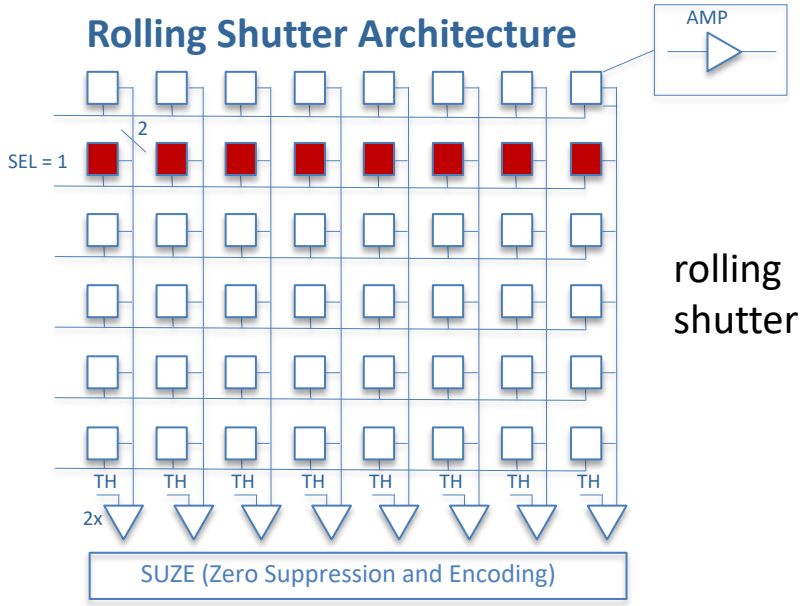
epi-layer not fully depleted

⇨ Charge collected (mostly) by diffusion and drift

⇨ Typical charge collection time < 100ns

Sensitive to radiation induced displacement damage in the epi layer ⇨ ok for applications with up to ~ 10^{12} 1MeV N_{eq}/cm^2





rolling shutter

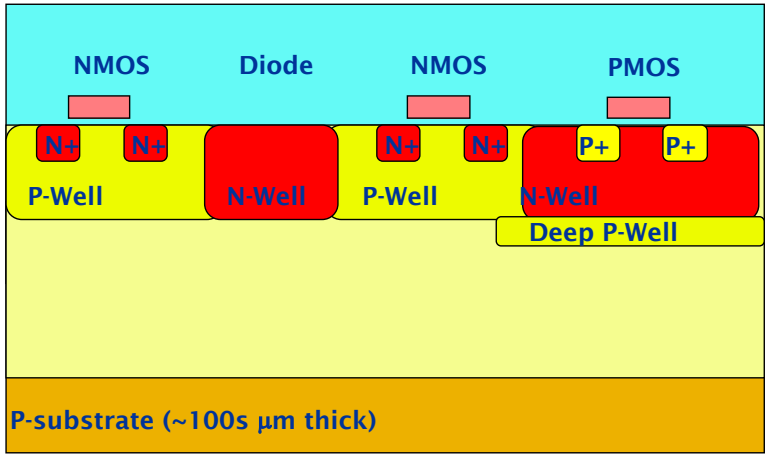
The INMAPS Process

"Monolithic Active Pixel Sensors (MAPS) in a Quadruple Well Technology for Nearly 100% Fill Factor and Full CMOS Pixel"

R. Turchetta et al. , Sensors 2008, 8, 5336-5351; DOI: 10.3390/s8095336

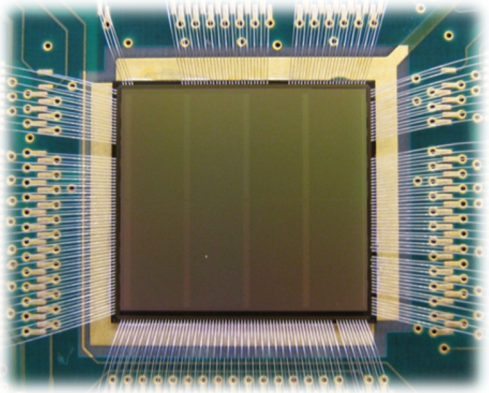
Standard CMOS with additional deep P-well implant Quadruple well technology

100% efficiency and CMOS electronics in the pixel



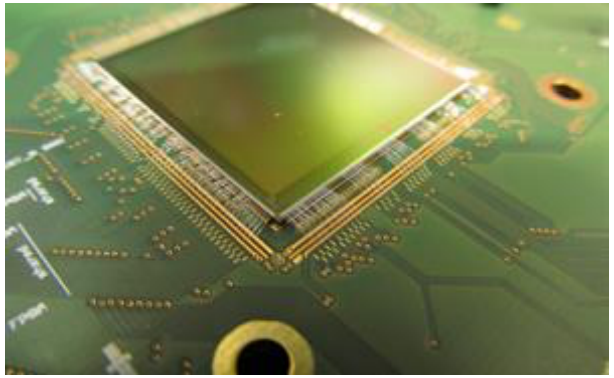
New generation of CMOS APS for scientific applications with complex CMOS circuitry inside the pixel (TowerJazz CIS 180nm)

TPAC - for ILC ECAL (CALICE)



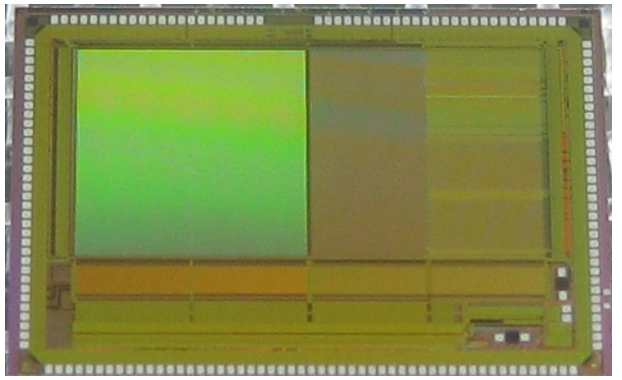
50µm pixel

PIMMS – for TOF mass spectroscopy



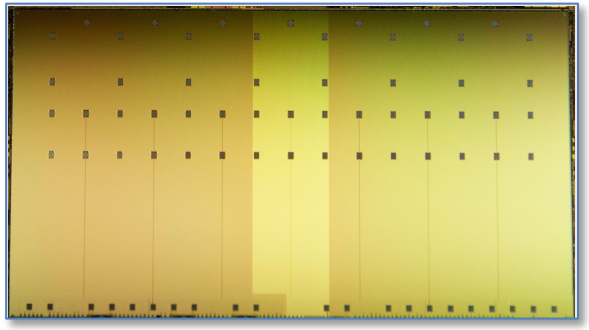
70µm pixel

CHERWELL – Calorimetry/Tracking



48 µm x 96 µm pixel

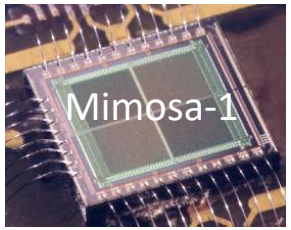
ALPIDE – Tracking

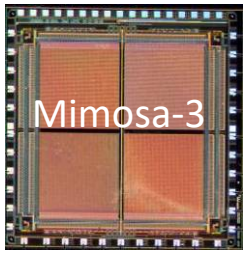


27 µm x 29 µm pixel

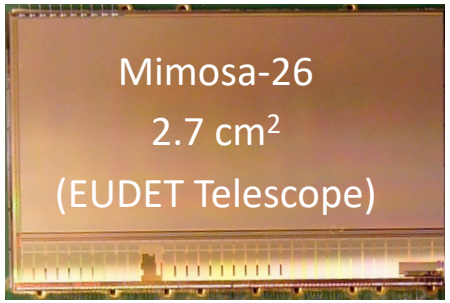
Development of CMOS APS (1999 – 2015)

Owing to the industrial development of CMOS imaging sensors and an intense R&D by HEP community …



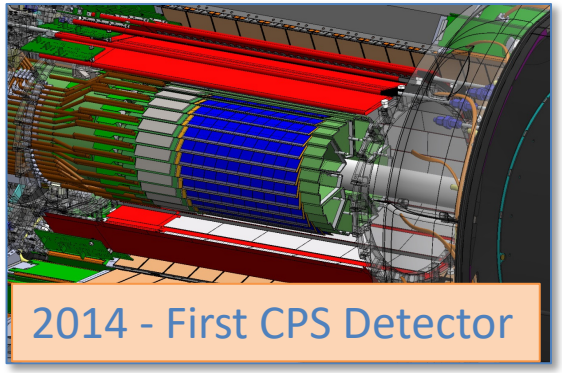


. . .

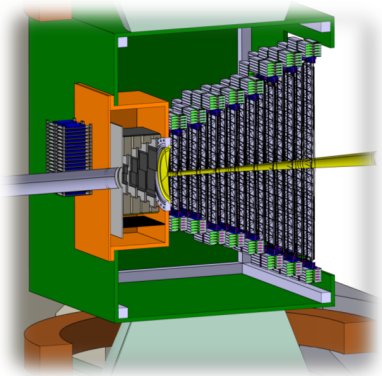


… several experiments have selected CMOS APS (STAR, ALICE, CBM, NICA MPD, sPHENIX, Mu3e)

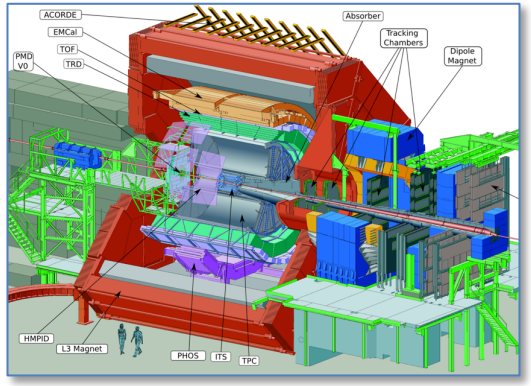
… and now intense R&D ongoing for HL-LHC (ATLAS) and LC



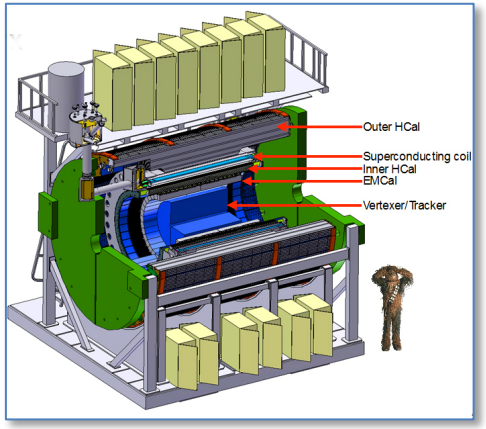
STAR HFT
0.16 m² – 356 M pixels



CBM MVD
0.08 m² – 146 M pixel



ALICE ITS Upgrade (and MFT)
10 m² – 13 G pixel



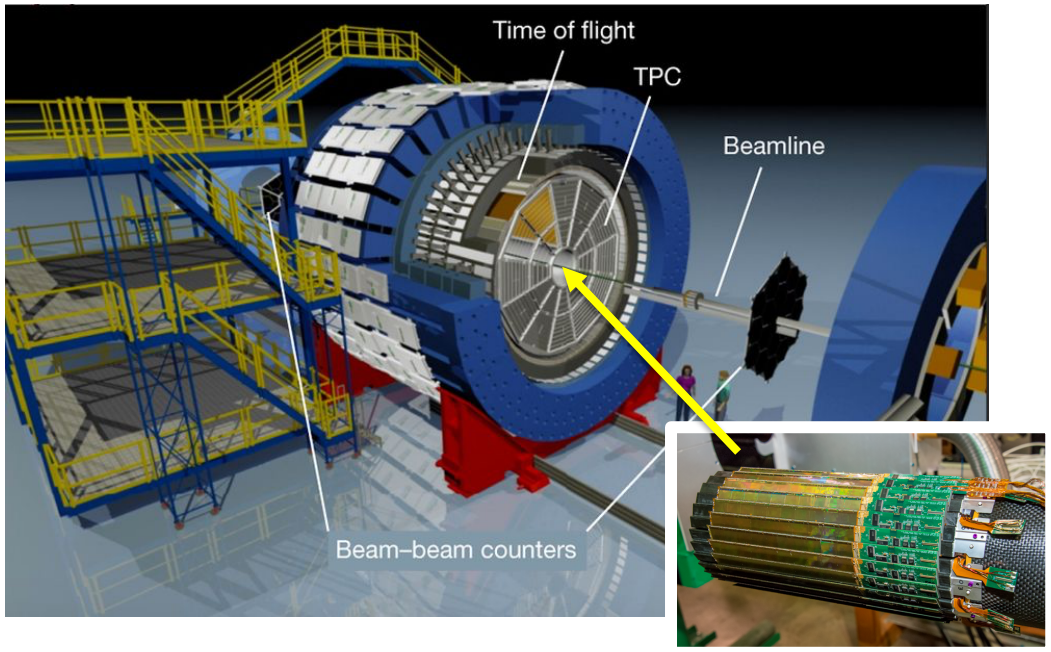
sPHENIX
0.2 m² – 251 M pixel

…

First application to Vertex Detectors

Measurement of short-lived particles in nuclear-nuclear collisions

First use of CMOS APS in HEP - STAR Pixel Detector

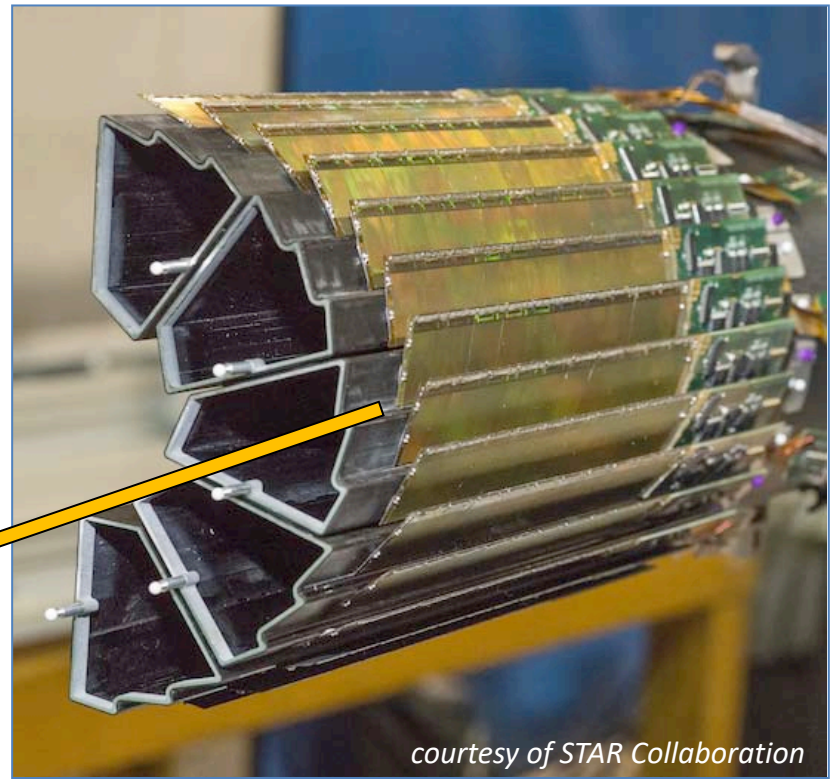


356 M pixels on ~0.16 m^2 of Silicon

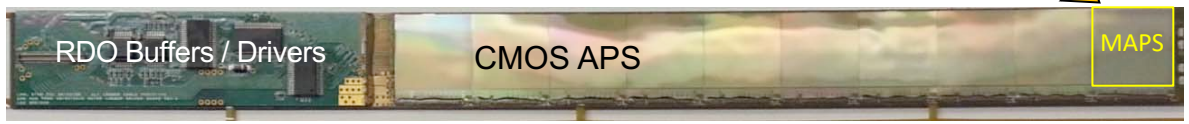
- Full detector Jan 2014
- Physics Runs in 2015-216

- 2 layers (2.8cm and 8cm radii)
- 10 sectors total (in 2 halves)
- 4 ladders/sector

20 to 90 kRad / year
$2*10^{11}$ to 10^{12} 1MeV n_{eq}/cm^2



Ladder with 10 CMOS APS sensors (~ 2×2 cm^2 each)



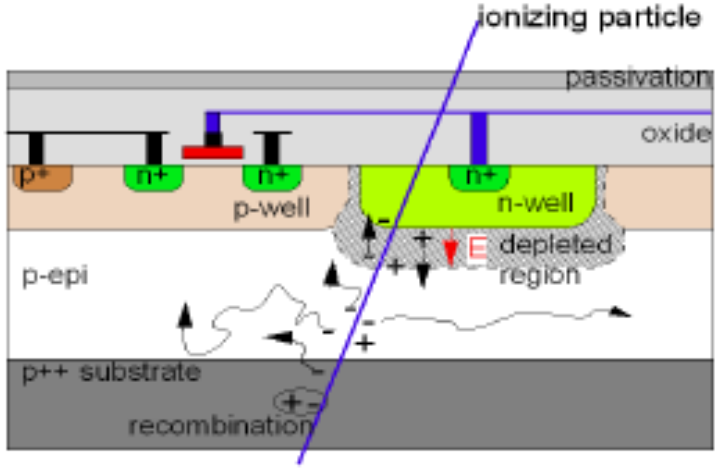
courtesy of STAR Collaboration

2-layer kapton flex cable with Al traces

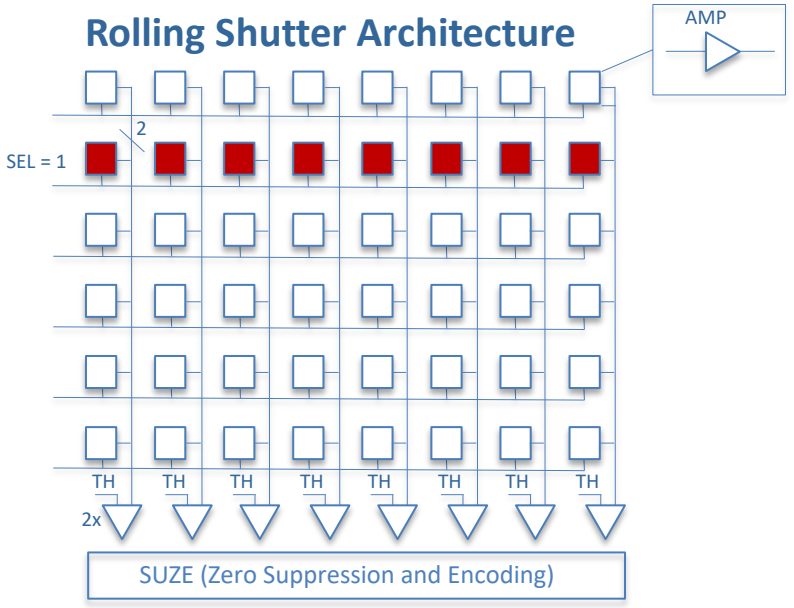
Radiation length (1st layer):
x/X_0 = 0.39% (Al conductor cable)

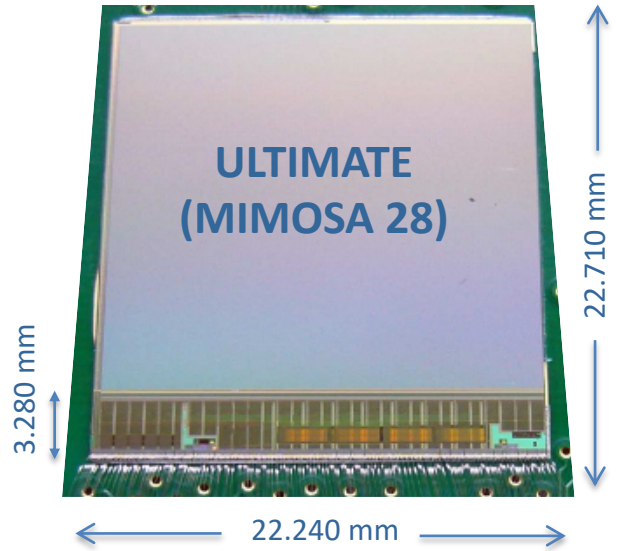
First use of CMOS APS in HEP - STAR Pixel Detector

Process: AMS 0.35μm twin-well CMOS
(NMOS only in pixel array)



courtesy of PICSEL group (IPHC)





courtesy of PICSEL group (IPHC)

20 μm high-resistivity p-epi layer (~ 800 Ω cm)

Matrix

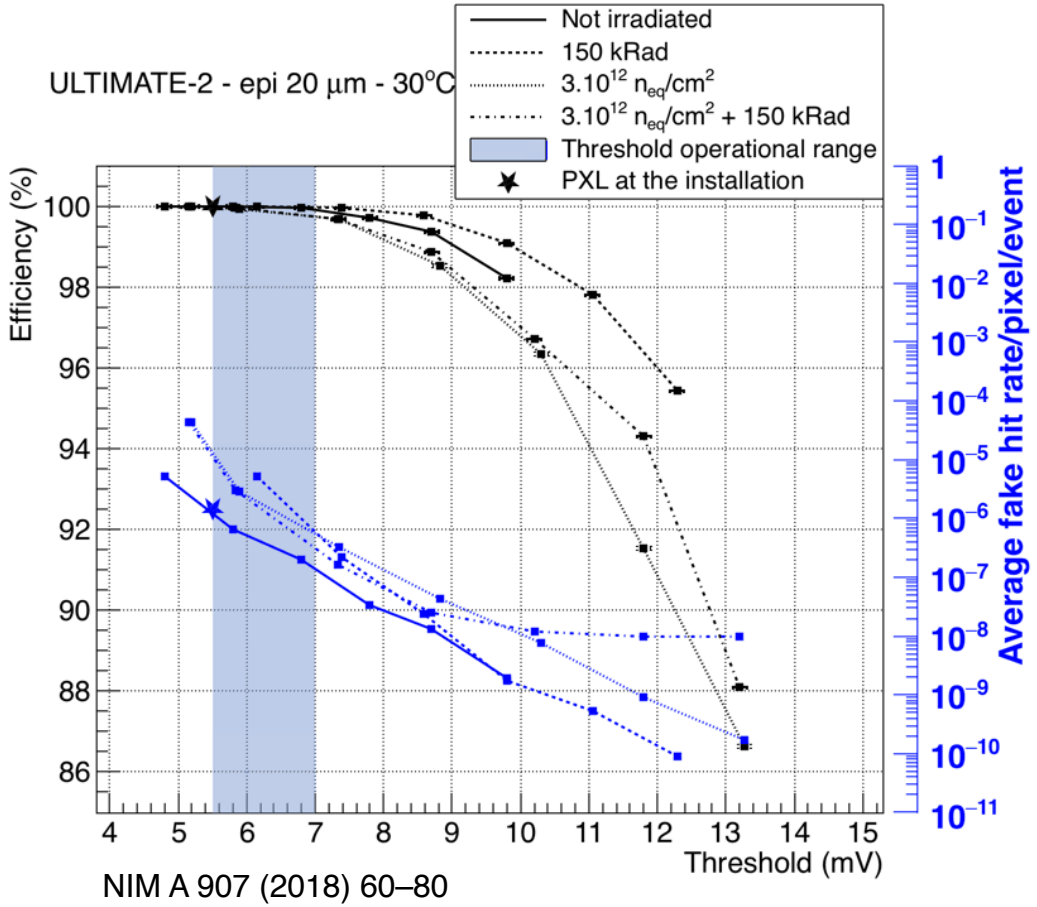
- pixel size: 20.7 μm x 20.7 μm
- 928 rows x 960 columns ~ 1M pixel
- in-pixel circuit: 2T structure
- Correlated Double Sampling

Periphery

- end-of-column discriminators and zero suppression
- ping-pong memory for frame readout (1500 word)
- 2 LVDS output @160 MHz
- 185.6 μs integration time
- ~160 mW/cm^2 power dissipation

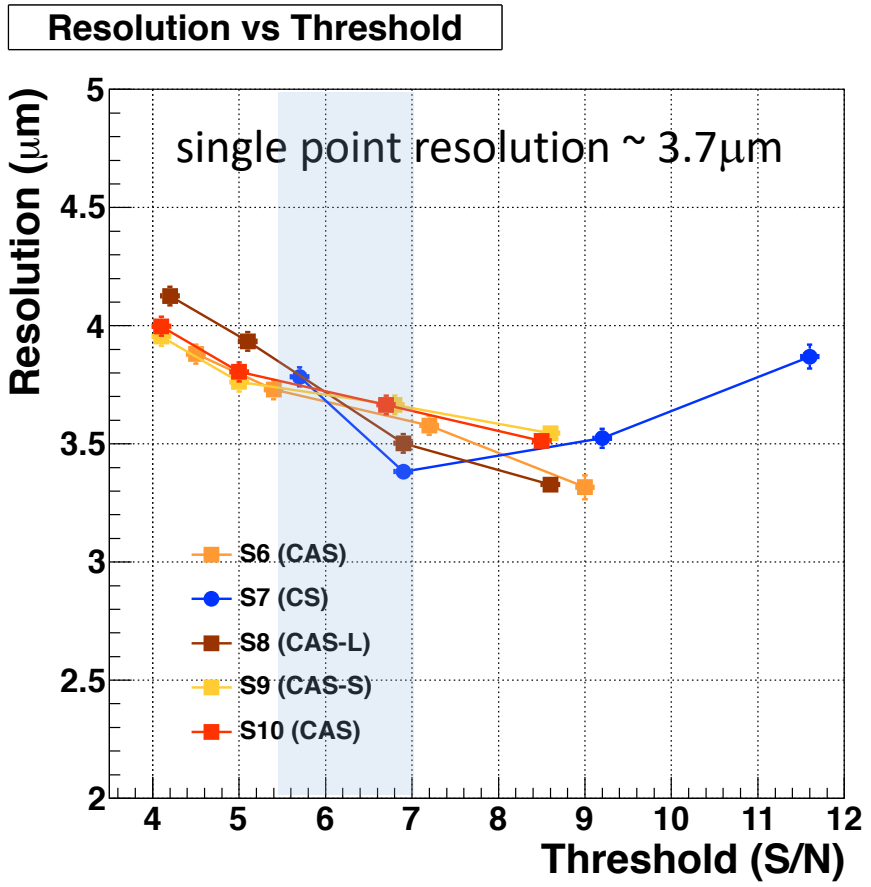
First use of CMOS APS in HEP - STAR Pixel Detector

Detection efficiency and fake hit rate



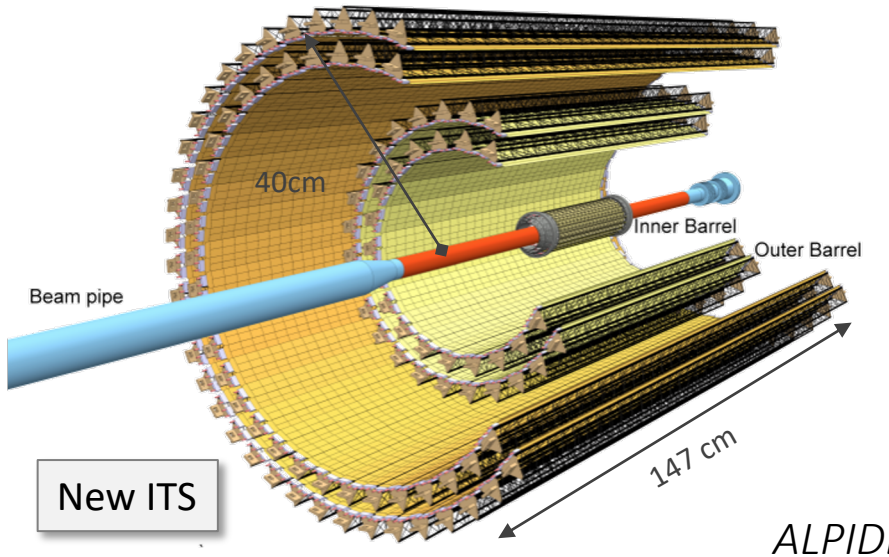
ENC ≤ 15 e^- at 30-35 °C

Spatial Resolution



Single point resolution ≈ 3.7µm

New ALICE ITS: closer to IP, thinner, higher position resolution



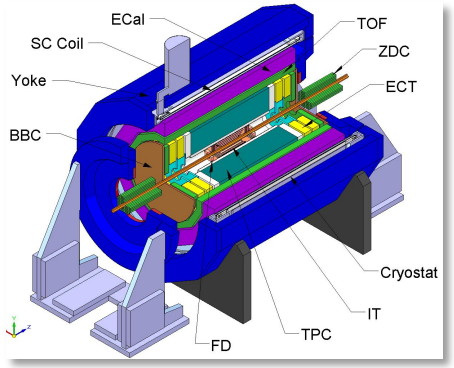
New ITS

Closer to IP:	39mm ➡ 22mm
Thinner:	~1.14% ➡ ~ 0.3% (for inner layers)
Smaller pixels:	50μm x 425μm ➡ 27μm x 29μm
Increase granularity:	20 chan/cm^3 ➡ 2k pixel/cm^3
Faster readout:	x 10^2 Pb-Pb, x 10^3 pp
10 m^2 active silicon:	12.5 G-pixels, $\sigma \approx 5\mu m$

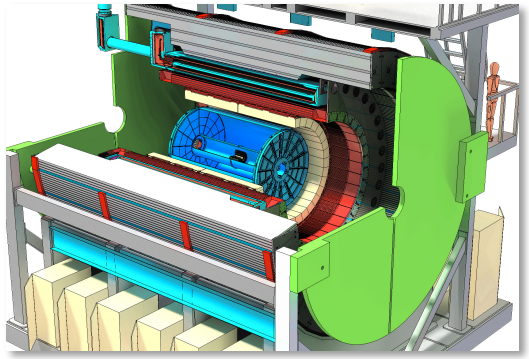
$1.5 \leq \eta \leq 1.5$

ALPIDE (ALICE Pixel Detector) - Developed for the ALICE upgrade (ITS and MFT) will be used for several other HEP detectors and non HEP applications

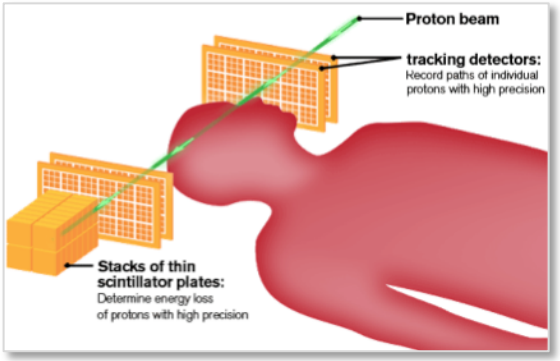
NICA MPD (@JINR)



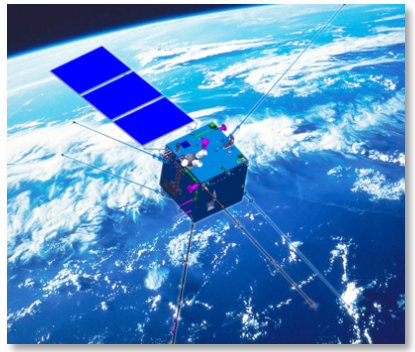
sPHENIX (BNL)



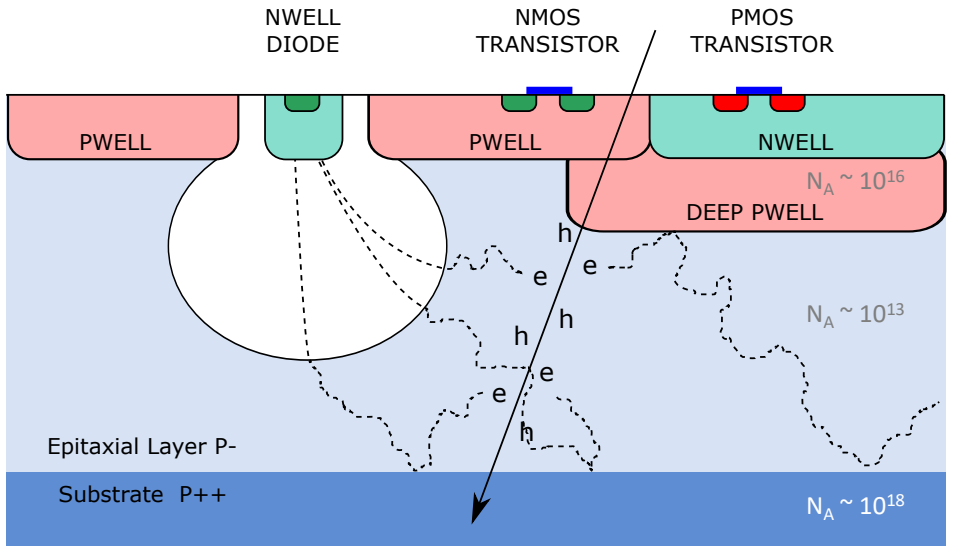
proton CT (tracking)



CSES – HEPD2 …

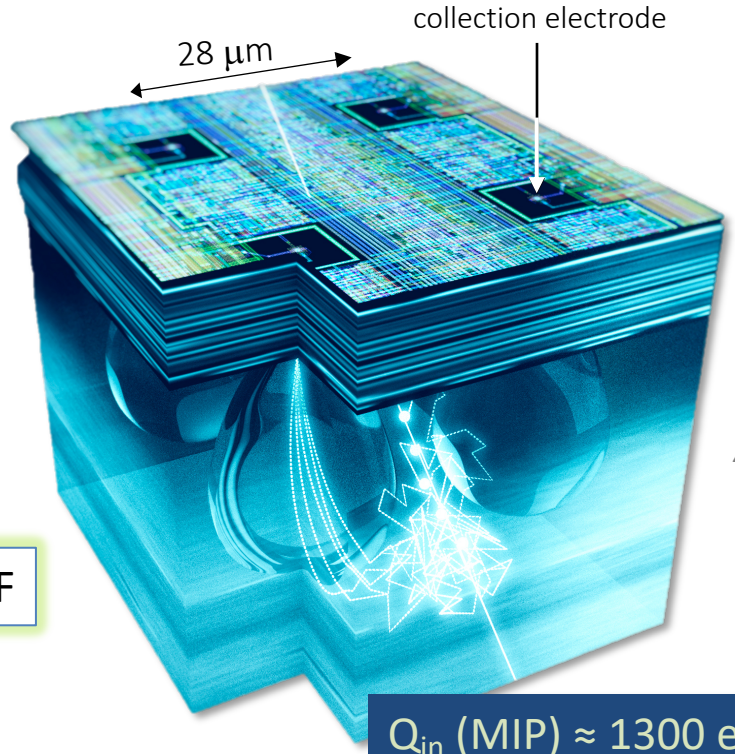


CMOS Pixel Sensor using TJ 0.18µm CMOS Imaging Process



pixel capacitance ≈5 fF (@ V_{bb} = -3 V)

2 x 2 pixel volume



Artistic view of a SEM picture of ALPIDE cross section

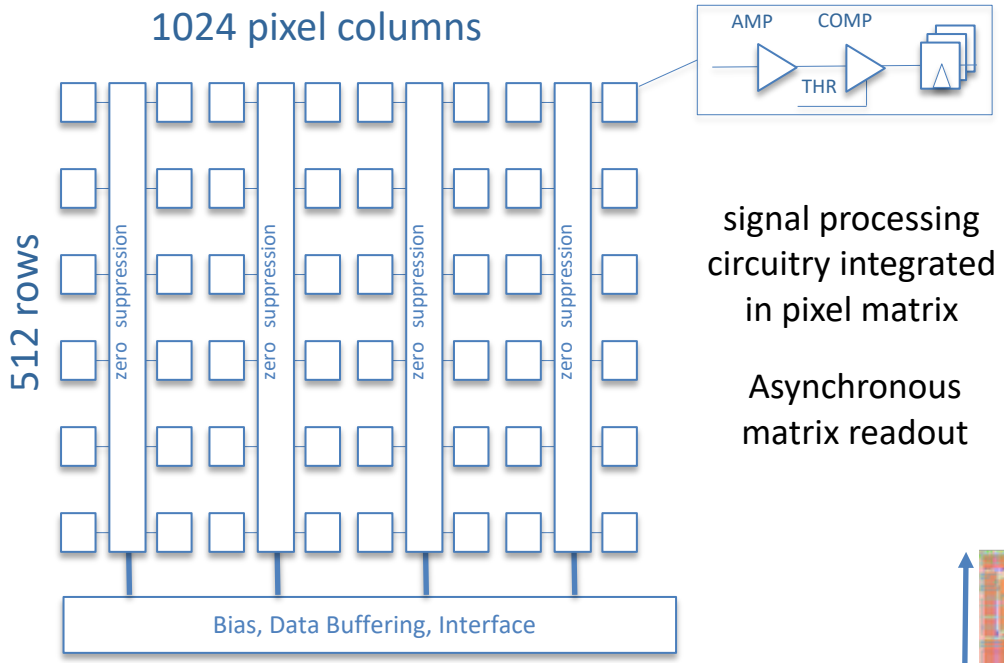
$C_{in} \approx 5$ fF

Q_{in} (MIP) ≈ 1300 e ⇨ V ≈ 40mV

- High-resistivity (> 1kΩ cm) p-type epitaxial layer (25µm) on p-type substrate
- Small n-well diode (2 µm diameter), ~100 times smaller than pixel => low capacitance (~fF)
- Reverse bias voltage (-6V < V_{BB} < 0V) to substrate (contact from the top) to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors

➔ full CMOS circuitry within active area

ALICE PIxel DEtector (ALPIDE)



signal processing circuitry integrated in pixel matrix

Asynchronous matrix readout

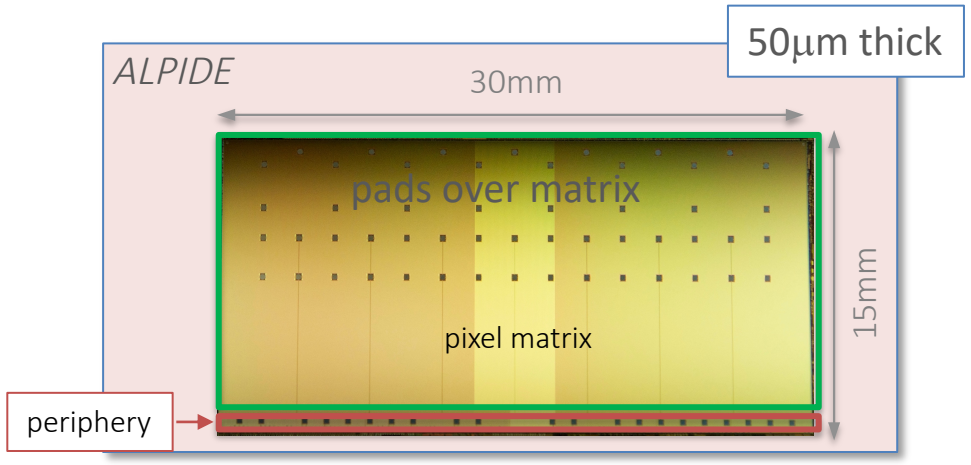
130,000 pixels / cm^2 27x29x25 µm^3

charge collection time <30ns (V_{bb} = -3V)

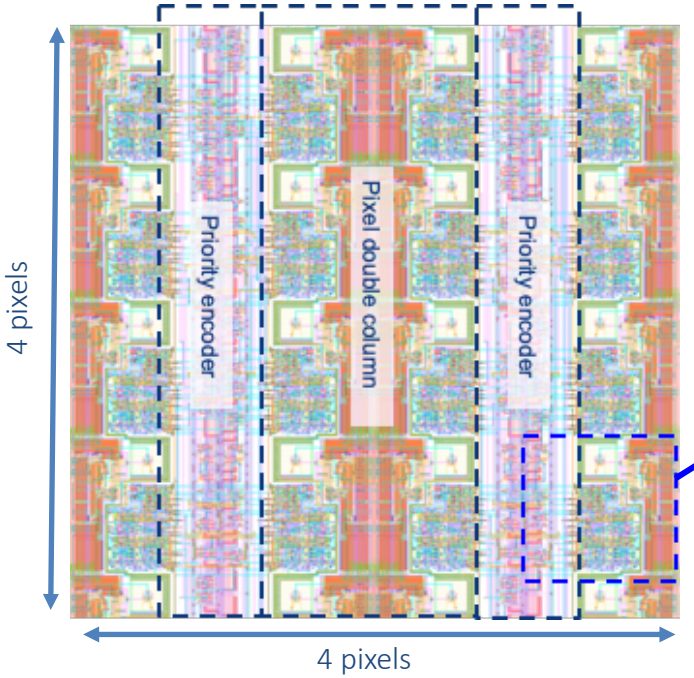
Max particle rate: 100 MHz/cm^2

fake-hit rate: < 1 Hz/ cm^2

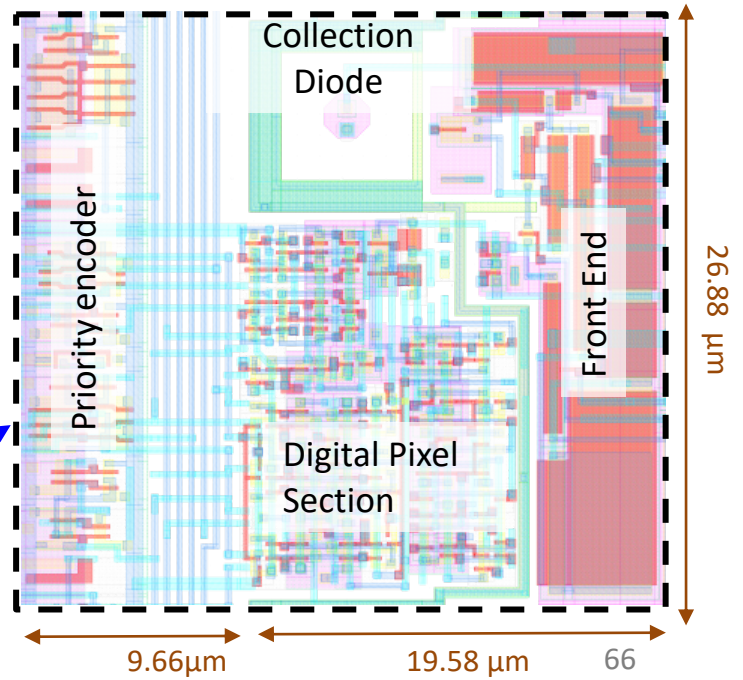
power : ≈300 nW /pixel (<40mW/cm^2)



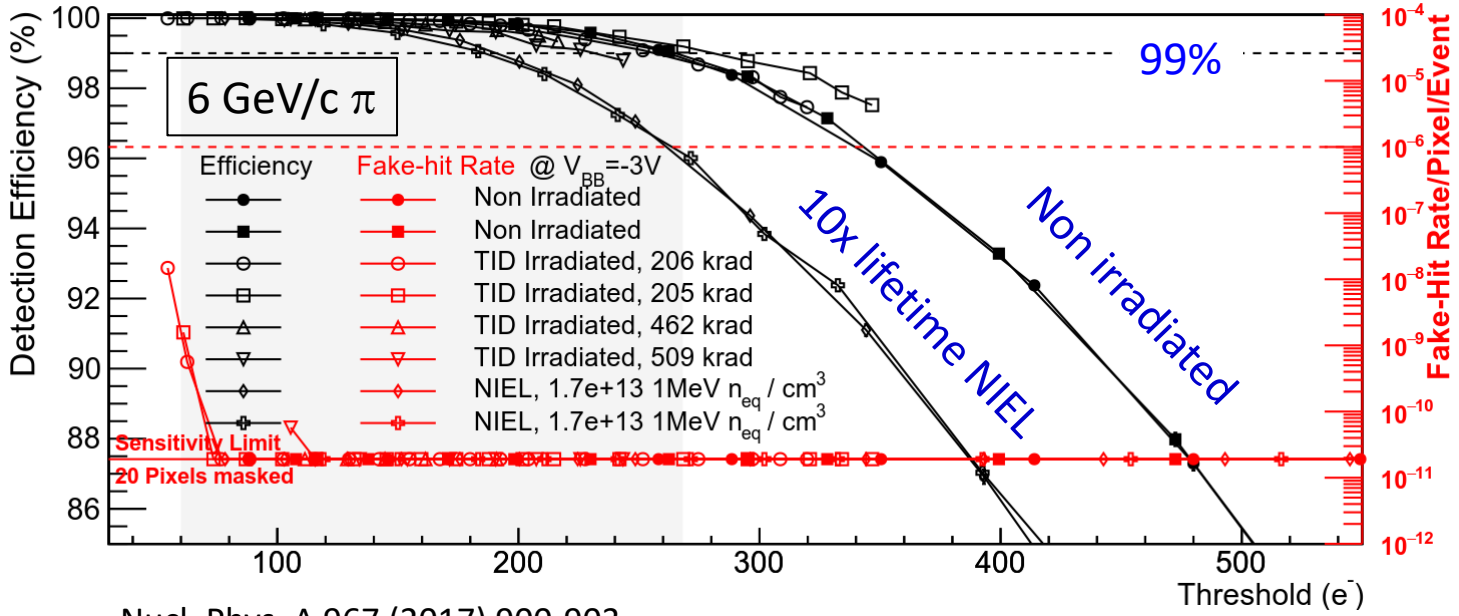
Matrix Layout



Pixel Layout



ALICE PIxel DEtector (ALPIDE)



Nucl. Phys. A 967 (2017) 900-903

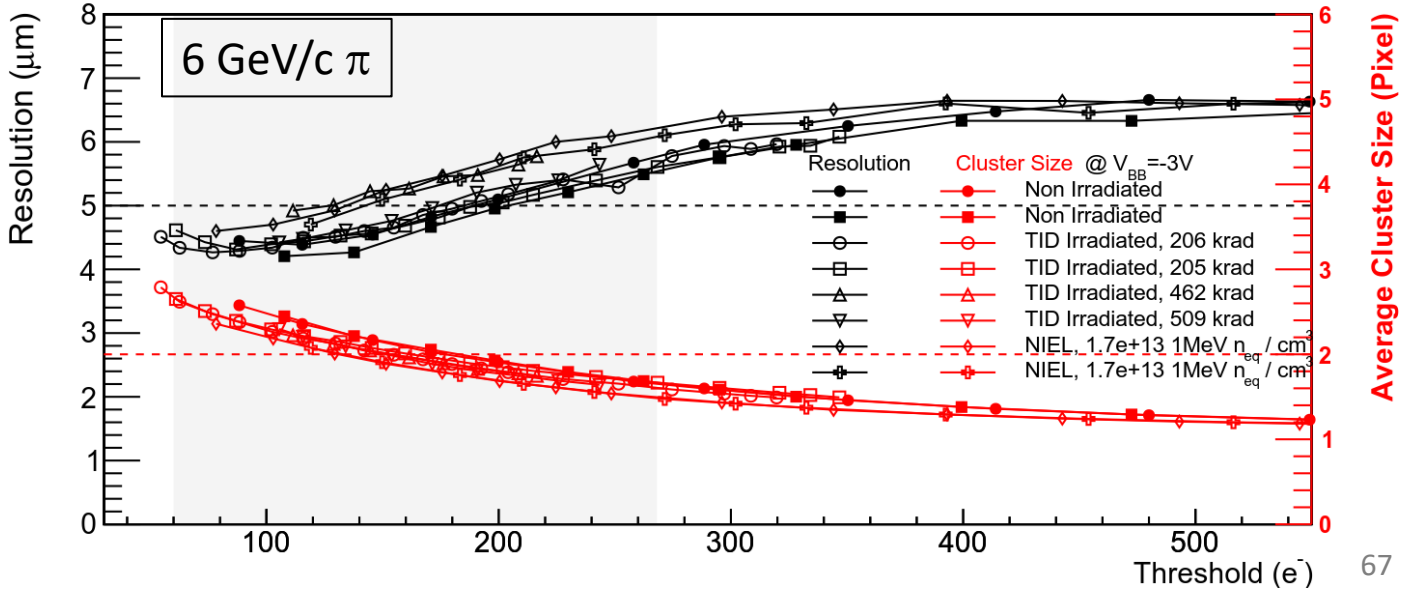
Large operational margin with only 10 masked pixels (0.002%), fake-hit rate < 2 x 10^{-11} pixel/event

Non irradiated and TID/NIEL chips similar performance

5 μm resolution @ 200 e^- threshold

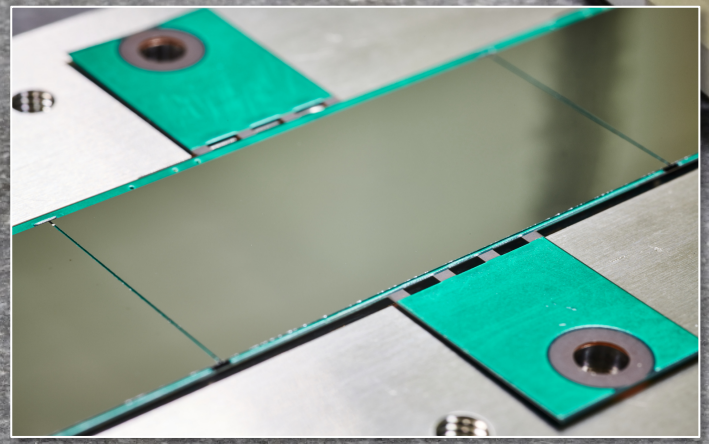
Chip-to-chip negligible fluctuations

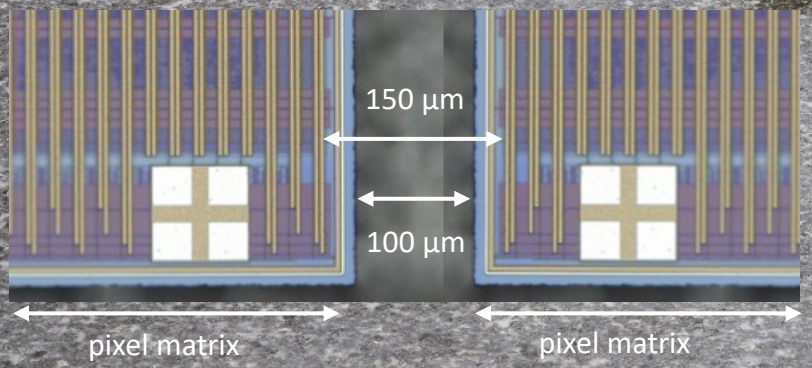
Nucl. Phys. A 967 (2017) 900-903



ALICE PIxel DEtector (ALPIDE)

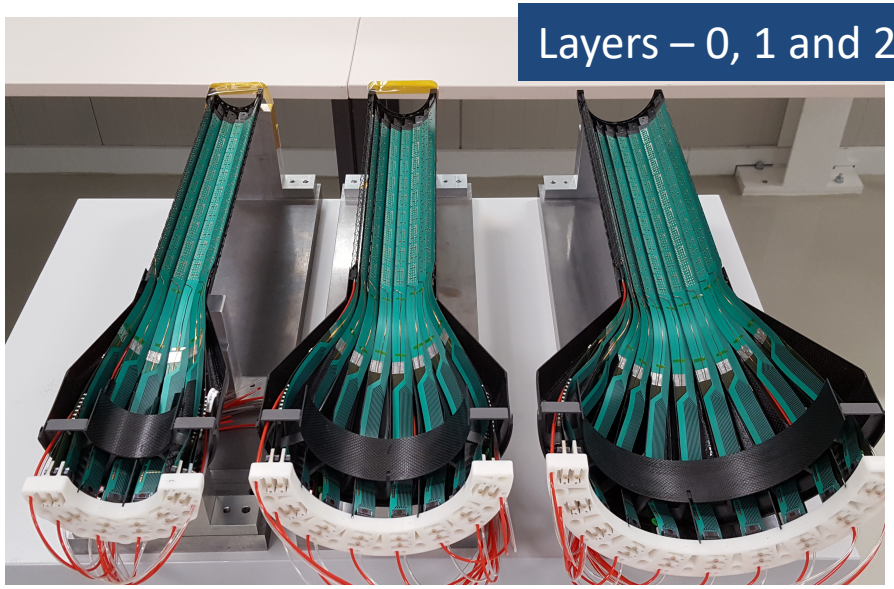
Inner Barrel is built at CERN

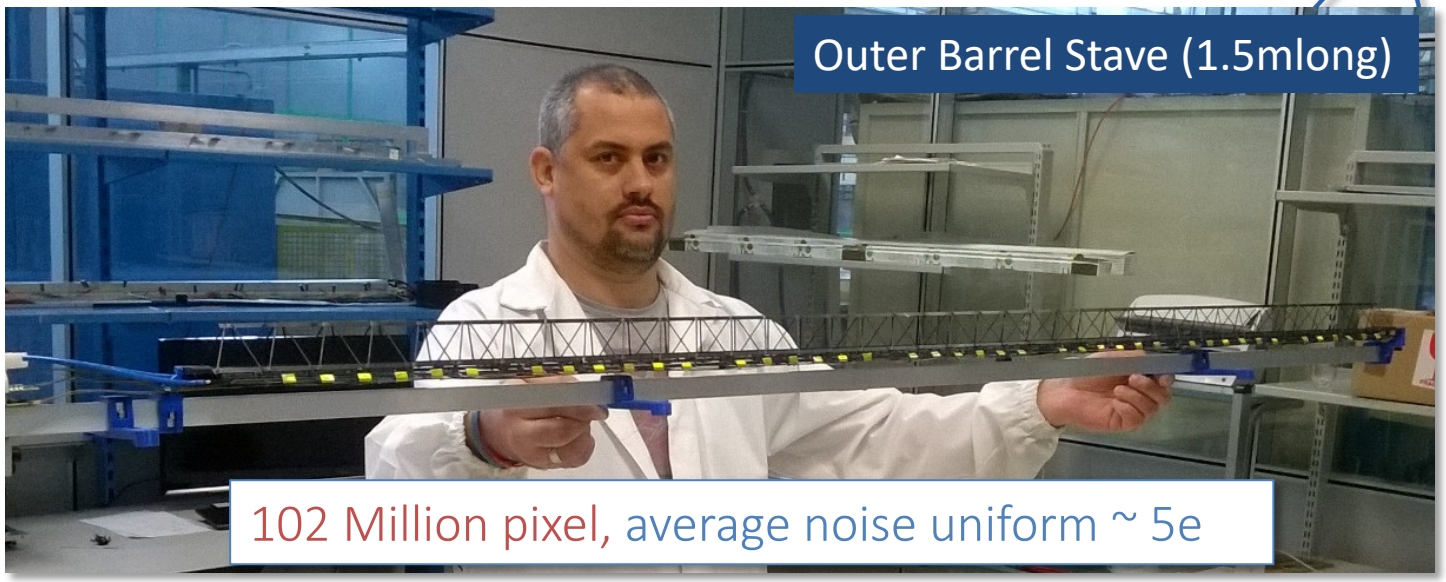




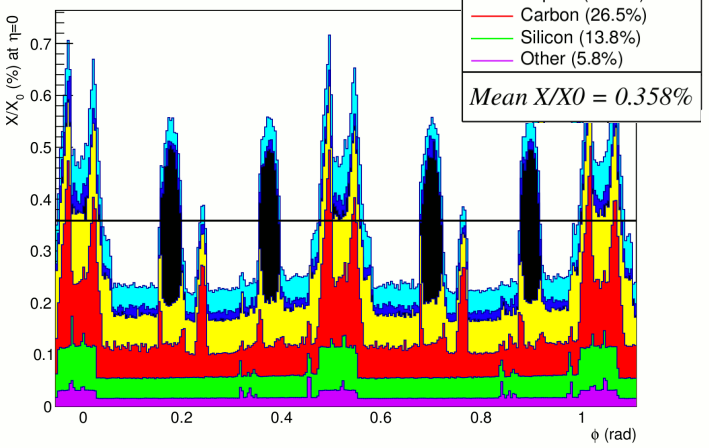
Sensors

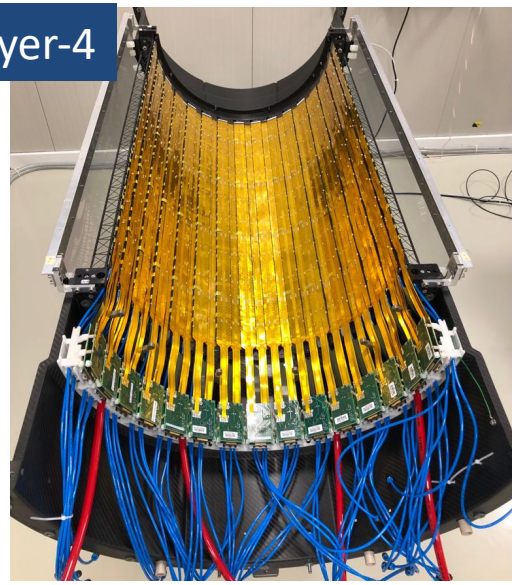
ALICE PIxel DEtector (ALPIDE)

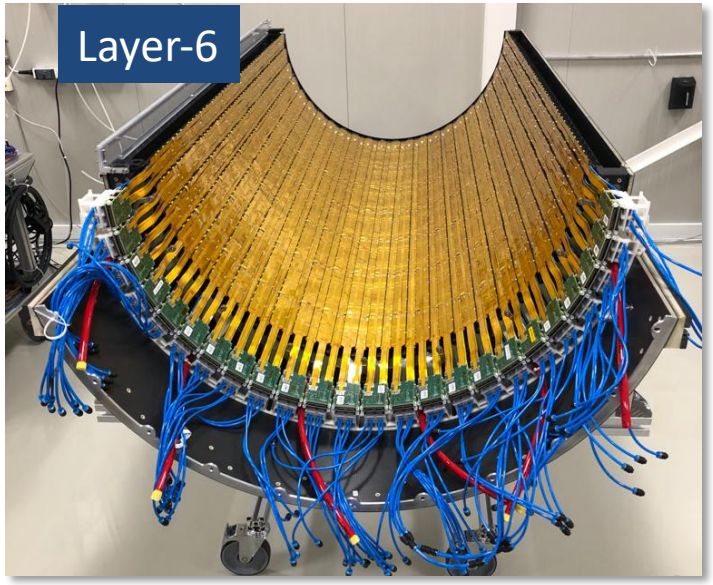




Material budget distribution







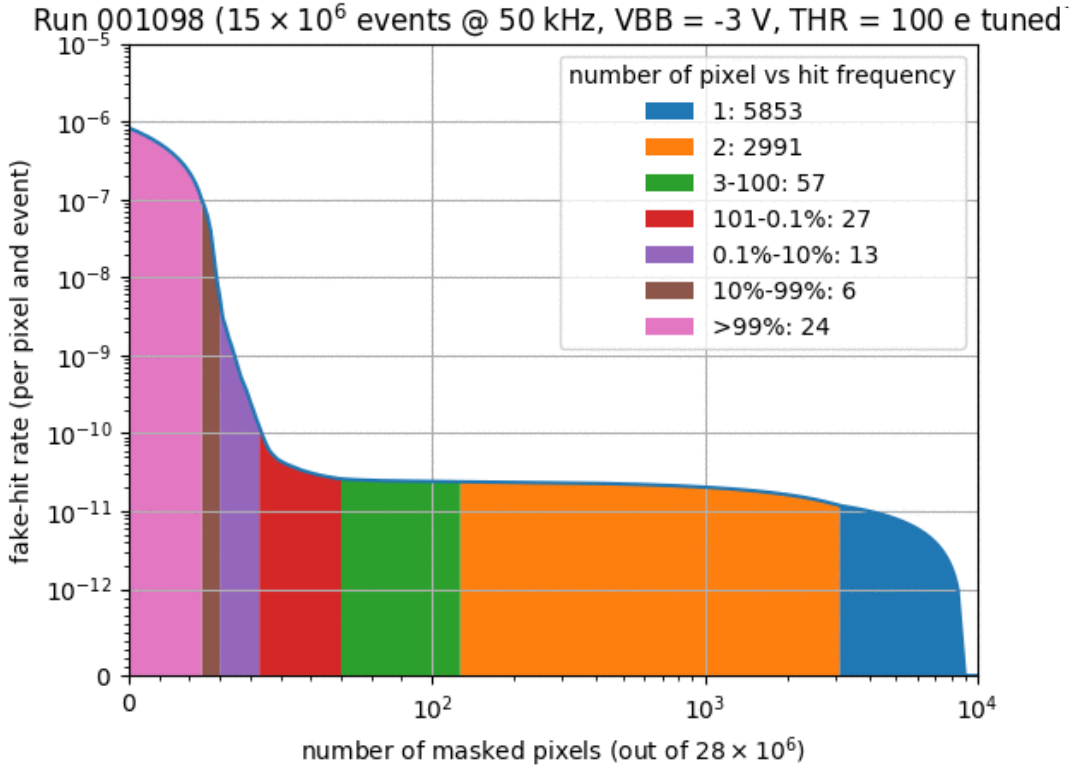
ALICE ITS Commissioning – Noise & Thresholds

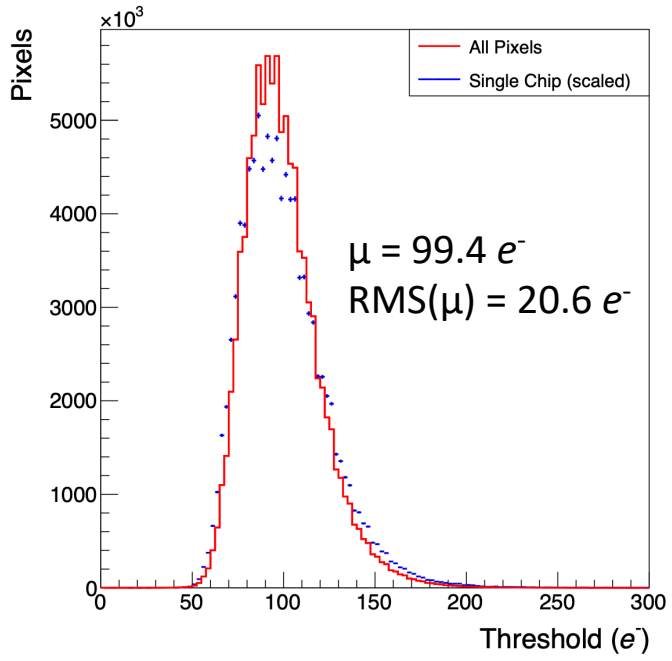
How to set the pixel threshold for the discrimination of the signal from the noise?

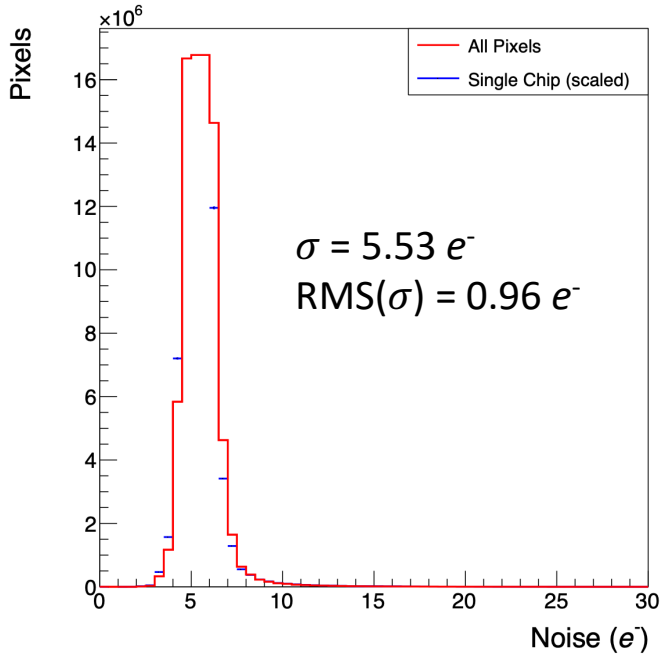
Trade-off between:

- Detection efficiency ⇨ Threshold < Charge Q_{MIP} (> 225e^-)
- Fake-hit rate ⇨ Threshold >> Noise

Extremely quiet detector!







Threshold and noise after tuning for an OL Stave (~100M pixels)

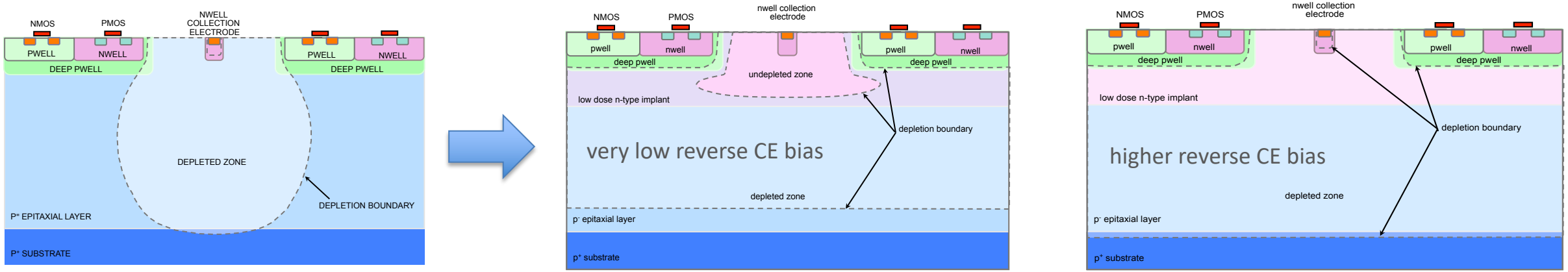
Fully Depleted MAPS

Improve speed and radiation hardness

Fully depleted MAPS – small electrodes with modified process

A process modification for CMOS Active Pixel Sensors (side activity of ALICE R&D)

A possible solution to achieve full depletion of the sensitive layer combined with a low capacitance electrode is to implement a planar junction separate from the collection electrode



Standard Process (+DEEP PWELL)

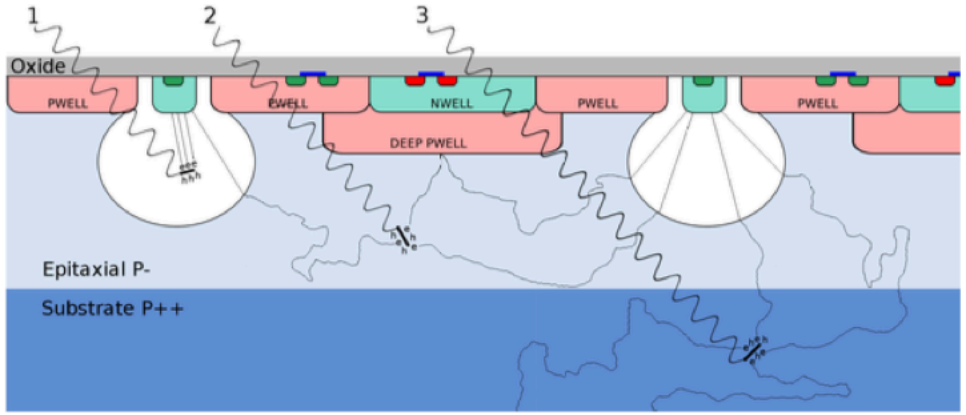
Modified Process with low-dose n-type implant (+DEEP PWELL)

The process modification requires a single additional process mask with no changes on the sensor and circuit layout

For details on process modification and experimental results: *W. Snoeys et al. NIM, A 871C (2017) pp. 90-96*

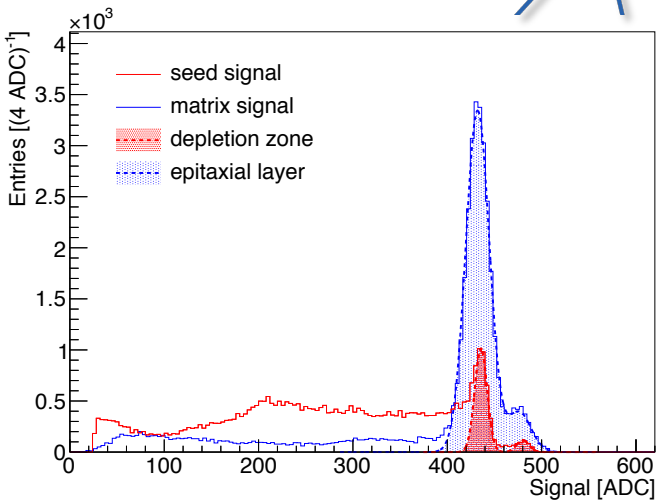
The ALICE test vehicle chip (investigator) and prototype ALPIDE chips exist with both flavors

X-ray detection in a sensor with std process



^{55}Fe: two X-Ray emission modes:

1. K-α: 5.9keV (1640 e/h in Si), rel. freq.: 89.5%, attenuation length in Si: 29μm
2. K-β: 6.5keV (1800 e/h in Si), rel. freq.: 10.5%, attenuation length in Si: 37μm

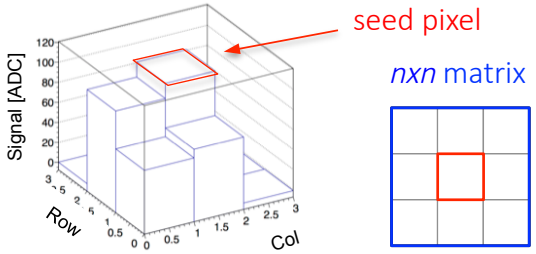


For X-ray absorption in sensors fabricated with the std process, three cases can be defined

1. Absorption in depleted volume: charge collected by drift, no charge sharing, single pixel cluster

J. Van Hoorne NSS 2016

   - These events populate the calibration peak in the signal histogram
   - Charge collection time expected to be <1ns



2. Absorption in non depleted volume of the epitaxial layer: charge partially collected by diffusion and then drift, charge sharing depending on position of X-Ray absorption
   - Charge collection time expected to be dependent on distance of X-Ray absorption from the depleted volume, and longer than events of case 1.

3. Absorption in substrate
   - Contribution depending on depth of X-Ray absorption, and charge carrier lifetime within substrate

TJ standard process – charge collection time and seed signal

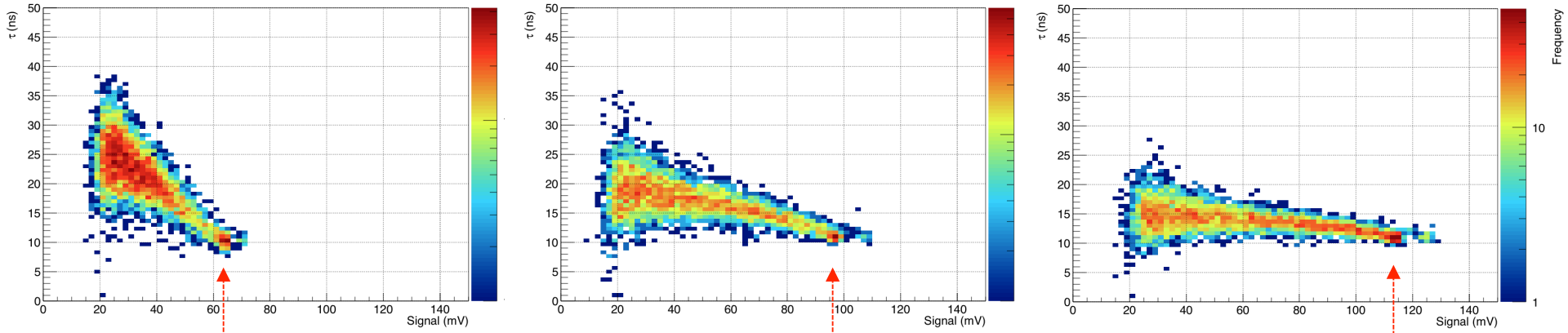
Tests performed on investigator chip (same pixel as ALPIDE) with analogue readout

Pixel size: 28 x 28 μm^2, CE: 2 x 2 μm^2 centered in a 8 x 8 μm^2 opening, P-well & substrate @ -6V, CE @ 1V

V_{BB} = -1V

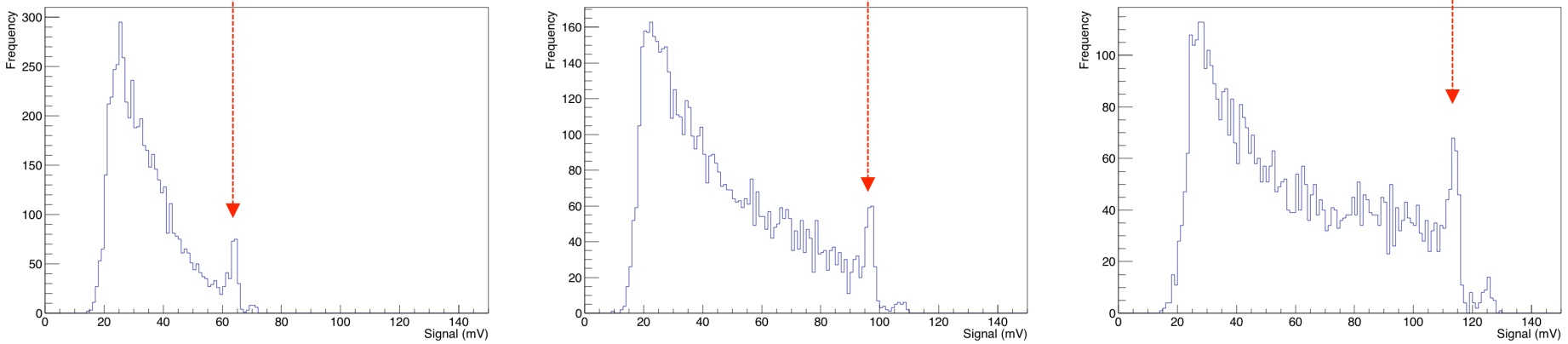
V_{BB} = -3V

V_{BB} = -6V



Calibration (drift) peaks

Signal:



Fully depleted MAPS – small electrodes with TJ modified process

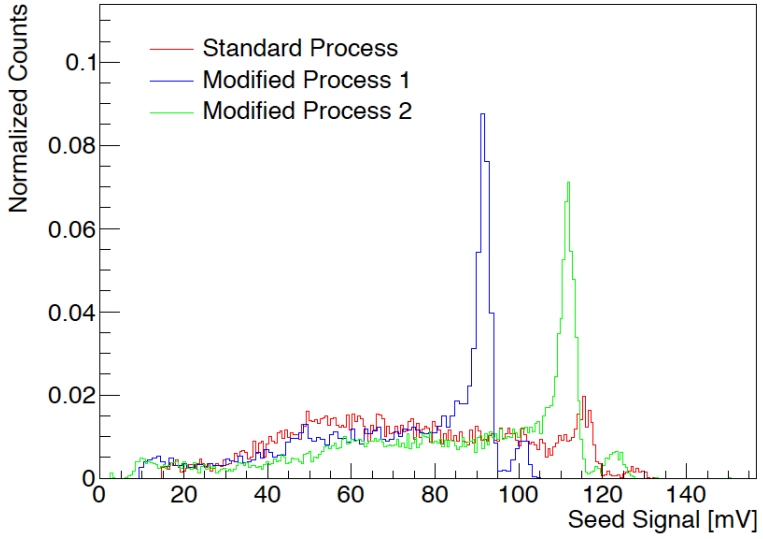
Signal and cluster distribution from a ^{55}Fe source for standard and modified process

Modified Process 1 = higher dose, Modified Process = lower dose

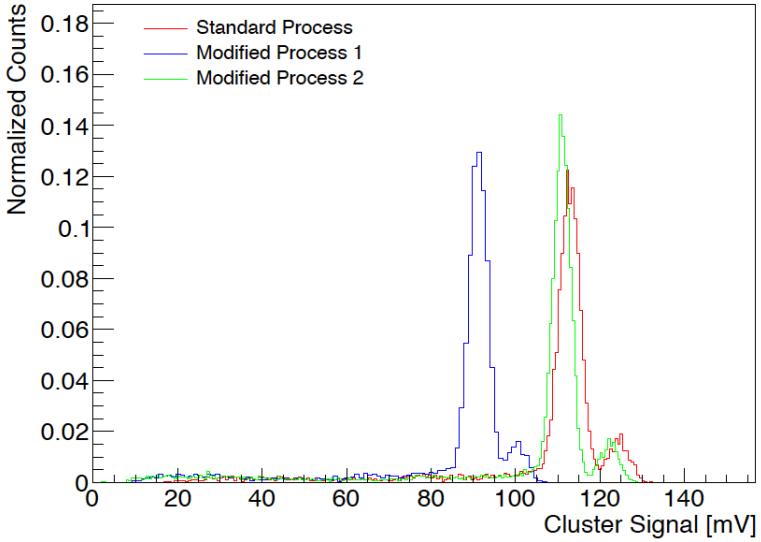
J. Van Hoorne et al., NSS 2016

Tests performed on investigator chip (same pixel as ALPIDE)

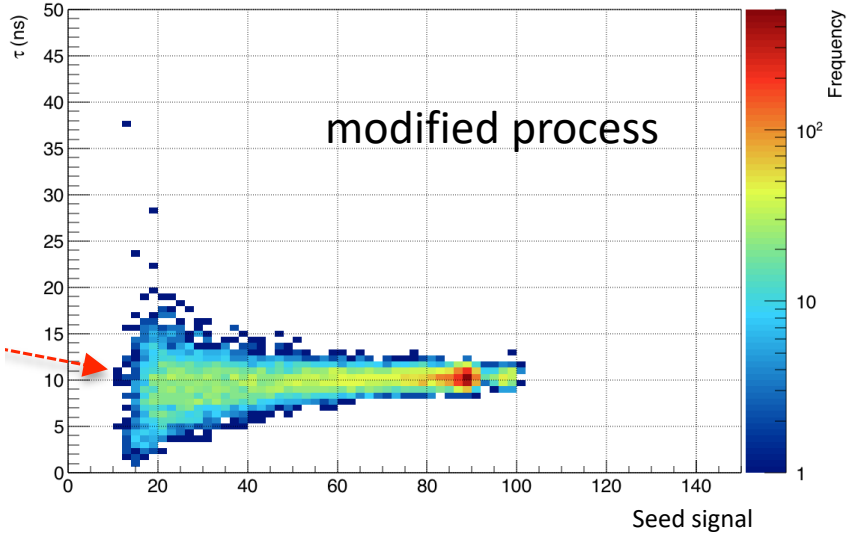
Pixel size: 28 x 28 μm^2, CE: 2 x 2 μm^2 centered in a 8 x 8 μm^2 opening, P-well & substrate @ -6V, CE @ 1V



(A) Seed signal



(B) cluster signal



Note: chip output buffer limits the rise time to 10ns

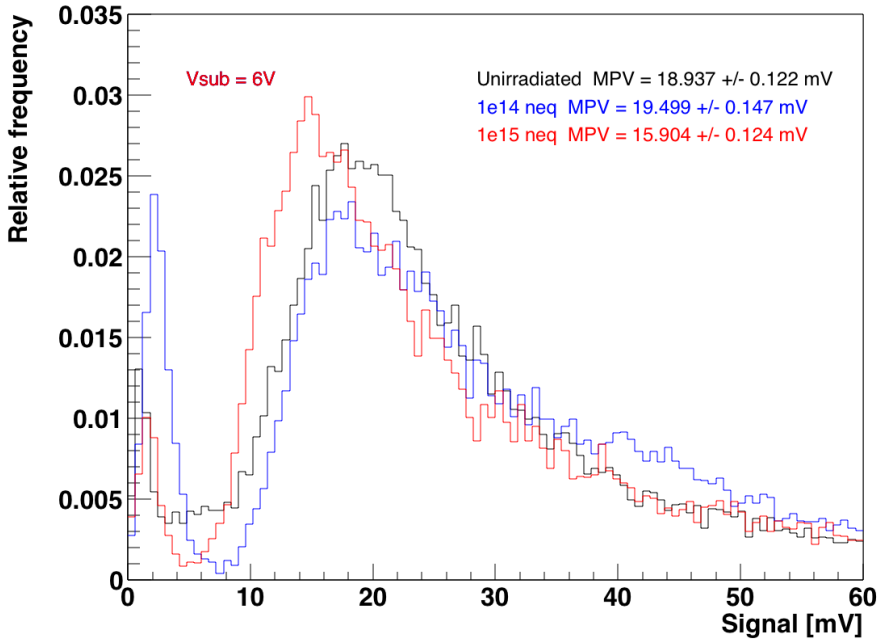
- For a lower dose (MP1) a no sensor capacitance penalty
- For modified process, larger fraction of single pixel clusters (see also fraction of signal within the peak in A)

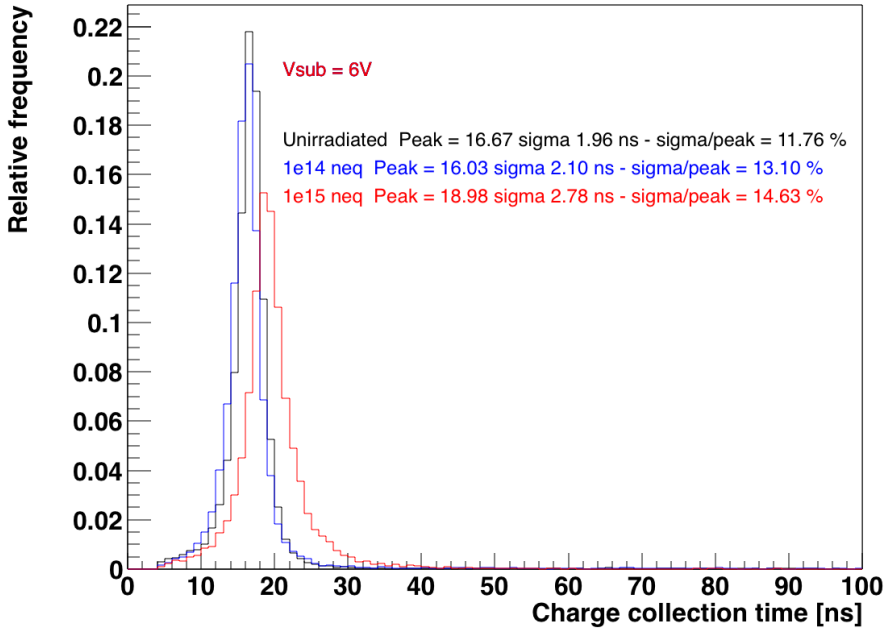
TJ modified process – charge collection time

^{90}Sr measurements on modified process samples (different setup, different pixel w.r.t. before)

- Non-irradiated
- 1 x 10^{14} 1MeV n_{eq}/cm^2 (NIEL) and 100krad (TID)
- 1 x 10^{15} 1MeV n_{eq}/cm^2 (NIEL) and 1Mrad (TID)

H. Pernegger et al 2017 JINST 12 P06008





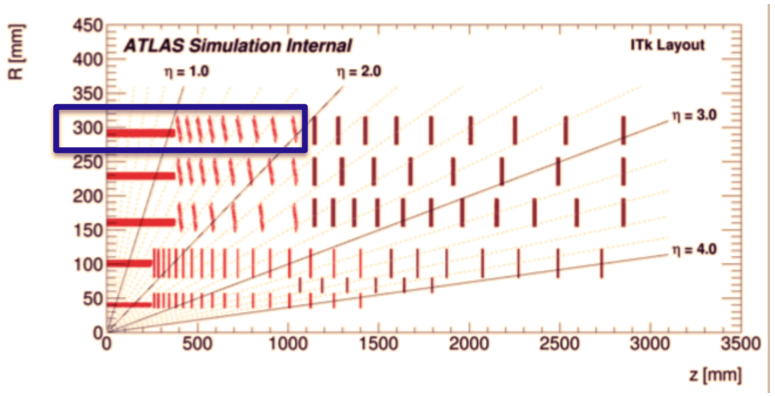
Tests performed on investigator chip (different pixel wrt to ALPIDE) *Note: chip output buffer limits the rise time to 10ns*

Pixel size: 50 x 50 μm^2, CE: 3 x 3 μm^2 centered in a 18 x 18 μm^2 opening, 25μm epi

New developments for ATLAS ITk L4

Outermost layer of ITk Pixel Barrel

- 2016 quad modules
- 3m^2



For 4000 fb^{-1}

- TID = 80 Mrad
- NIEL = 1.5 x 10^{15} n_{eq}/cm^2

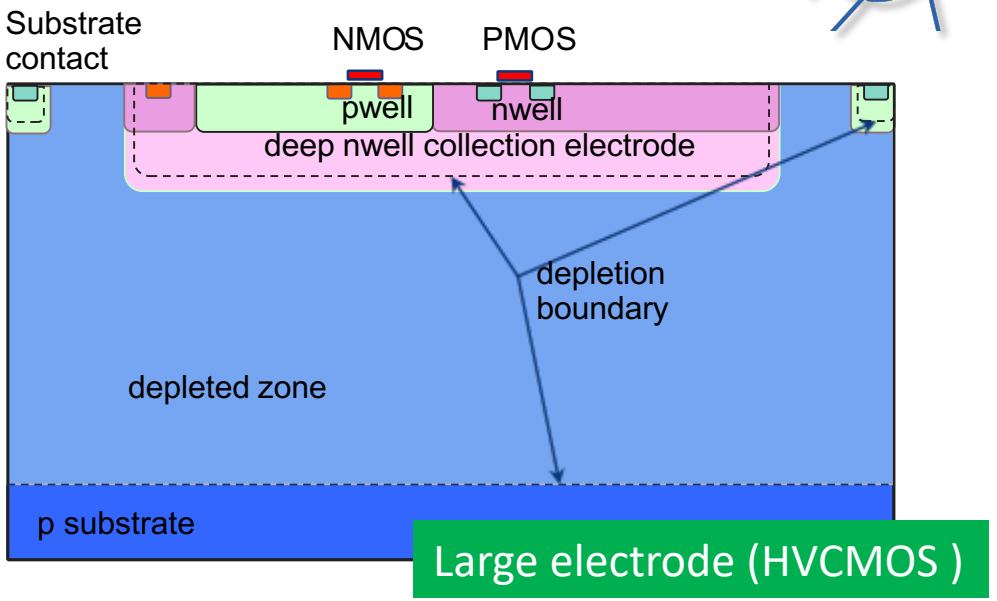
Monolithic CMOS sensors are considered as option for the outermost layer

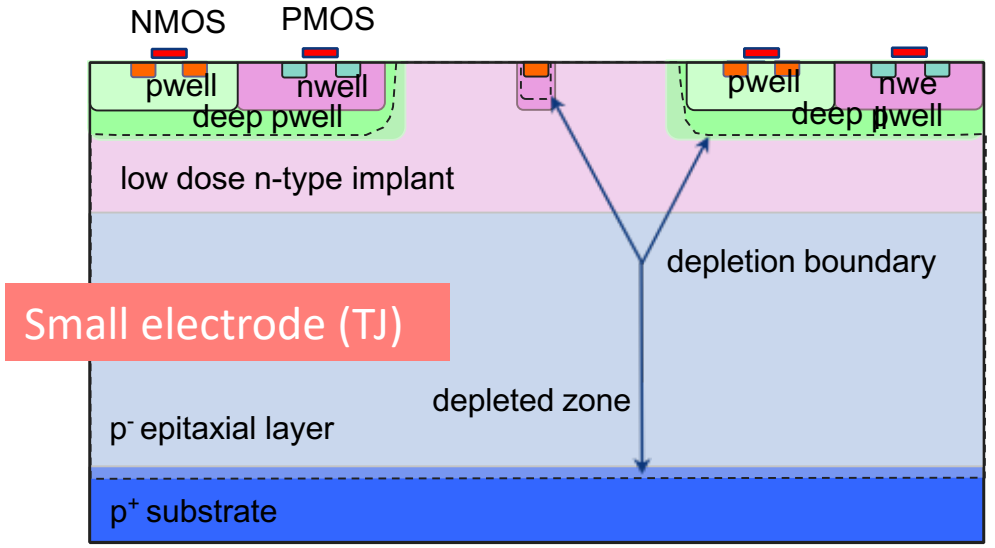
- Saves bump bonding for 45% of outer barrel system
- Cost reduction and reduce module assembly time

Three developments on three technologies

- Large CE: AMS ⇨ TSI (ATLASPix)
- Large CE: LFOUNDRY (Monopix) *Toko Hirono, Thu*
- Small electrode: TJ modified process (MALTA, Monopix)

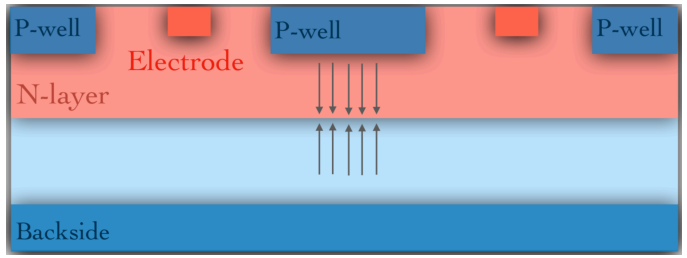
Enrico Junior Schioppa, Thu



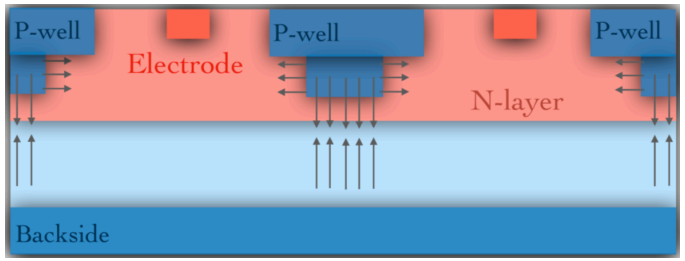


New developments for ATLAS ITk: small electrode TJ modified process

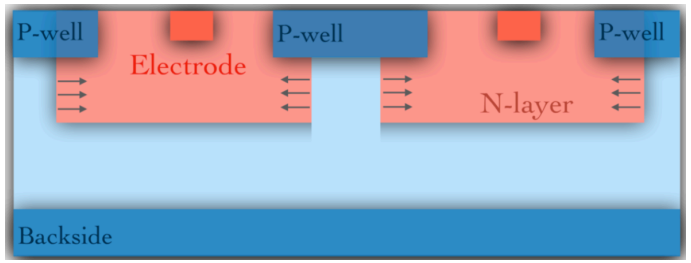
modified process (mp) – "standard"

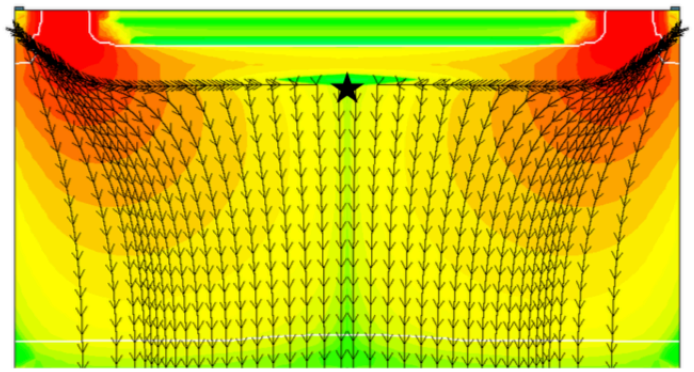


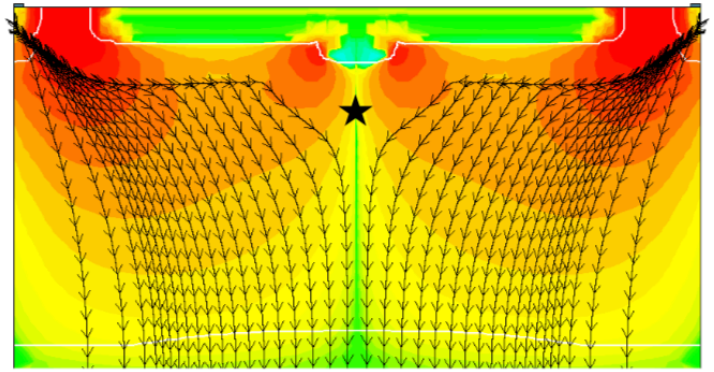
mp + additional p-implant

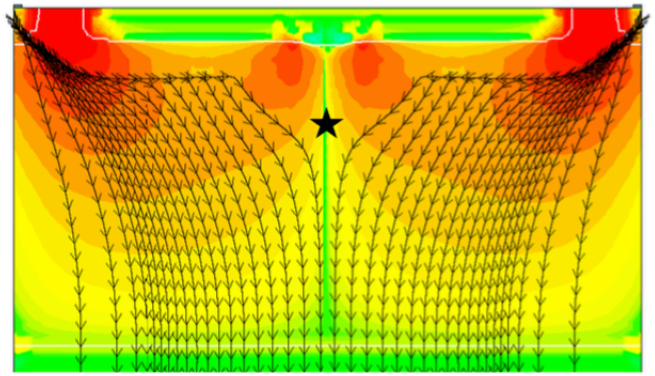


mp + gap in n-layer









Magdalena Munker (CERN), Pixel 2018 (Taipei - Dec 2018)

TJ modified process: E field minimum at pixel corners => charges pushed to the minimum before they propagate to CE

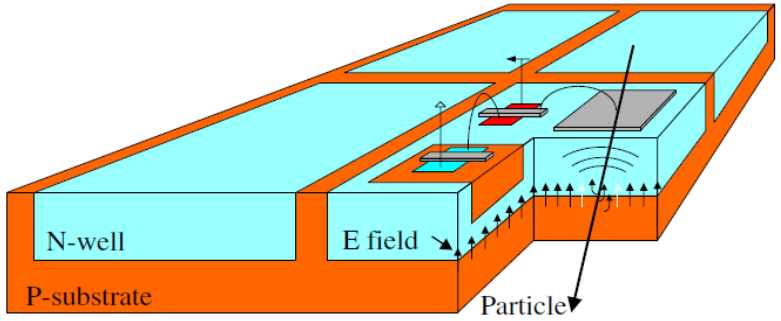
Additional p-implant or gap in n-layers: bend the field towards the CR, shorted drift path

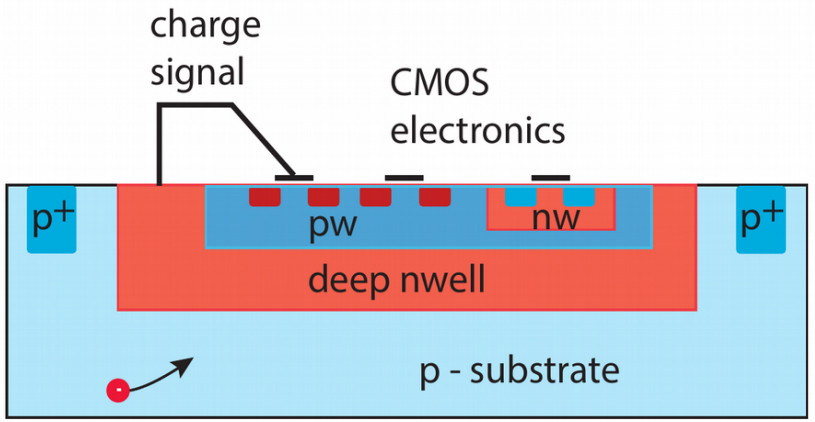
HV CMOS – developments for the Mu3e tracker and ATLAS

- Compatible with standard CMOS technology
- Triple well process on p-type substrate (20- 1000 Ω cm)
- Prototypes with var CMOS processes (AMS, TSI, LFounfry)

The HV CMOS Collaboration

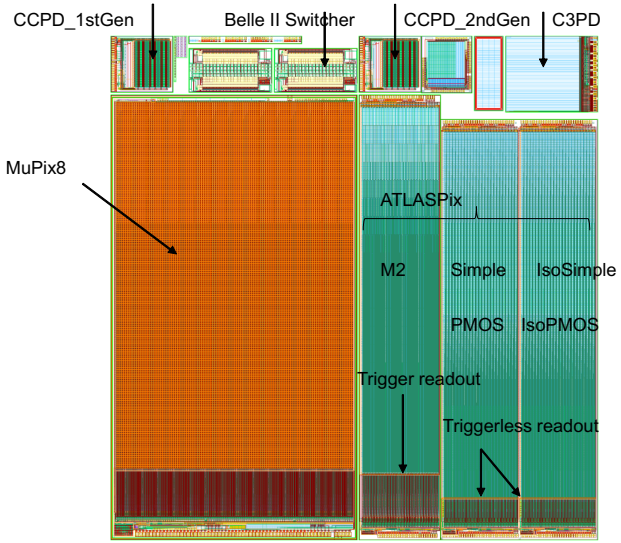
I. Peric et al., NIM A 582 (2007) 872





- The collection diode occupies a large part of the pixel
- Electronic circuits inside deep n-well
- HV O(60 – 120V) contacts at the top side
- MUPIX8 pixel: 80x81 μm^2

- Circuitry in the collection diode introduces additional sensor capacitance
- Keep pixel circuitry as simple as possible
- Confine digital circuitry at the periphery

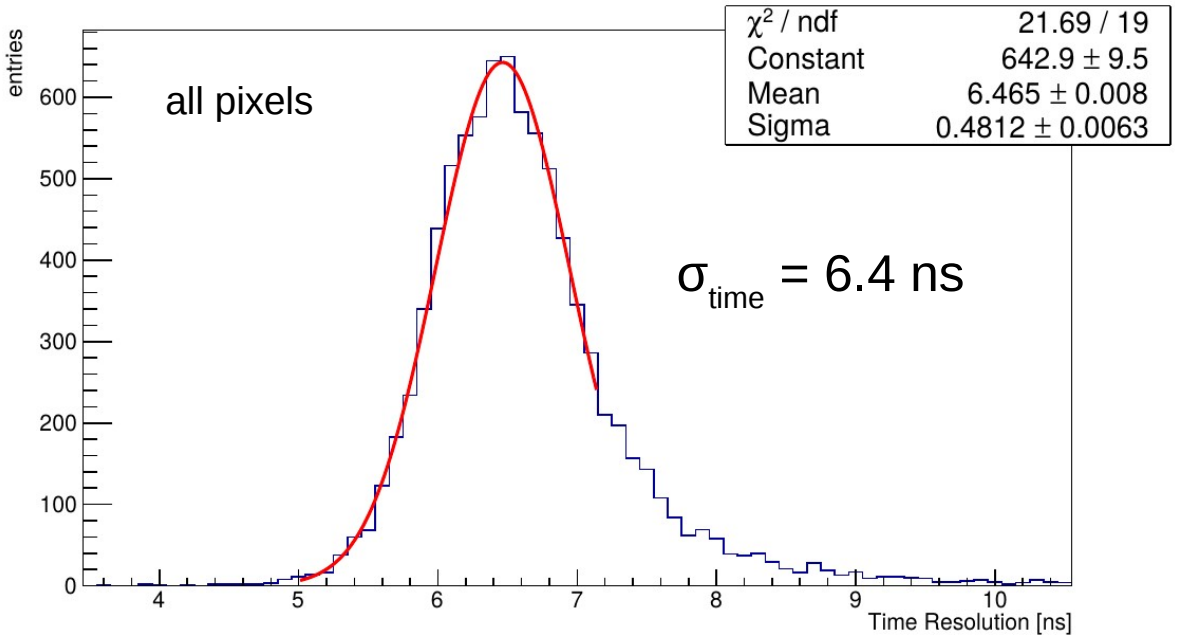


MuPix, ATLASPIX

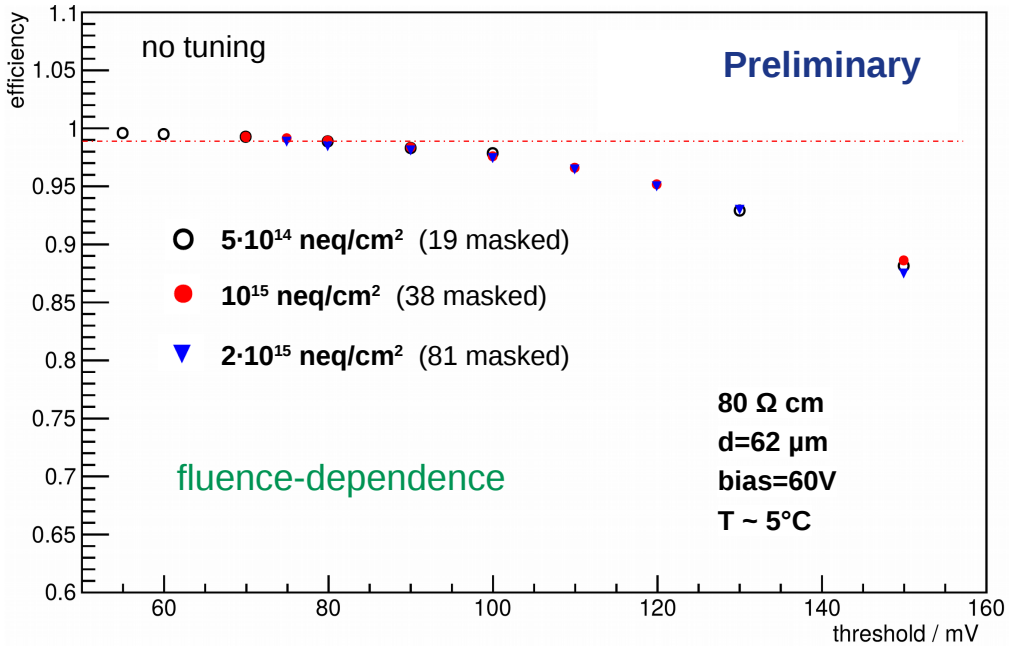
courtesy of I. Peric and A. Schoening

MUPIX8 - a full-scale HV-CMOS prototype for the Mu3e tracker

Time resolution with timewalk correction



Efficiency and fake hit rate

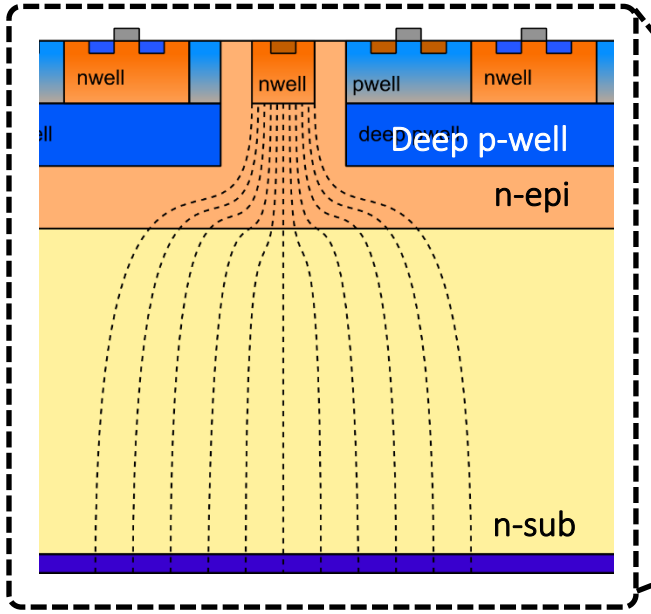


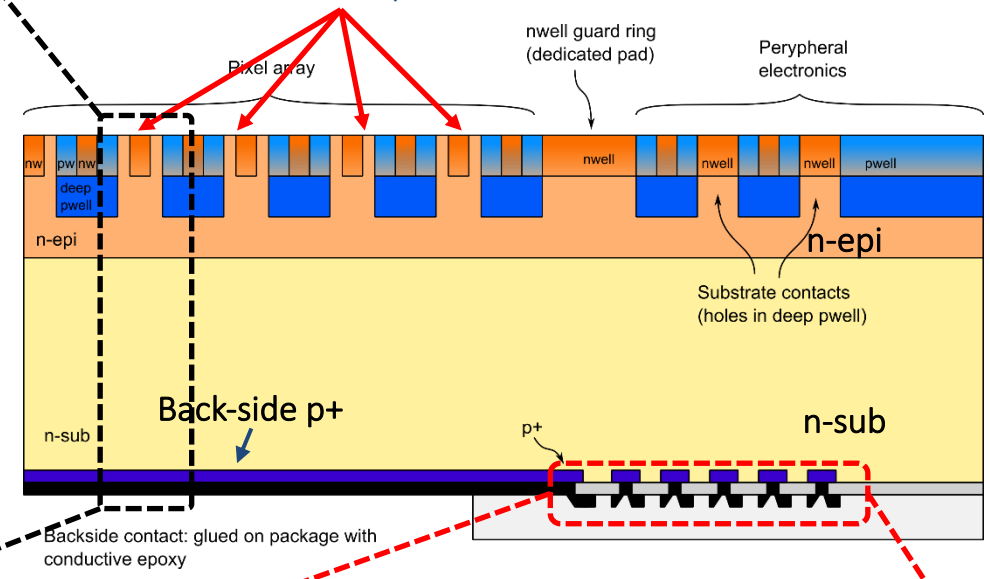
courtesy of I. Peric and A. Schoening

INFN projects SEED and ARCADIA: two phases of the same development

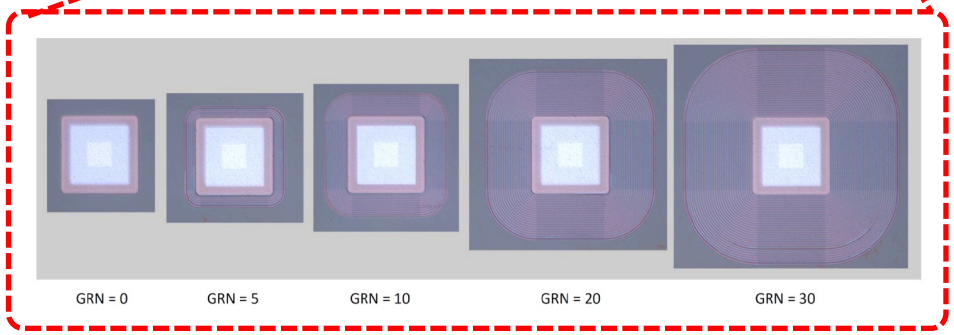
The SEED project successfully demonstrated a fully depleted, up to 300 µm thick MAPS sensor

- LFoundry 110nm CMOS process.
- Sensor nodes are n-type implantation (become insulated only with full substrate depletion)
- The high resistivity, floating zone n-type substrate is depleted by negative voltage at the p+ backside
- Deep pwell implantations allows implementing full CMOS gates





- Double-sided lithography was used for the processing of the backside layers (5 extra masks)
- The backside p+ implantation was done after thinning the substrate, and activated with laser annealing
- To avoid early breakdown, termination structures with floating guard rings have been added at the borders

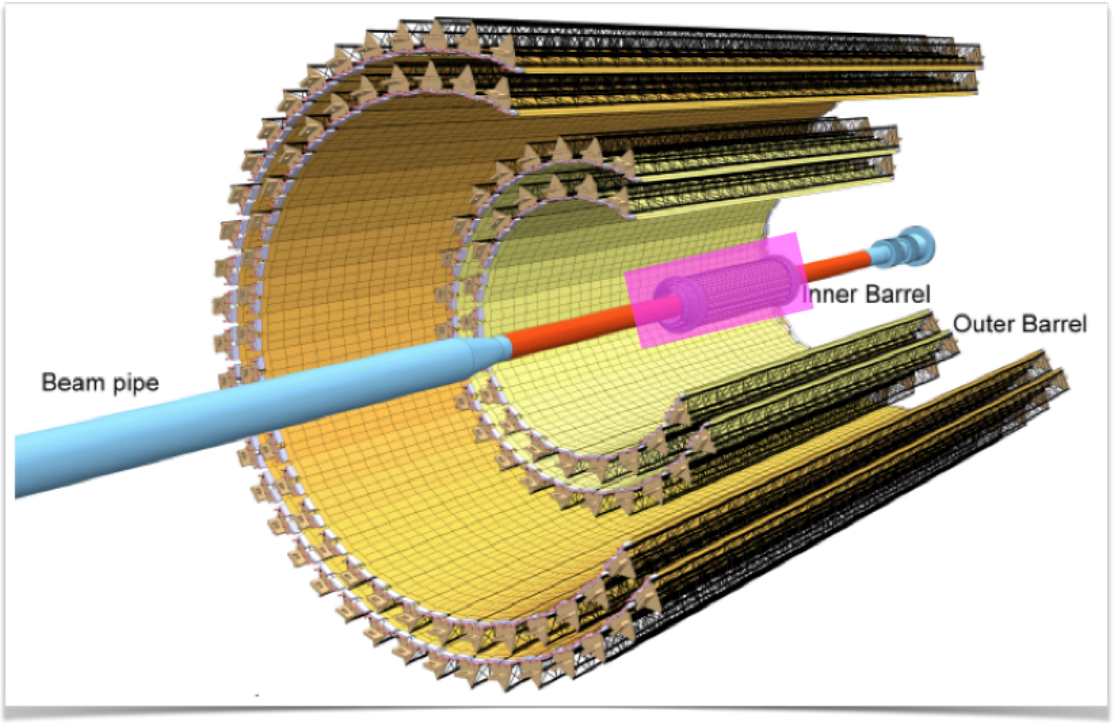


Different guard-rings on the backside diodes

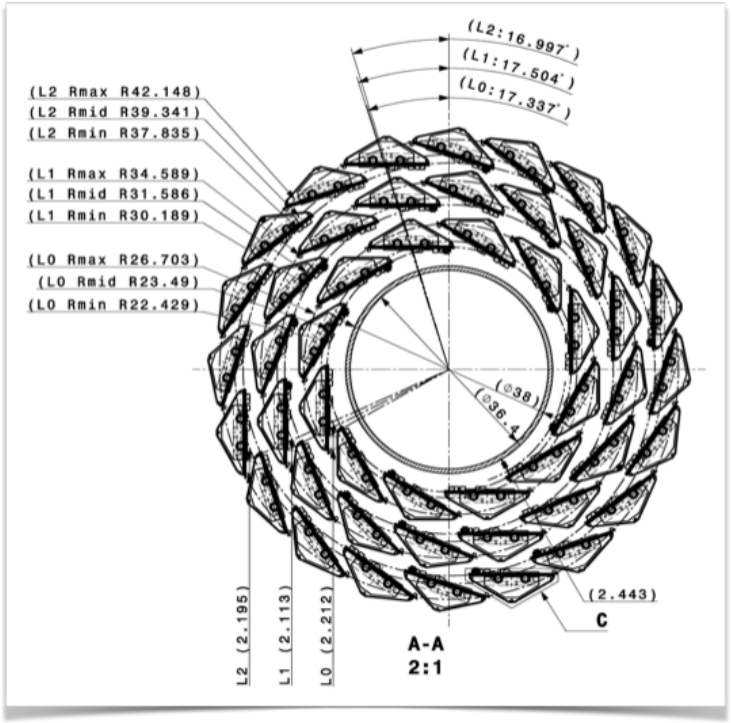
Novel Development
Ultra-thin and flexible

ALICE ITS Upgrade in LS2 ("ITS2")

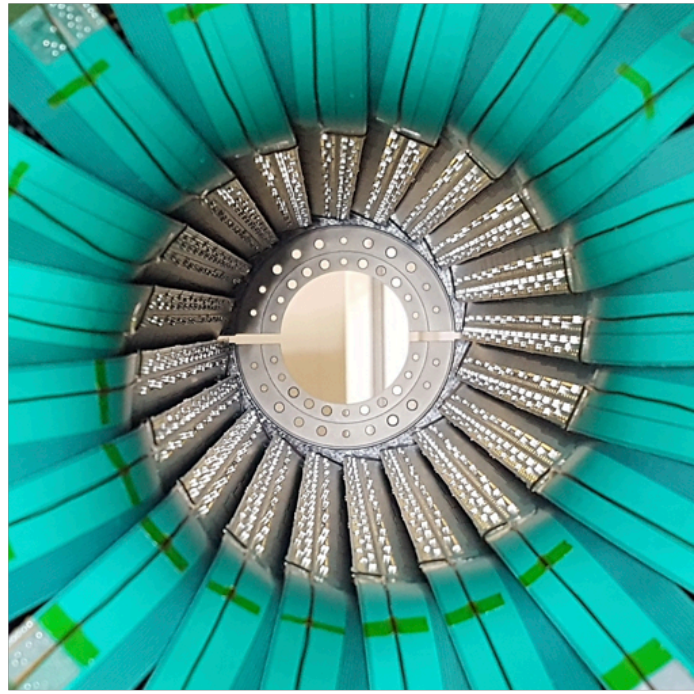
ITS2 layout



Inner barrel



Layer 2 (20 staves)

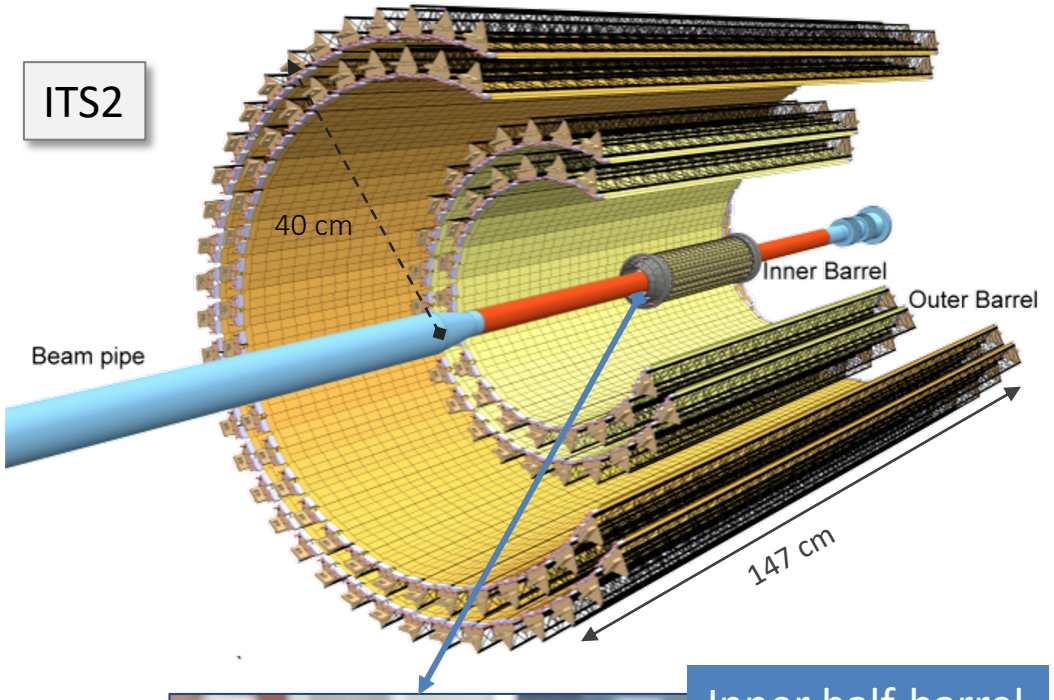


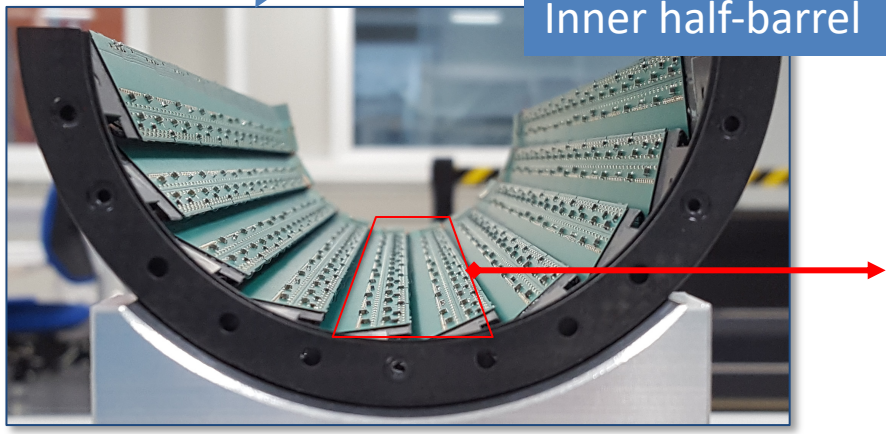
➡ already very good performance estimates for ITS2

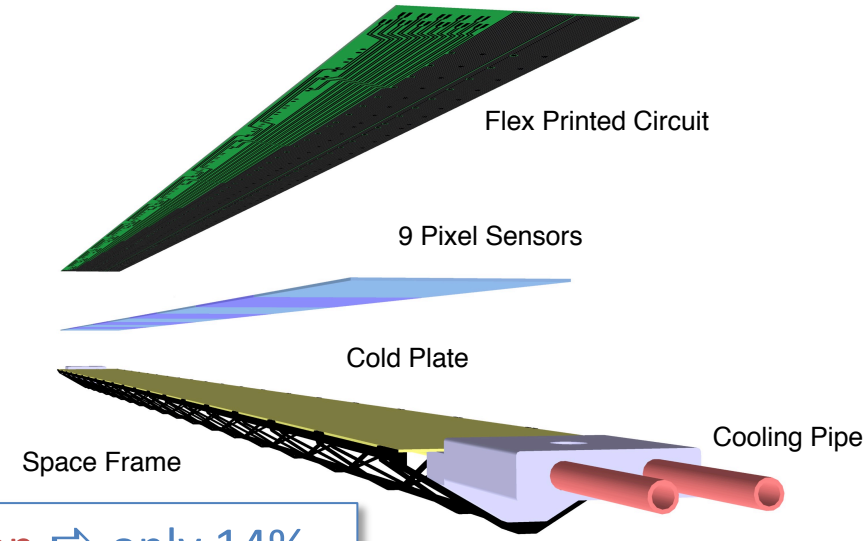
➡ still, further improvements for the measurements of heavy-flavour hadrons and low-mass di-leptons possible

key questions: ➡ Can we get even closer? ➡ Can we get even lighter?

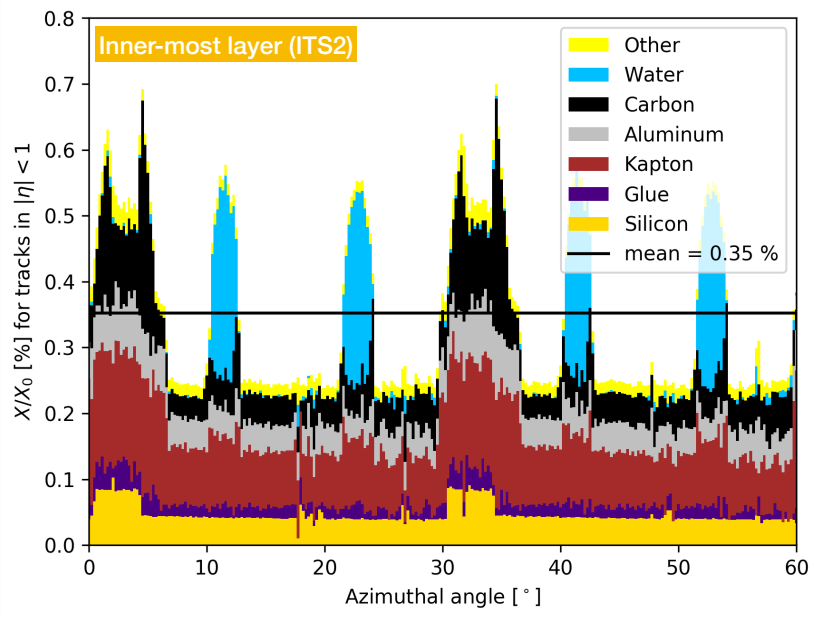
ITS2 – Material Budget



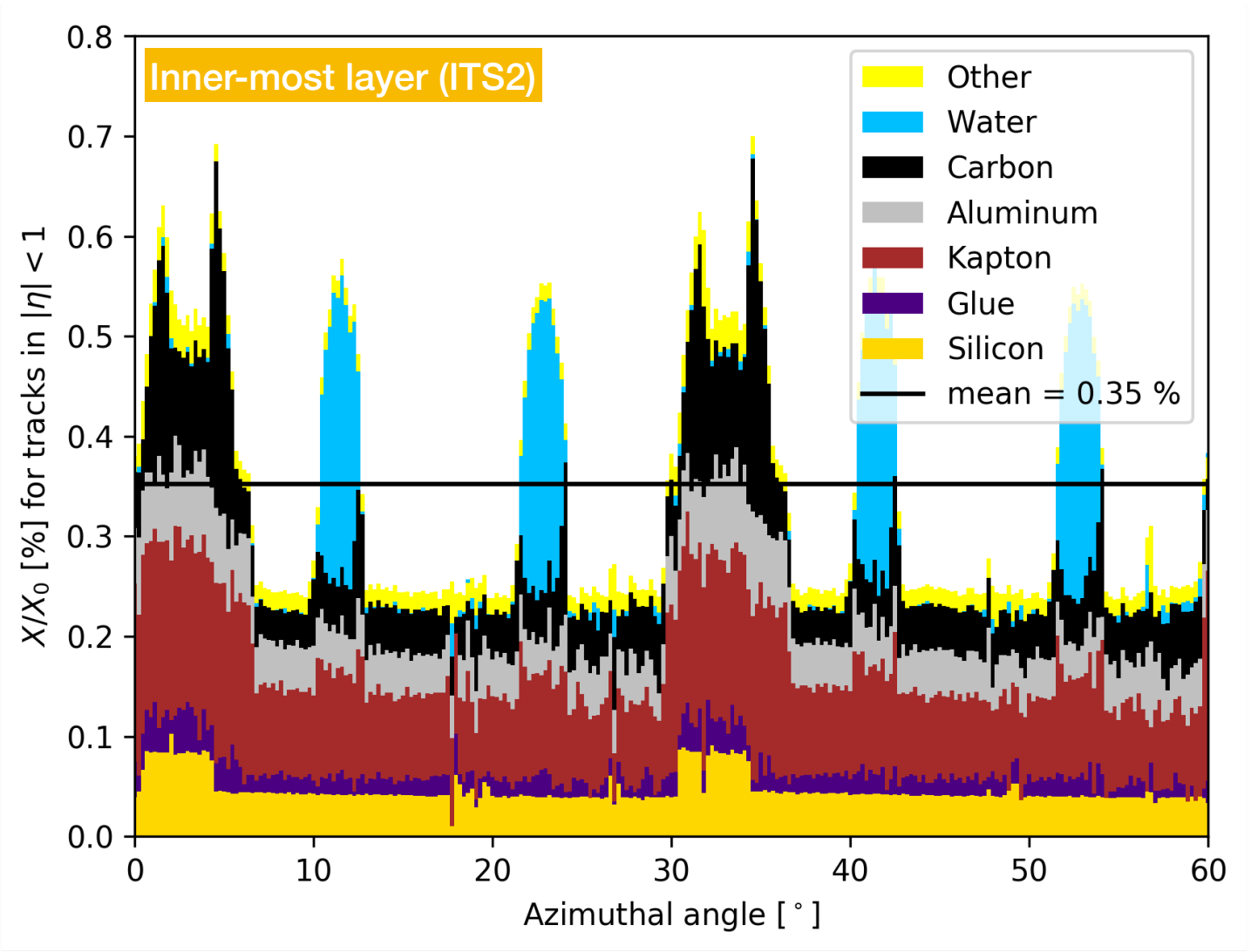




Silicon ⇨ only 14%



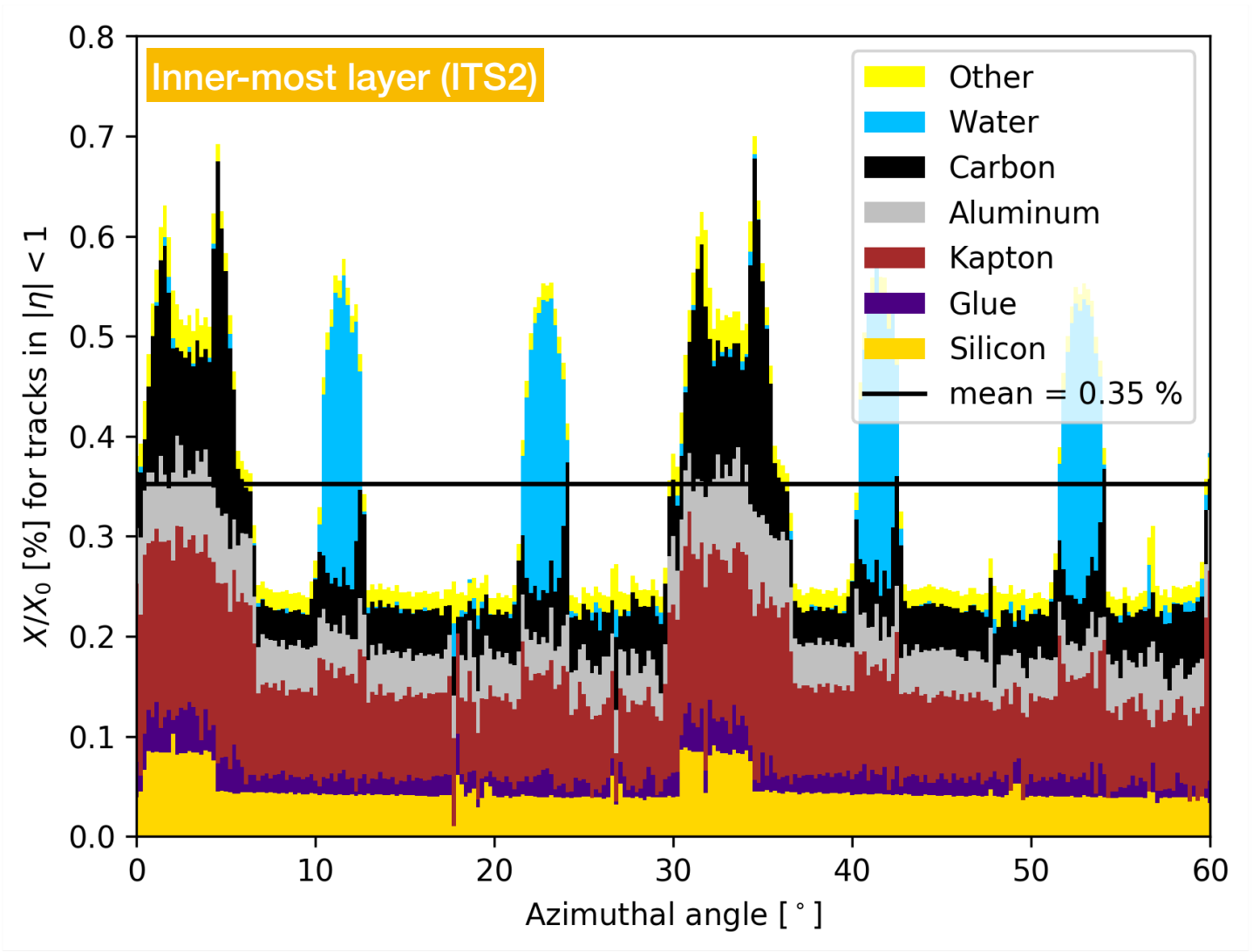
ITS2 Material Budget



⇨ Silicon only 1/7th of total material

⇨ irregularities due to overlaps + support/cooling

ITS2 Material Budget



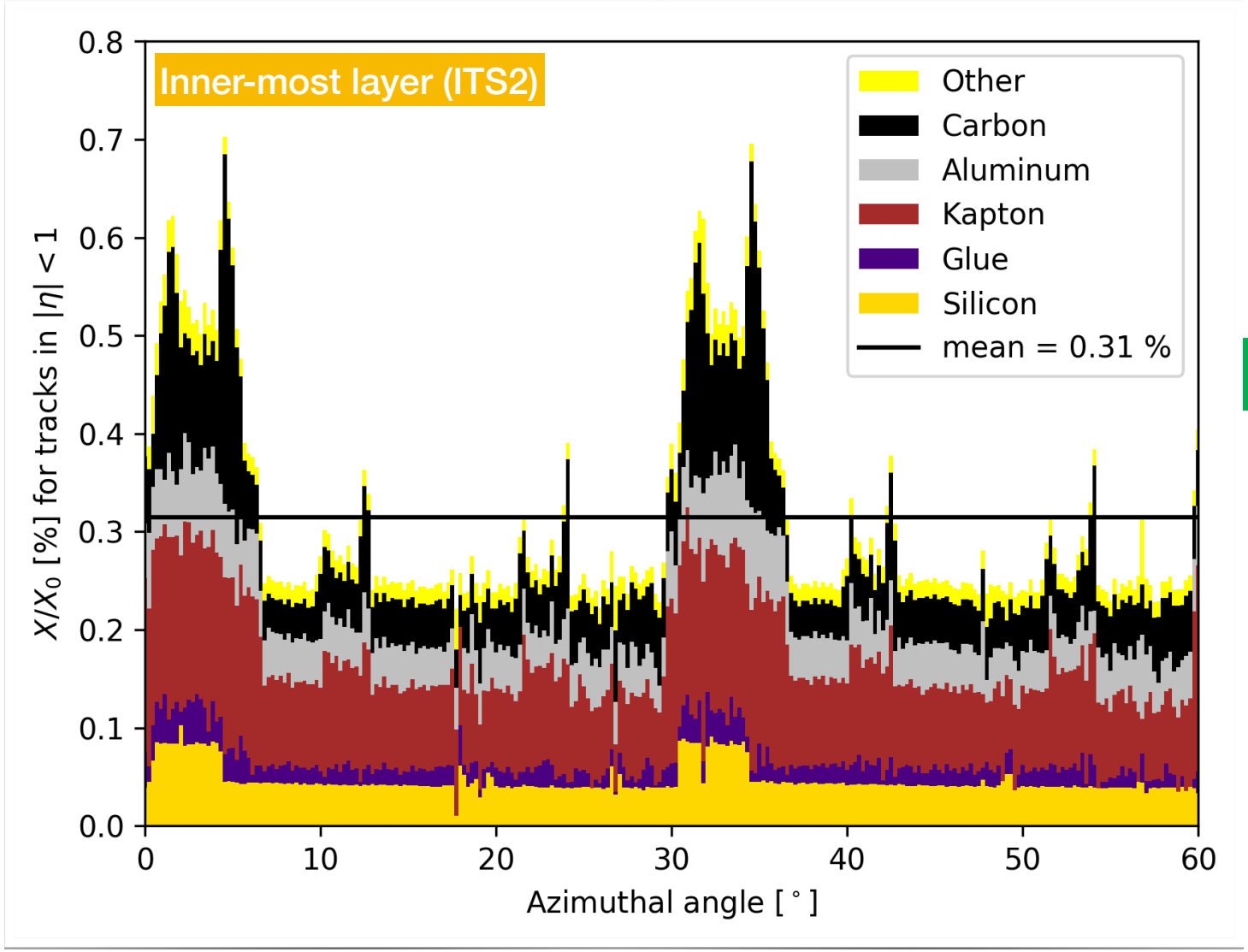
⇨ Silicon only 1/7th of total material

⇨ irregularities due to overlaps + support/cooling

⇨ Remove water cooling

⇨ Possible by reducing power in fiducial volume to < 20mW/cm^2

ITS2 Material Budget



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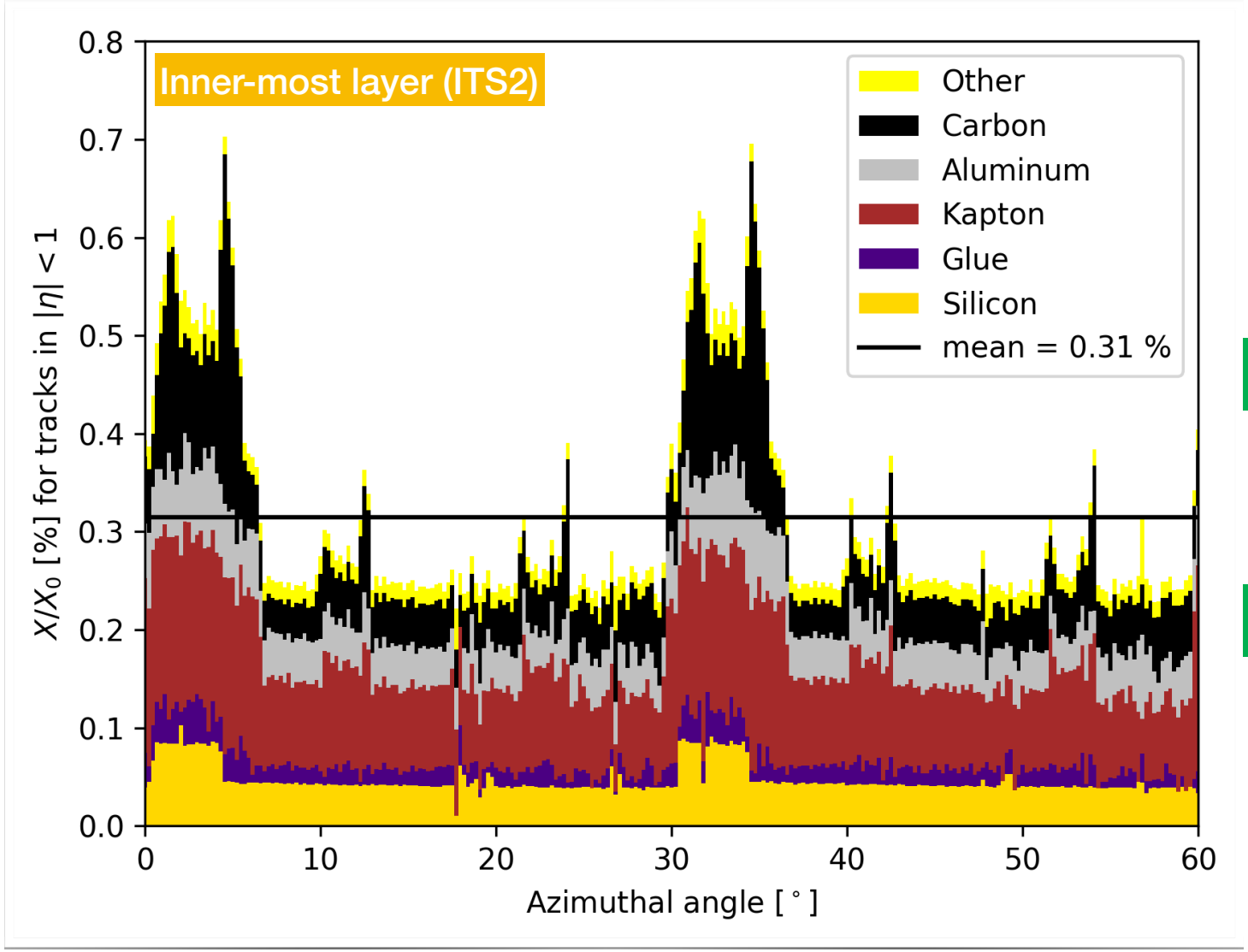

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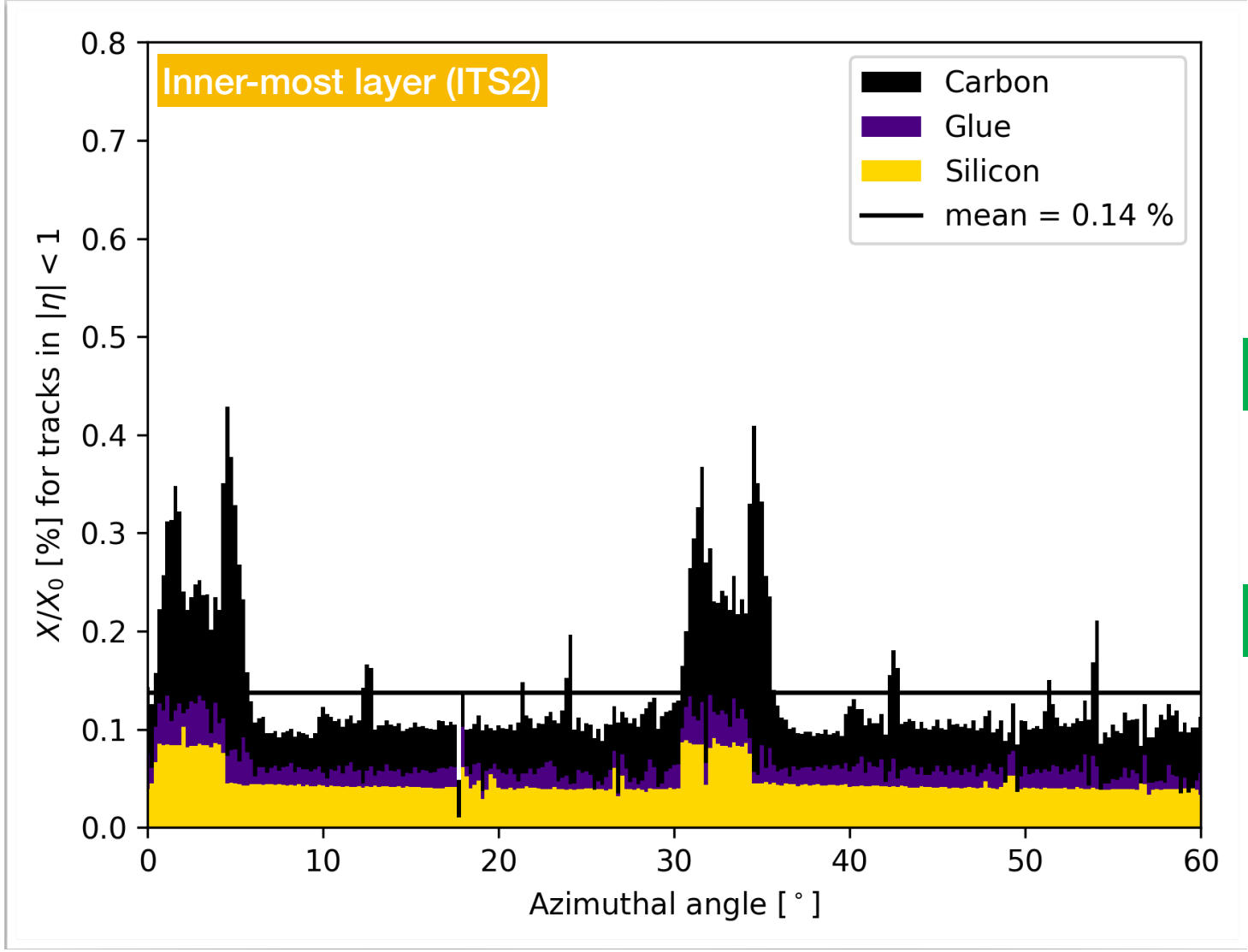
⇨ Remove power and data bus

⇨ Possible by making the sensor chip as long as the detector

ITS2 Material Budget



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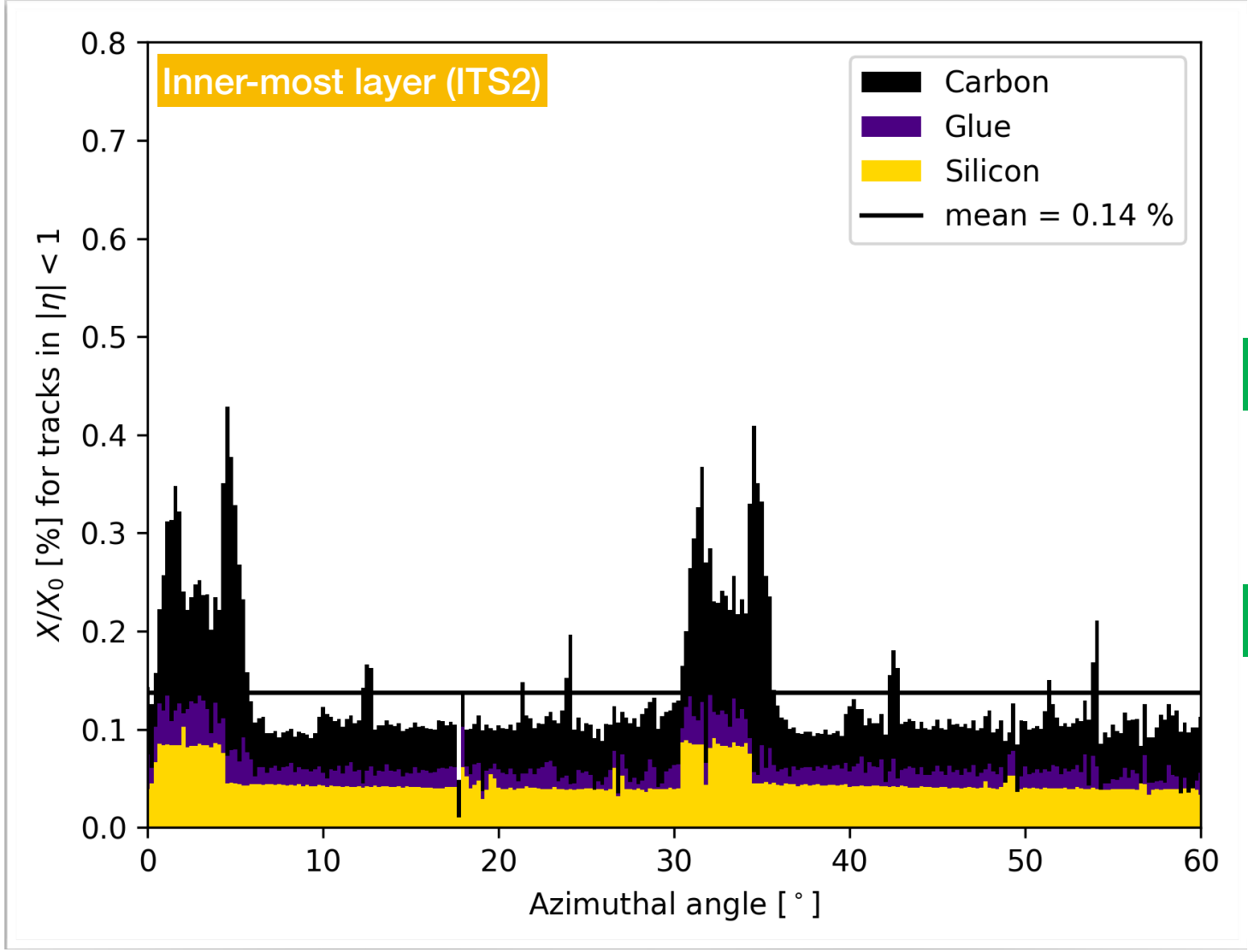
ITS2 Material Budget



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⇨ irregularities due to overlaps + support/cooling

⇨ Remove water cooling

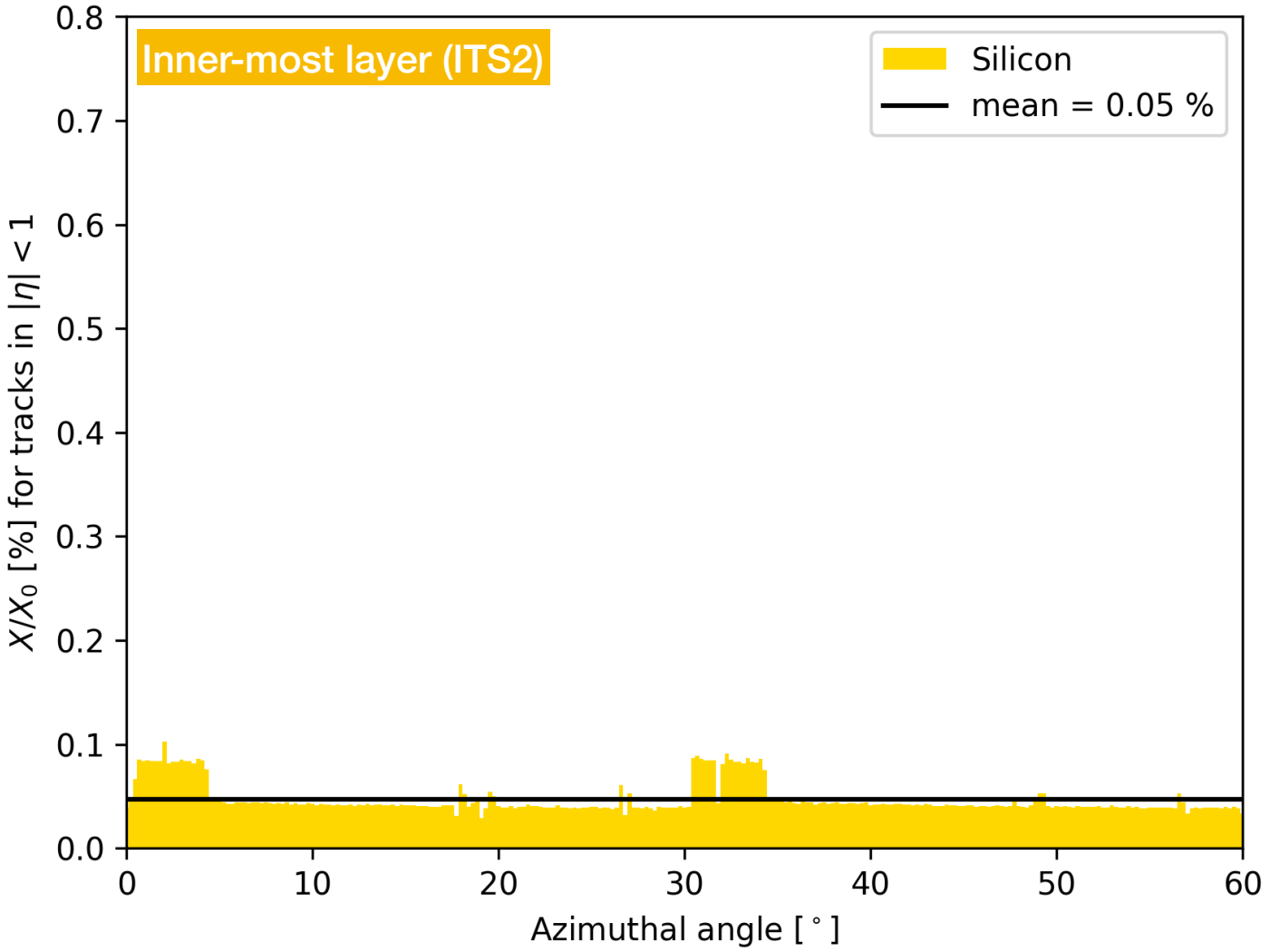
⇨ Possible by reducing power in fiducial volume to < 20mW/cm^2

⇨ Remove power and data bus

⇨ Possible by making the sensor chip as long as the detector

⇨ Move mechanical support outside acceptance

ITS2 Material Budget



⇨ Silicon only 1/7th of total material

⇨ irregularities due to overlaps + support/cooling

⇨ Remove water cooling

⇨ Possible by reducing power in fiducial volume to < 20mW/cm^2

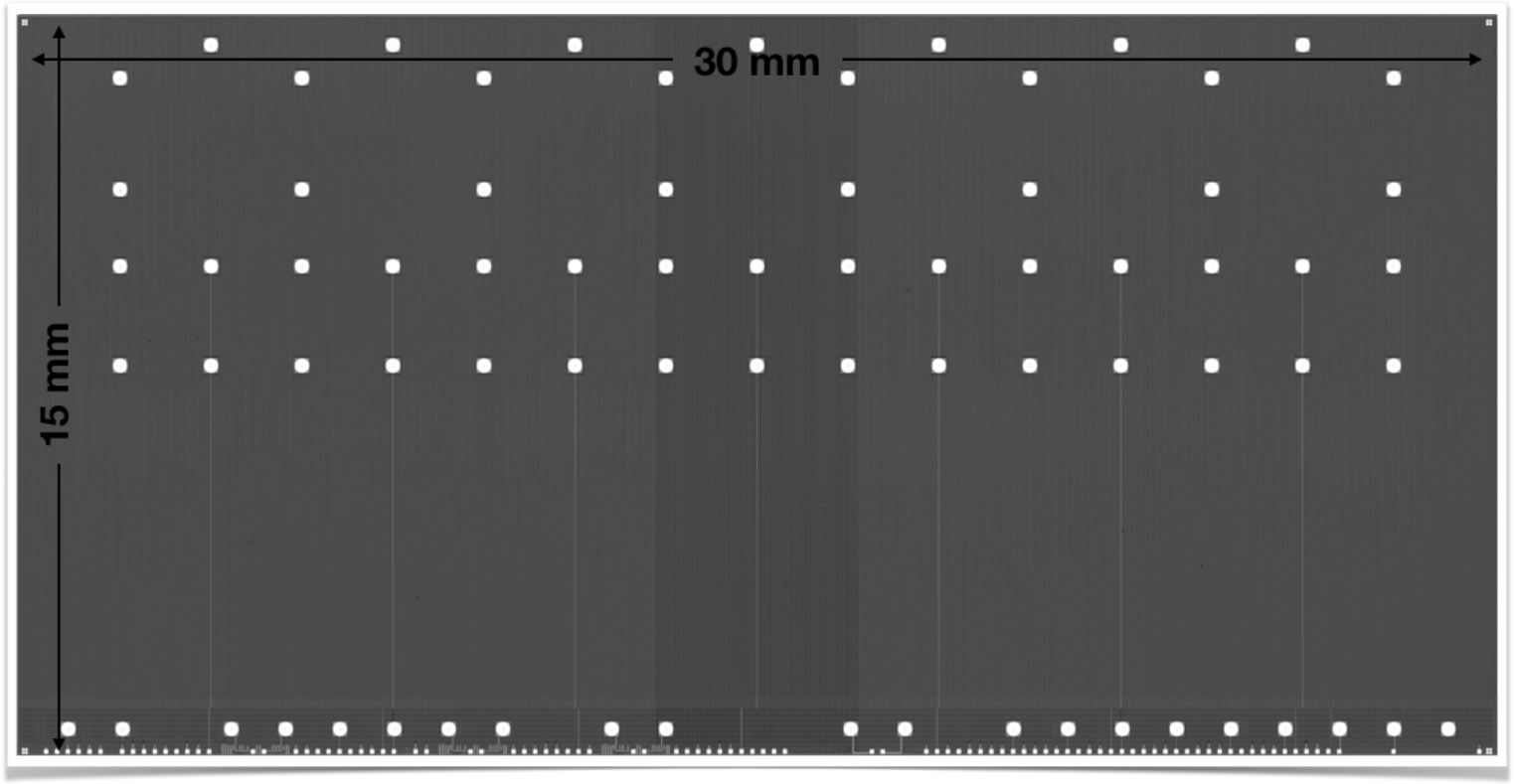
⇨ Remove power and data bus

⇨ Possible by making the sensor chip as long as the detector

⇨ Move mechanical support outside acceptance

Power Consumption

ALPIDE

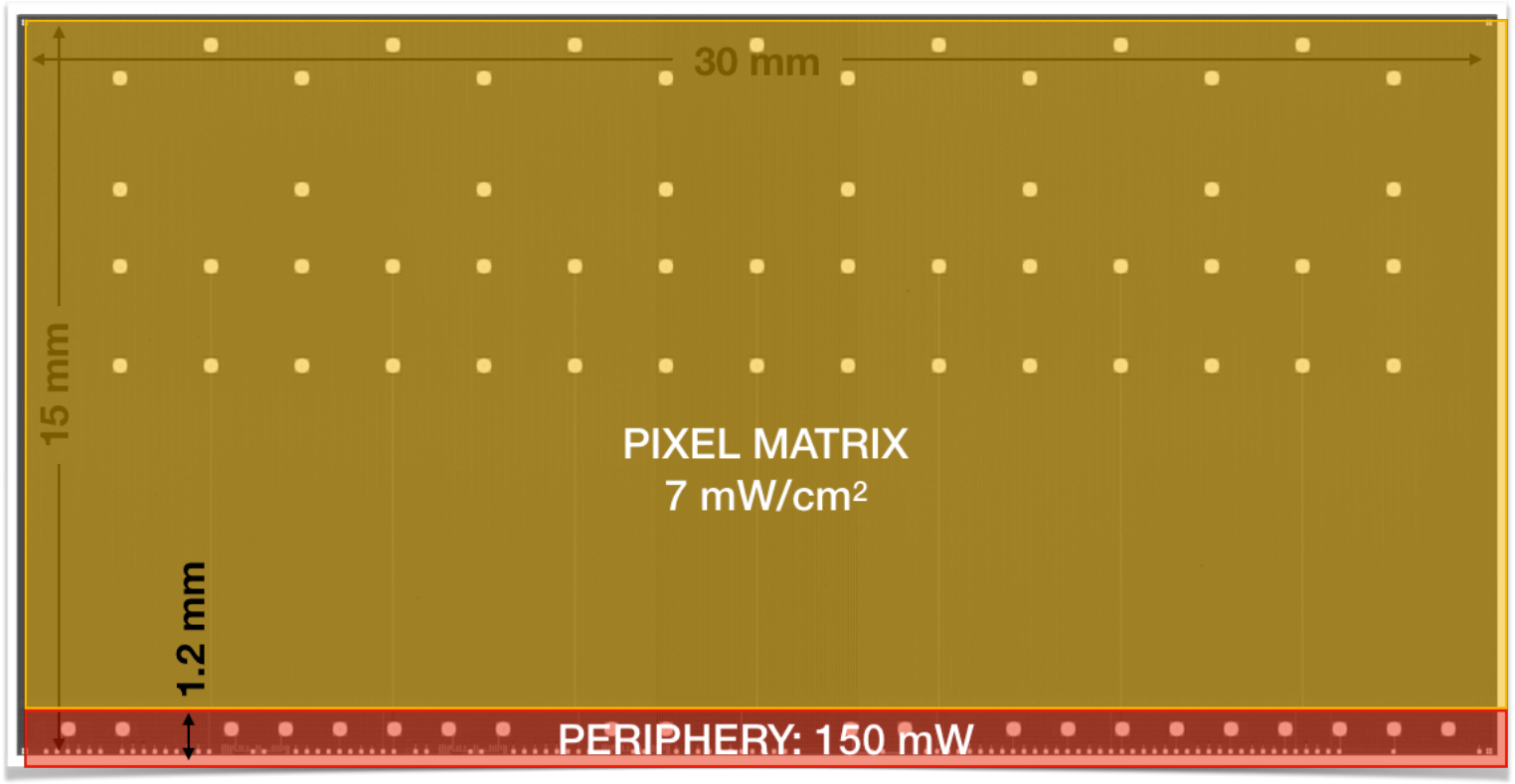


➪ Air cooling possible as of ~20mW/cm^2

➪ ALPIDE already close: ≤ 40mW/cm^2

Power Consumption

ALPIDE



⇨ Air cooling possible as of ~20mW/cm²

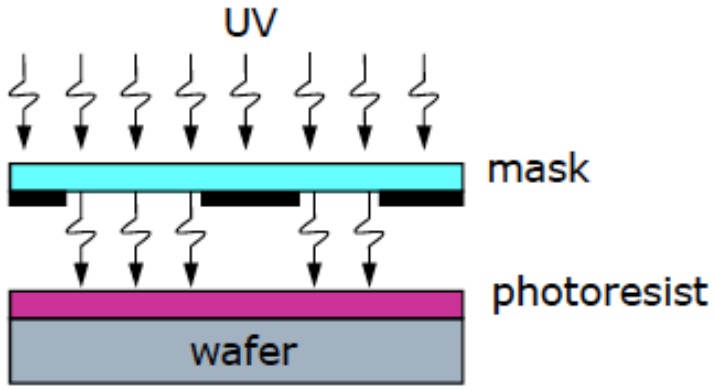
⇨ ALPIDE already close: ≤ 40mW/cm²

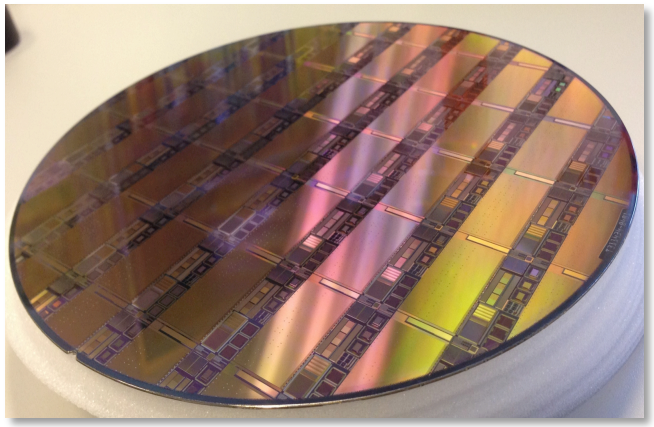
⇨ Actually sufficiently low if periphery outside fiducial volume

CMOS Active Pixel Sensor – wafer-scale integration

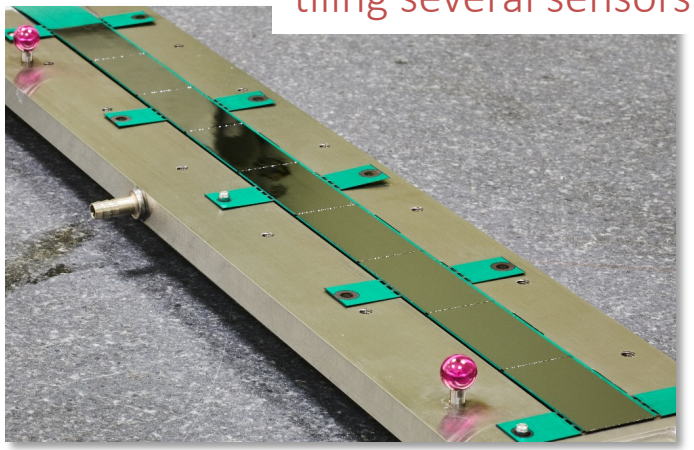
Photolithographic process defines wafer reticles size ⇨ Typical field of view O(2 x 2 cm^2)

Reticle is stepped across the wafers to create multiple identical images of the circuit(s)





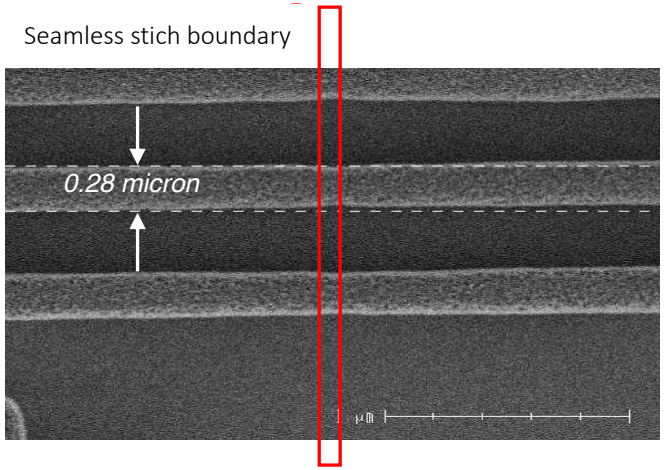
tiling several sensors

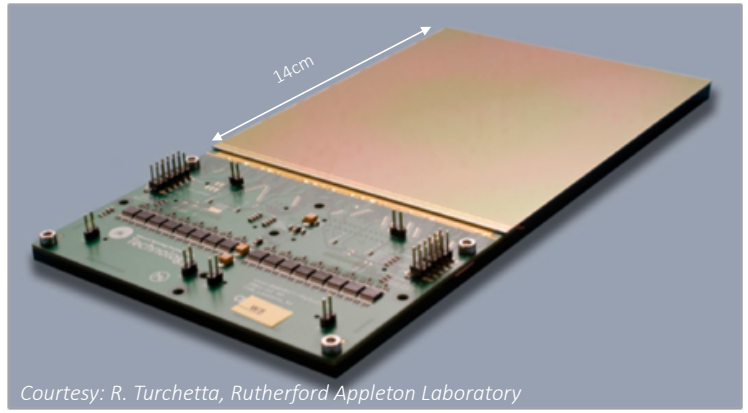


A stepping process called "stitching" allows building sensors of arbitrary size, the only limit being the size of the wafer.

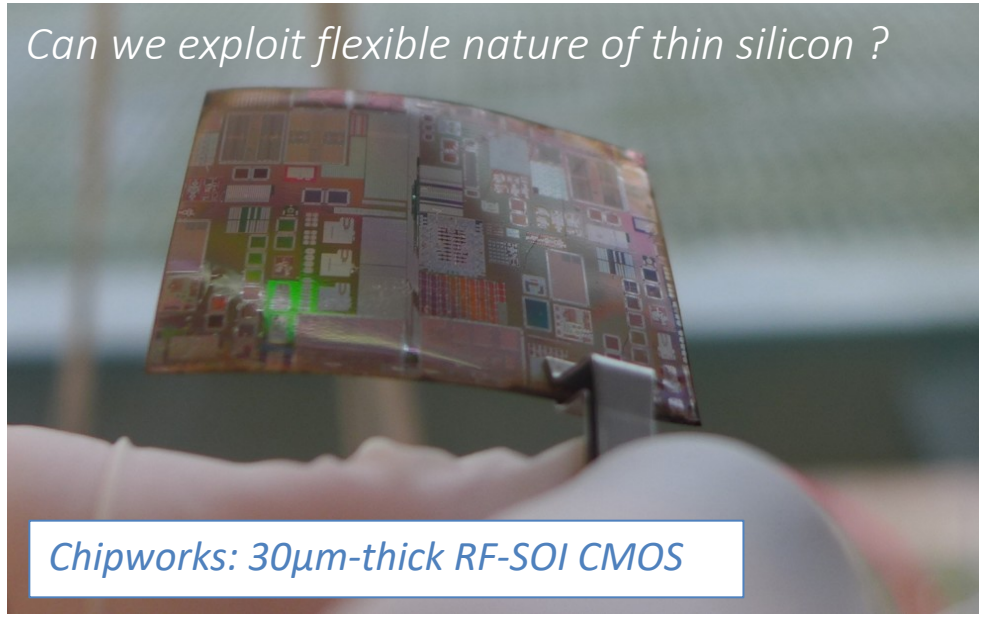
- Reticle made of blocks
- Printing only individual blocks at each step with a tiny well-defined overlap

These days, stitching is widely applied in the digital imaging industry (e.g. large flat panels for medical and dental X-rays)





Ultra-thin curved silicon chips

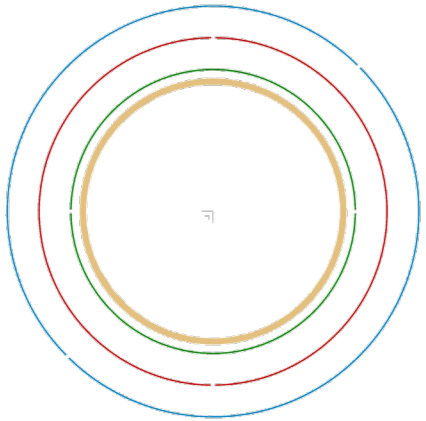


Ultra-thin chip (<50 um): flexible with good stability

Die type	Front/back side	Ground/polished/plasma	Bumps	Die thickness (µm)	CDS (MPa)	Weibull modulus	MDS (MPa)	r_{min} (mm)
Blank	Front	Ground	No	15–20	1263	7.42	691	2.46
Blank	Back	Ground	No	15–20	575	5.48	221	7.72
IZM28	Front	Ground	Yes	15–20	1032	9.44	636	2.70
IZM28	Back	Ground	Yes	15–20	494	2.04	52	32.7
Blank	Back	Polished	No	25–35	1044	4.17	334	7.72
IZM28	Back	Polished	Yes	25–35	482	2.98	107	24.3
Blank	Back	Plasma	Yes	18–22	2340	12.6	679	2.50
IZM28	Front	Plasma	Yes	18–22	1207	2.64	833	2.05
IZM28	Back	Plasma	Yes	18–22	2139	3.74	362	4.72

van den Ende DA et al. *Mechanical and electrical properties of ultra-thin chips and flexible electronics assemblies during bending*. Mircoelectron reliab (2014), http://dx.doi.org/10.1016/j.microrel.2014.07.125

Geometrical Parameters of ITS3



New Beampipe: r ≈ 16mm , ΔR = 0.5mm

L0: r ≈ 18mm , L1: r ≈ 24mm, L2: r ≈ 30 mm

Beam pipe thickness: 500µm (0.14% X_0)

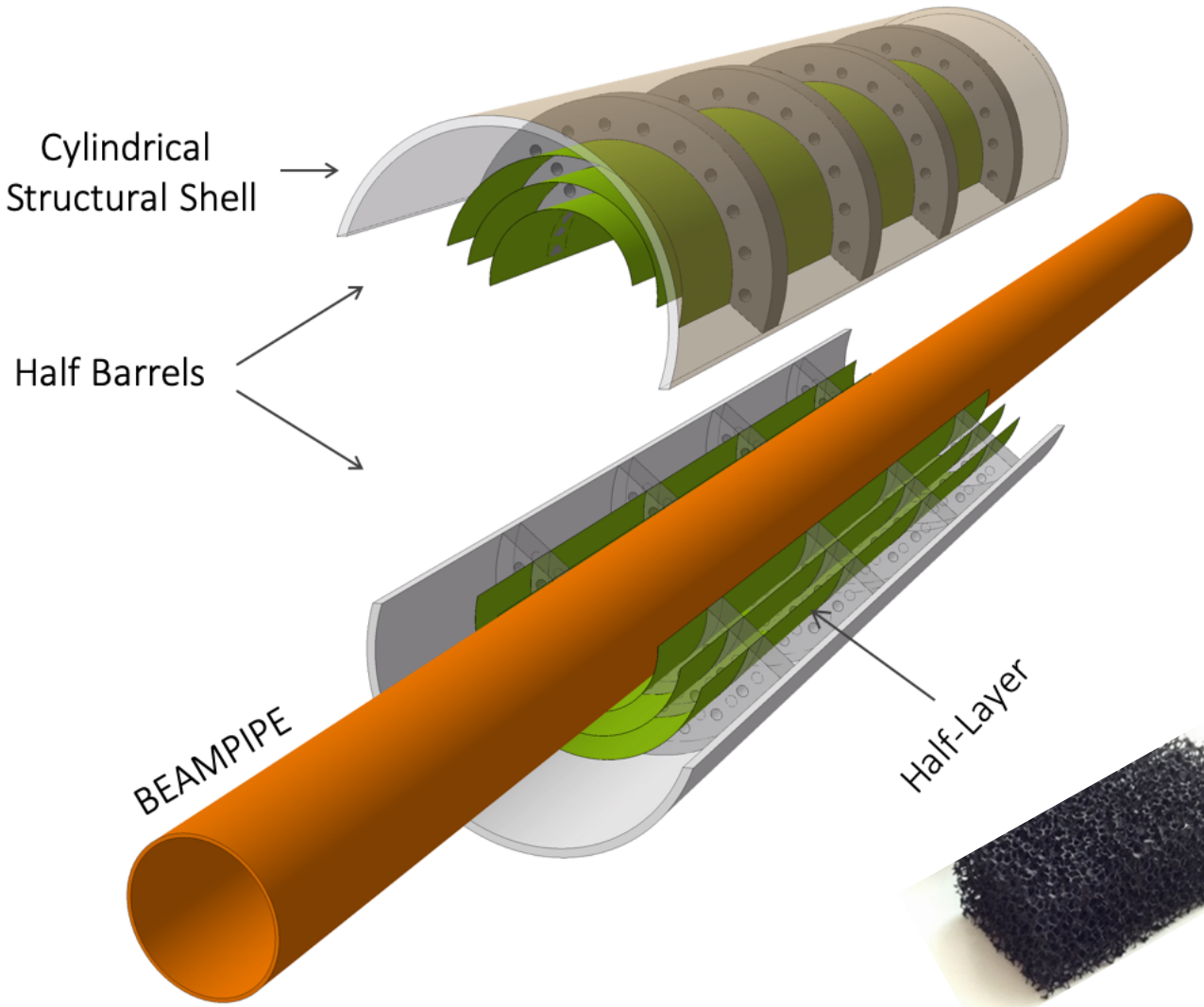
Sensor thickness: 20 – 40µm (0.03 - 0.05% X_0)

Beampipe inner/outer radius (mm)		16.0/16.5	
IB Layer parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	270	270	270
Pseudo-rapidity coverage[a]	±2.5	±2.3	±2.0
Active area (cm^2)	305	408	508
Pixel sensors dimensions (mm^2)	280×56.5	280×75.5	280×94
Number of pixel sensors / layer		2	
Pixel size (μm^2)		$O(15 \times 15)$[b]	

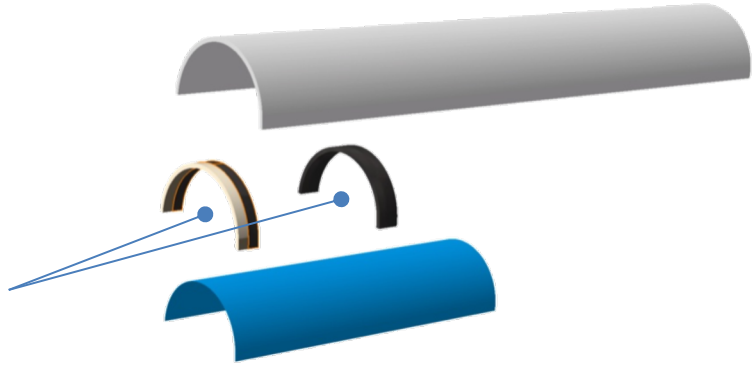
[a] The pseudorapidity coverage of the detector layers refers to tracks originating from a collision at the nominal interaction point ($z = 0$).

[b] For the fallback solution the pixel size is about a factor two larger ($O(30 \times 30)\ \mu m^2$).

ITS3 Mechanical Layout



Layers supported by high-thermal conductive carbon foam (half-ring)



Open cell carbon foam

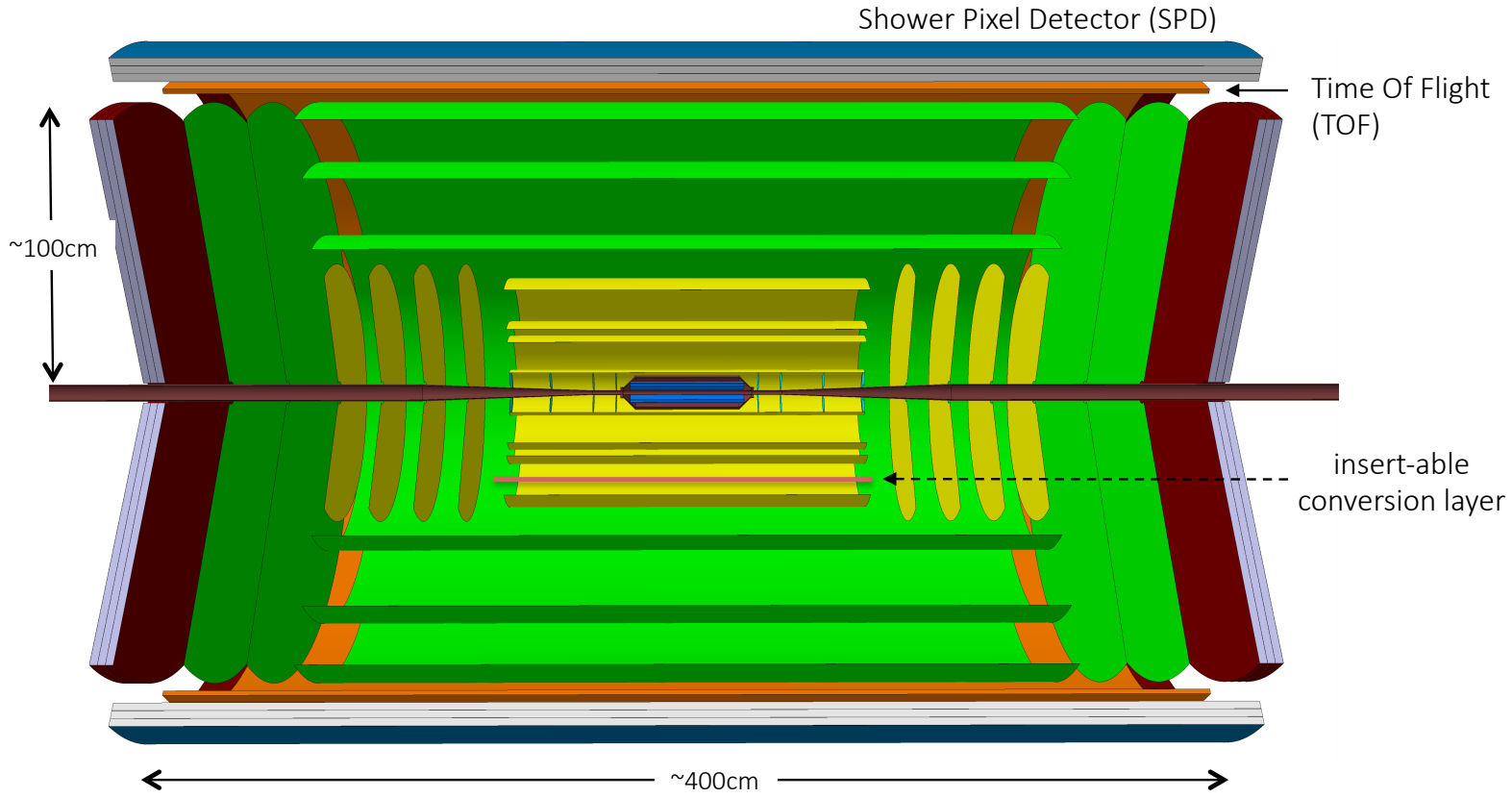
A Next Generation HI Experiment at the LHC ("all-silicon" detector)

Tracker: ~10 tracking barrel layers (blue, yellow and green) based on CMOS sensors

Particle ID:

- TOF with outer silicon layers (orange)
- Shower Pixel Detector (outermost blue layer)

Extended rapidity coverage: **up to 8 rapidity units**



Magnetic Field
- B = 0.5 or 1 T

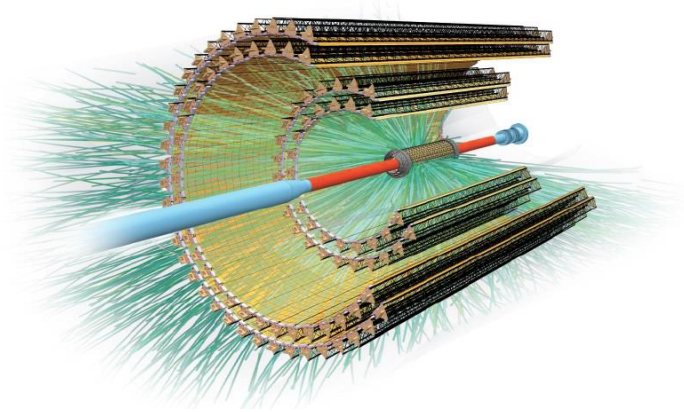
Spatial resolution
- Innermost 3 layers: $\sigma < 3\mu m$
- Outer layers: $\sigma \sim 5\mu m$

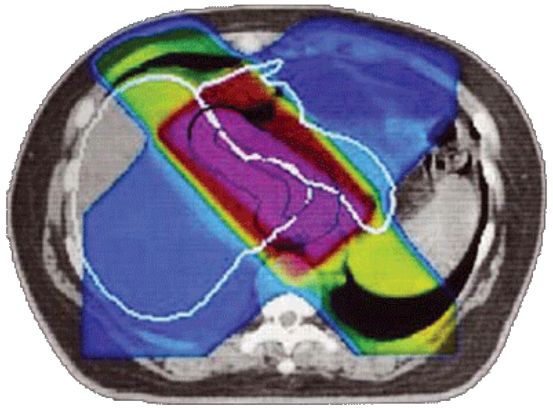
Vertex material thickness
- X/X0 ~ 0.05% / layer

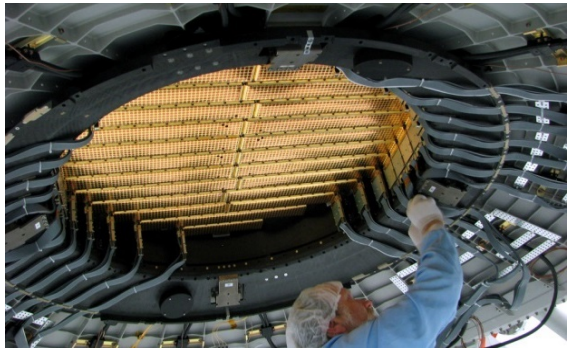
Time Measurement
Outermost layer integrates high precision time measurement
($\sigma_t \sim 20ps$)

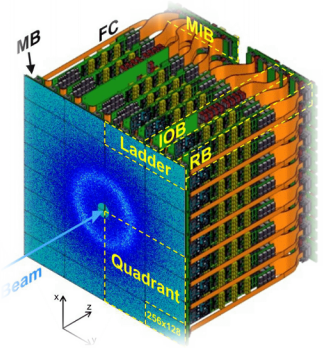
Concluding Remarks

Large area, low power CMOS pixel sensors are enabling devices for many cutting-edge research field and practical application: HEP trackers, medical imaging, space-borne instruments, FEL imagers, etc…









The use of CMOS and stitching technologies, open new opportunities in HEP

⇨ **Vertex detectors, large area tracking detectors and digital calorimeters**

- enhanced performance (spatial and time resolution)
- reduction of power consumption and material budget

large cost saving due to low production costs

Migration to smaller technology nodes (180nm ⇨ 65nm, 28nm) ⇨ large power reduction

Additional Material

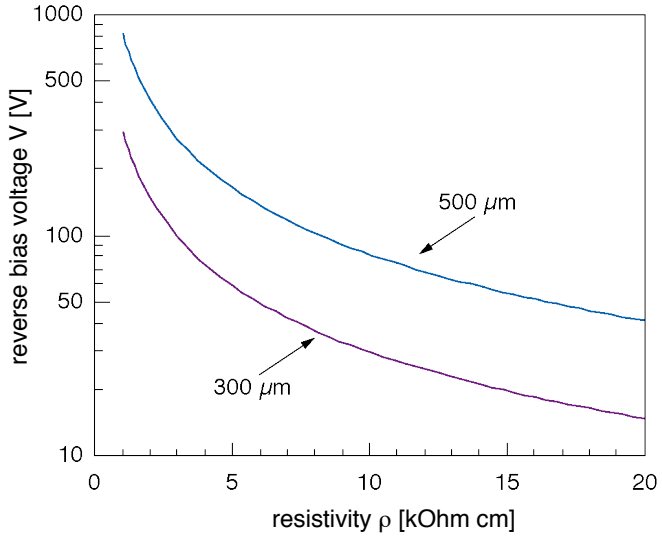
Detector characteristics – Depletion Voltage Capacitance

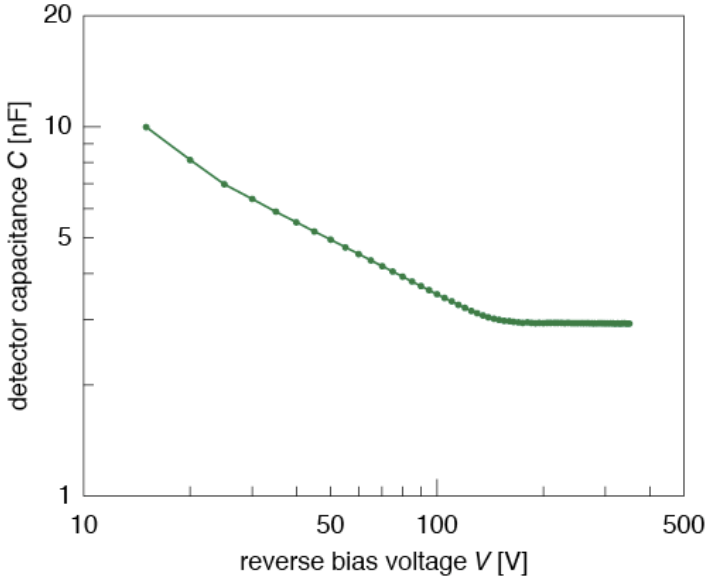
Depletion voltage = minimum voltage at which bulk is fully depleted

The operating voltage is usually chosen to be slightly higher (over depletion)

High resistivity material (i.e. low doping) requires low depletion voltage

$$V_{fd} = \frac{e}{2\varepsilon_s}(N_D - N_A)d^2$$





Measured detector capacitance as function of bias voltage, CMS strip detector
M. Krammer, F. Hartmann

For a Typical Si p-n junction ($N_a >> N_d >> n_i$) with planar geometry, the detector capacitance is

$$C = \sqrt{\frac{\varepsilon_0 \varepsilon_r}{2\mu\rho|V|}} \cdot A$$

ρ: resistivity of the bulk

μ: mobility of majority carrier

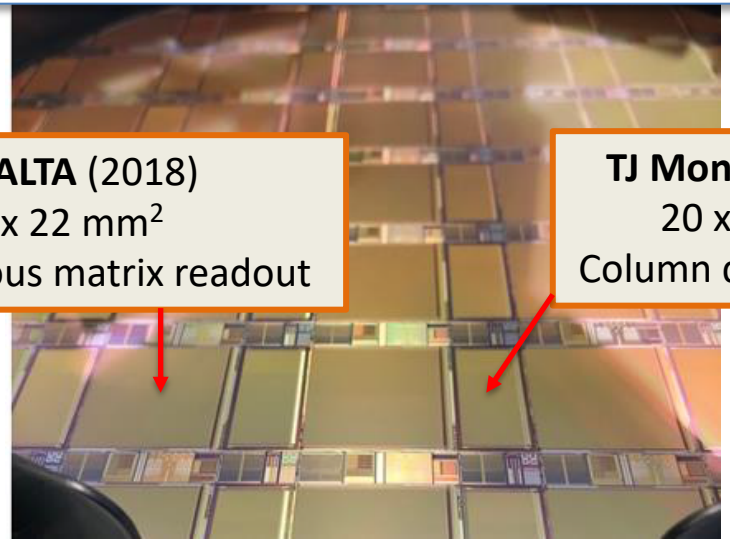
V: bias voltage

A: detector surface

New developments for ATLAS ITk: small electrode TJ modified process

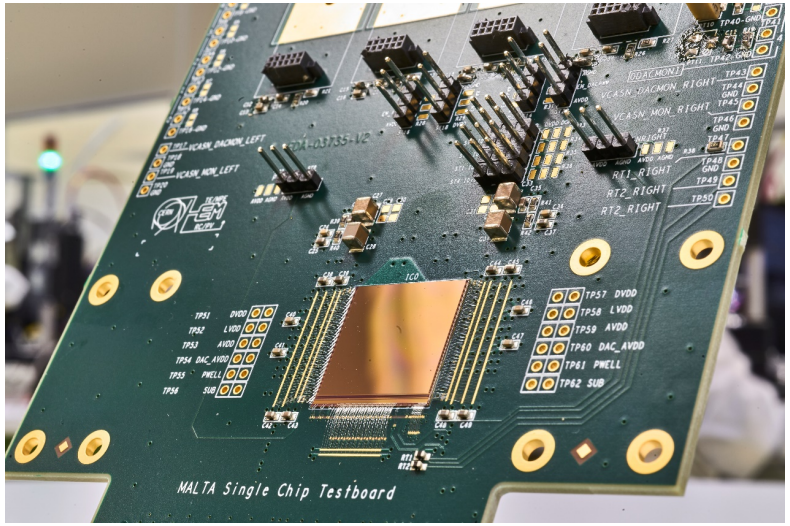
Analogue front-end optimized for timing, based on ALPIDE

Design of two large scale demonstrators
Collaboration CERN - Bonn



TJ MALTA (2018)
20 x 22 mm^2
Asynchronous matrix readout

TJ MonoPix (2018)
20 x 10 mm^2
Column drain readout



MALTA: Monolithic Pixel Detector from ALICE to ATLAS

- The 512 x 512 pixel – 8 sectors
- Front-end is a development from the ALPIDE one
- Design based on low-power analogue front-end and an asynchronous architecture to readout the pixel matrix