DCH prototypes instrumentation & measurements

The prototypes

Two DCH prototypes available

→ KLOE DC prototype

- 49 drift cells
- 7 layers
- almost square shape 2 cm^2
- 55 cm length (active area)
- 25 μm gold-plated tungsten sense wire diameter
- 80 μm silver-plated aluminum field wire diameter

→ DCH prototype (DCHProto1)

- 24 drift cells
- 4 layers
- 40 length (active area)
- almost hexagonal cells 2 cm^2

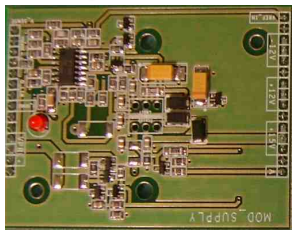
The DCHProto1 will be instrumented with a section of the KLOE readout chain and dedicated to gas mixture study and characterization

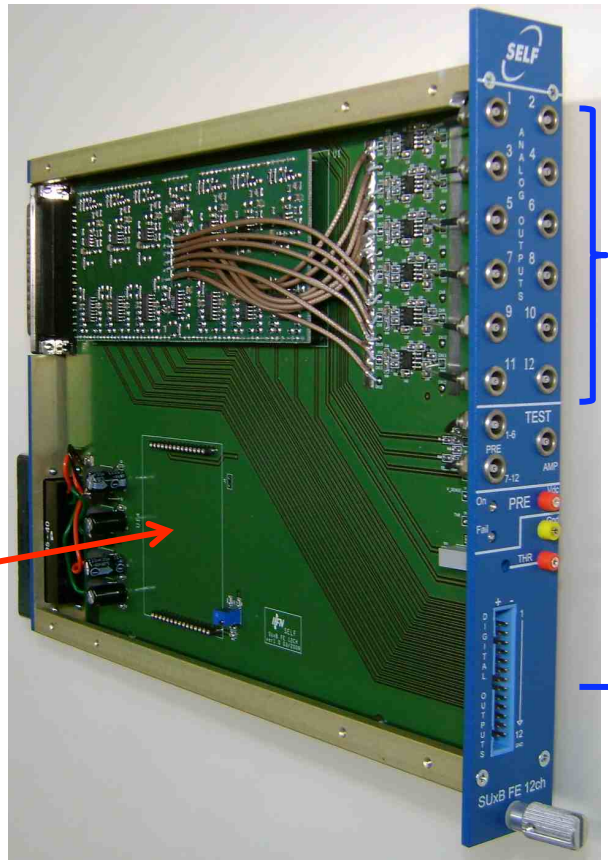
Analog inputs

Preamplifier LVPS

Preamplifier Test Pulse

Preamplifier LVPS





ADC outputs

TDC outputs

KLOE DC prototype – cluster counting

The KLOE DC prototype will be used to verify the possibility of using cluster counting in dE/dx measurements

Measurements results will be compared with simulations and (if possible) with high sampling frequency digital scope (parallel) data acquisition

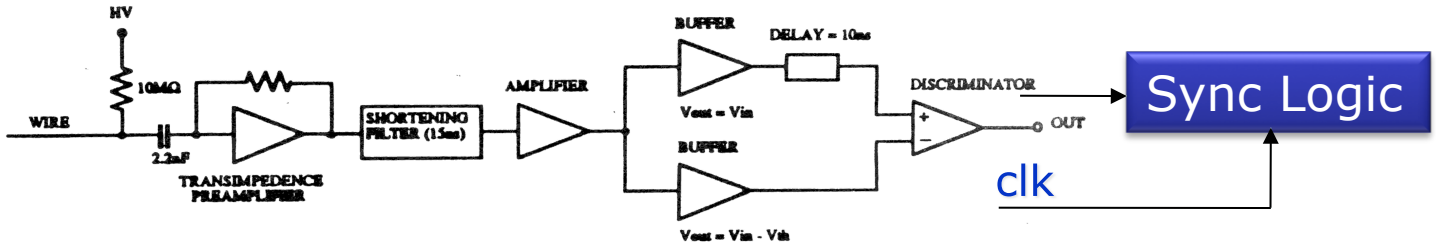
Three different technique should be investigated

→ Local derivative method (LNF)

→ FADC based device (Lecce)

→ Transient Waveform Recorder based device (Target1 chip - University of Hawai'I Manoa)

Cluster counting – local derivative method



Setup

→ up to 3 instrumented channels

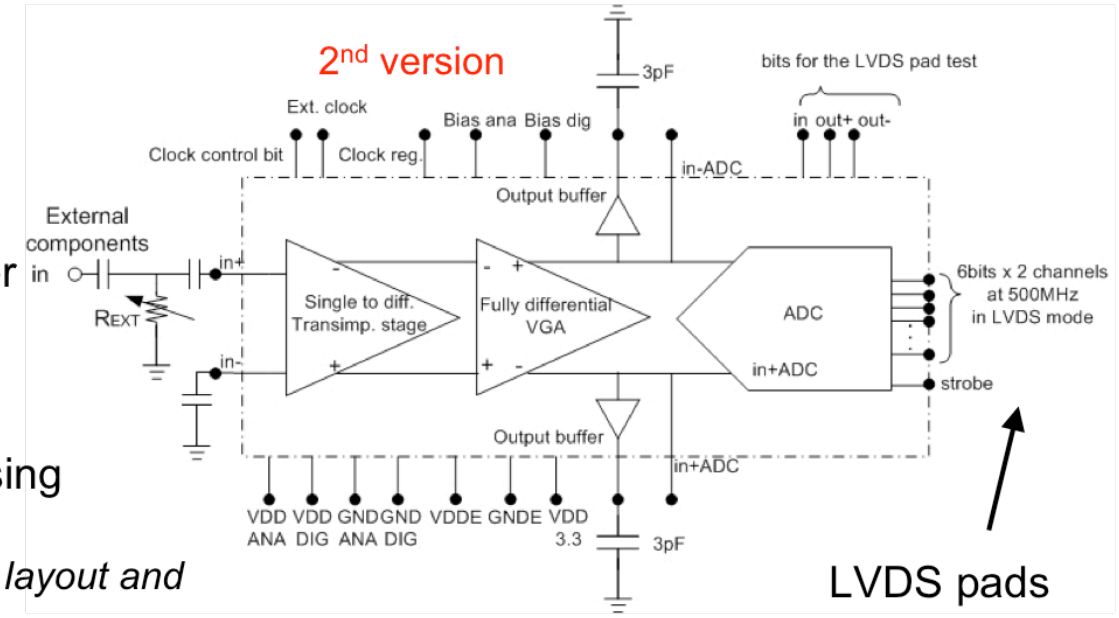
→ Different types of transimpedance preaplifiers

- preamplifier baseline
  - 1.7 mV/fC gain
  - ≈ 5 ns t_r
  - ≈ 400 μV rms noise output voltage (100 MHz BW)
- commercial (High Bandwidth) transimpedance preamplifier
  - Max3665 (equivalent)
    - 8 kΩ transimpedance
    - 450 μA peak current
    - 470 MHz BW

Cluster counting – Full Custom ASIC (I)

- In order to instrument a full scale Drift Chamber a special readout electronics is needed;
  goals:
  - fast (sampling rate ≥ 1Gsa/s, bandwidth > 500 MHz);
  - compact;
  - low cost in power and in money.

Overall architecture:

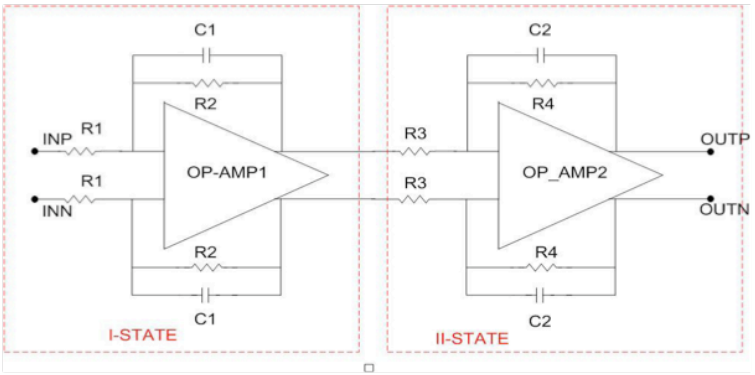


- designed in 0.13 µm CMOS technology;
- 1-2V and ~ 100 mW;
- Transimpedance preamplifier 26dB, -3dB @ 700 MHz;
- fast ADC 6 bit @ 1Gs/s;

Design and simulation using
CADENCE 5.4.14
For the second chip version layout and MOS technology studied

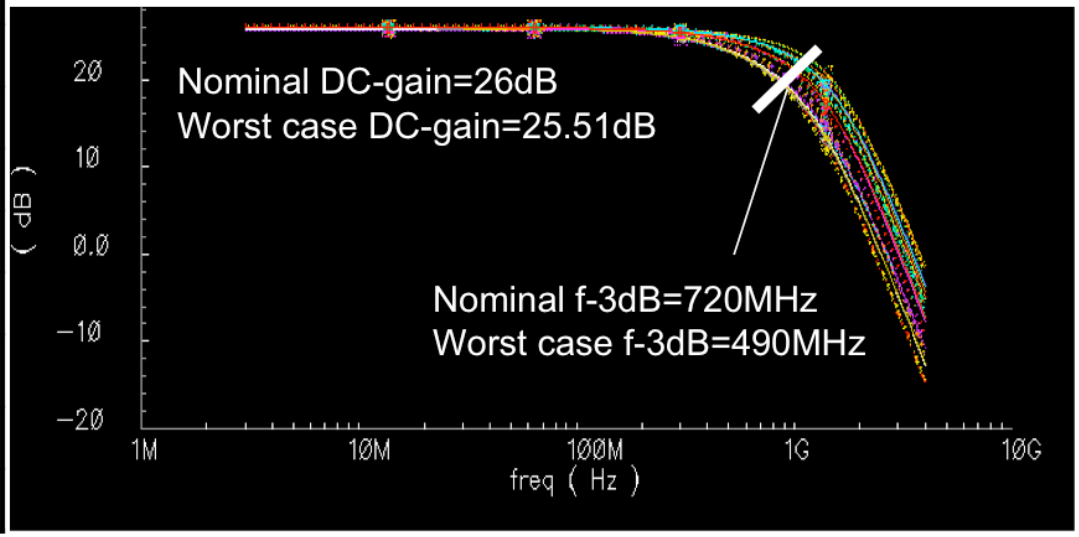
Cluster counting – Full Custom ASIC (II)

Preamplifier characteristics



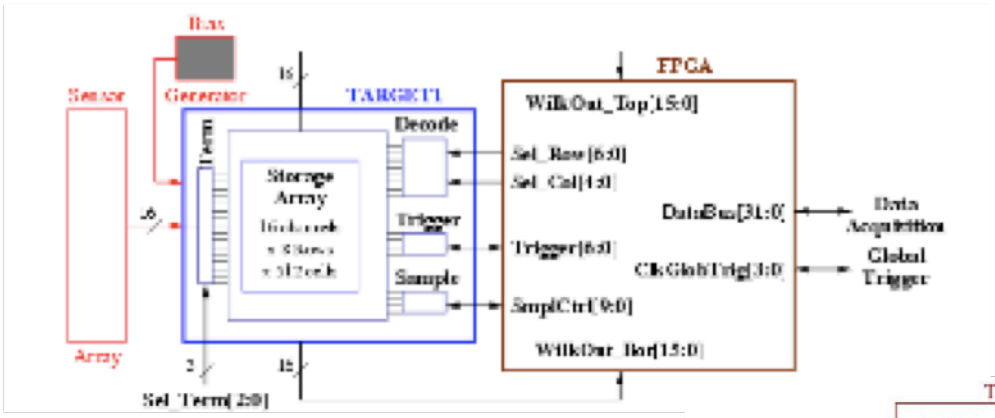
The following variables have been considered:
-Process spread (nom-ss-ff models for MOS, capacitors and resistors);
-Temperature variation (0°-80°).

Parameter	Value
Input impedance	50 Ω
No. of stages	2
1st stage gain	16 dB
2nd stage gain	10 dB
Overall DC-gain amplifier	26.12 dB
Nominal -3dB Bandwidth amplifier	735MHz
Current consumption	13.22 mA
Noise	81 μV_{rms}



Cluster counting – Target 1

16-channel, GSPS Transient Waveform Recorder with Self-Triggering and Fast, Selective Window Readout

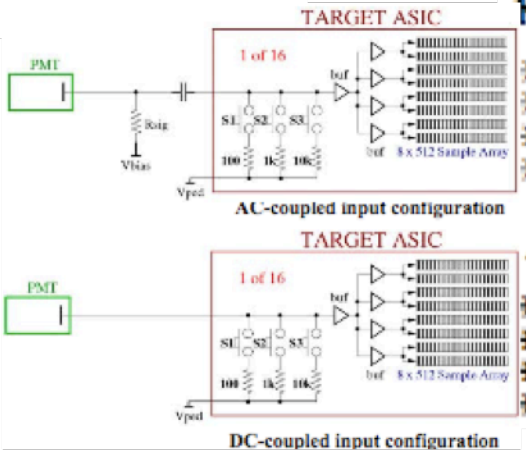


Features

- High density (16 channels)
- Good timing performance
- 9-10 bits of resolution
- Fast conversion (<0.5us/32 samples)
- Random access to groups of 16 samples
- Flexible operating modes
- 100Ω, 1k and 10k programmable terminators

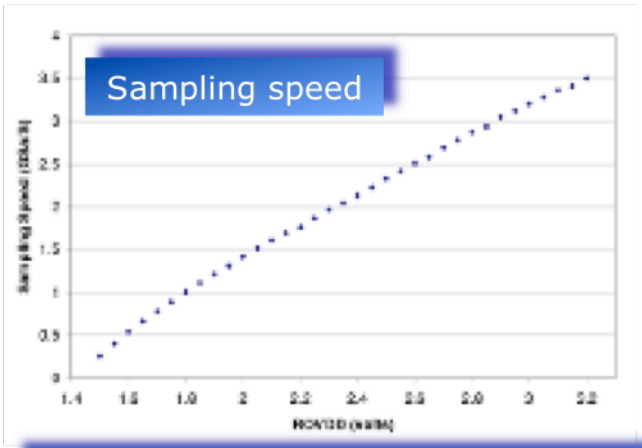
Key Specifications

- Low power (<10mW/channel)
- Giga-sample per second recording
- Selective (windowed) readout
- 4,096 storage samples/channel



Applications

- Next generation TeV gamma readout
- Low-cost, highly integrated systems
- Collider Detector Instrumentation
- Portable/pocket oscilloscope



Temperature compensation required for fixed sampling frequency

Readout rates up to 50kHz (2 channels ?)

Time schedule

The prototypes setup time schedule could be delayed because the LNF electronic workshop is involved in the KLOE2 experiment starting up foreseen in November 09

DCHproto1 (24 channels / gas mixtures studies)

→ Wiring/Instrumentation : October 09

KLOE DC prototype (cluster counting studies)

→ Because the 49 cells available, several cluster counting techniques can be tested at the mean time

→ The main aim is to get an answer on the cluster counting feasibility within march 10

- Further investigation on cluster counting foresee the measurement of the improvement on the impact parameter measurement