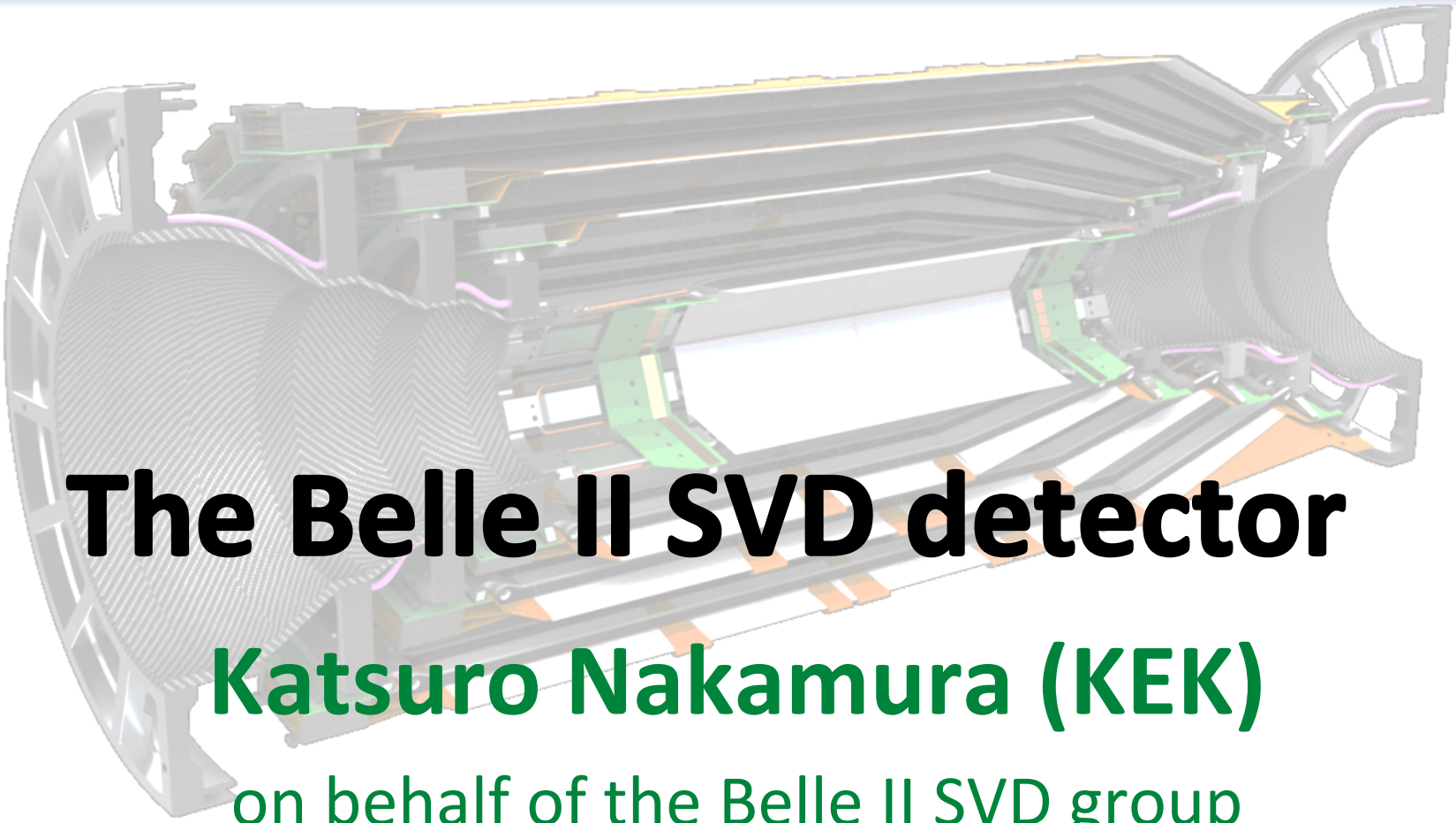
KEK

High Energy Accelerator Research Organization



The Belle II SVD detector

Katsuro Nakamura (KEK)

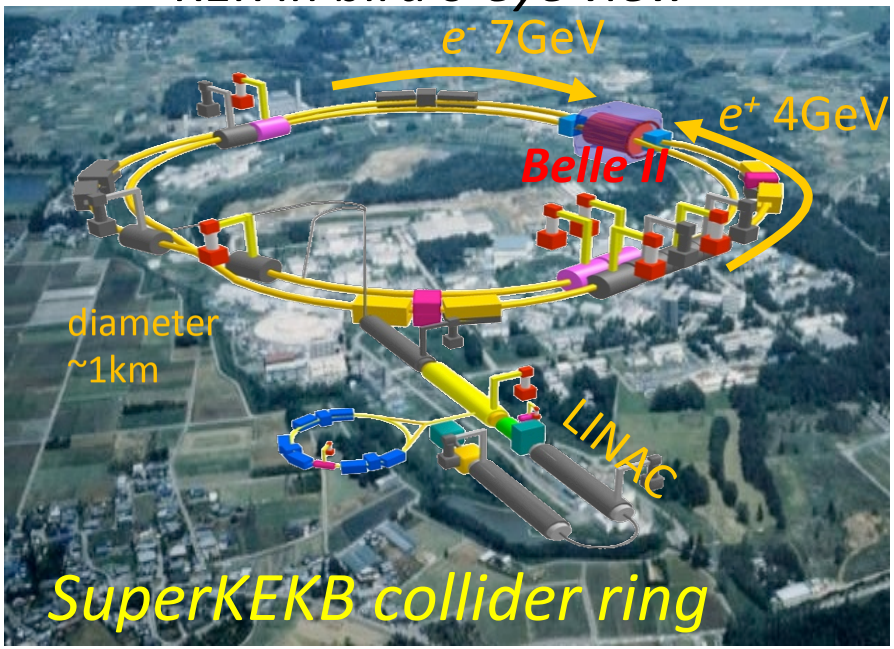
on behalf of the Belle II SVD group

VERTEX2016 Sep. 26, 2016

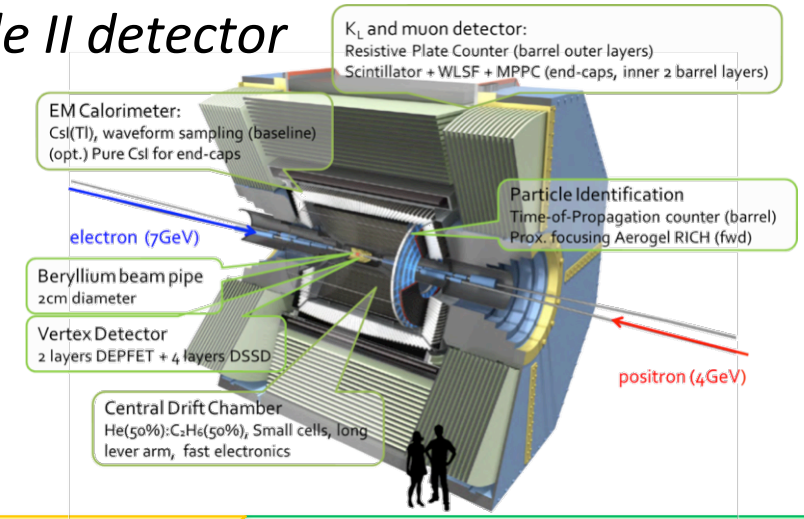
SuperKEKB and Belle II Experiment

- **SuperKEKB collider at KEK**
  - e^+-e^- collider with *Vs* of 11GeV (= $M_{\Upsilon(4S)}$)
    - Asymmetric beam: e^+ 4 GeV , e^- 7 GeV
  - World-highest designed luminosity: $L = 8.0\times10^{35}\ cm^{-2}s^{-1}$
- **Belle II experiment**
  - Intensity frontier experiment at SuperKEKB to discover and understand physics beyond the SM (BSM).
  - Precise determination of the decay vertices and low-momentum tracking are essential to perform the BSM search.
- **The detectors and accelerator are being developed toward start of physics experiment at 2018.**

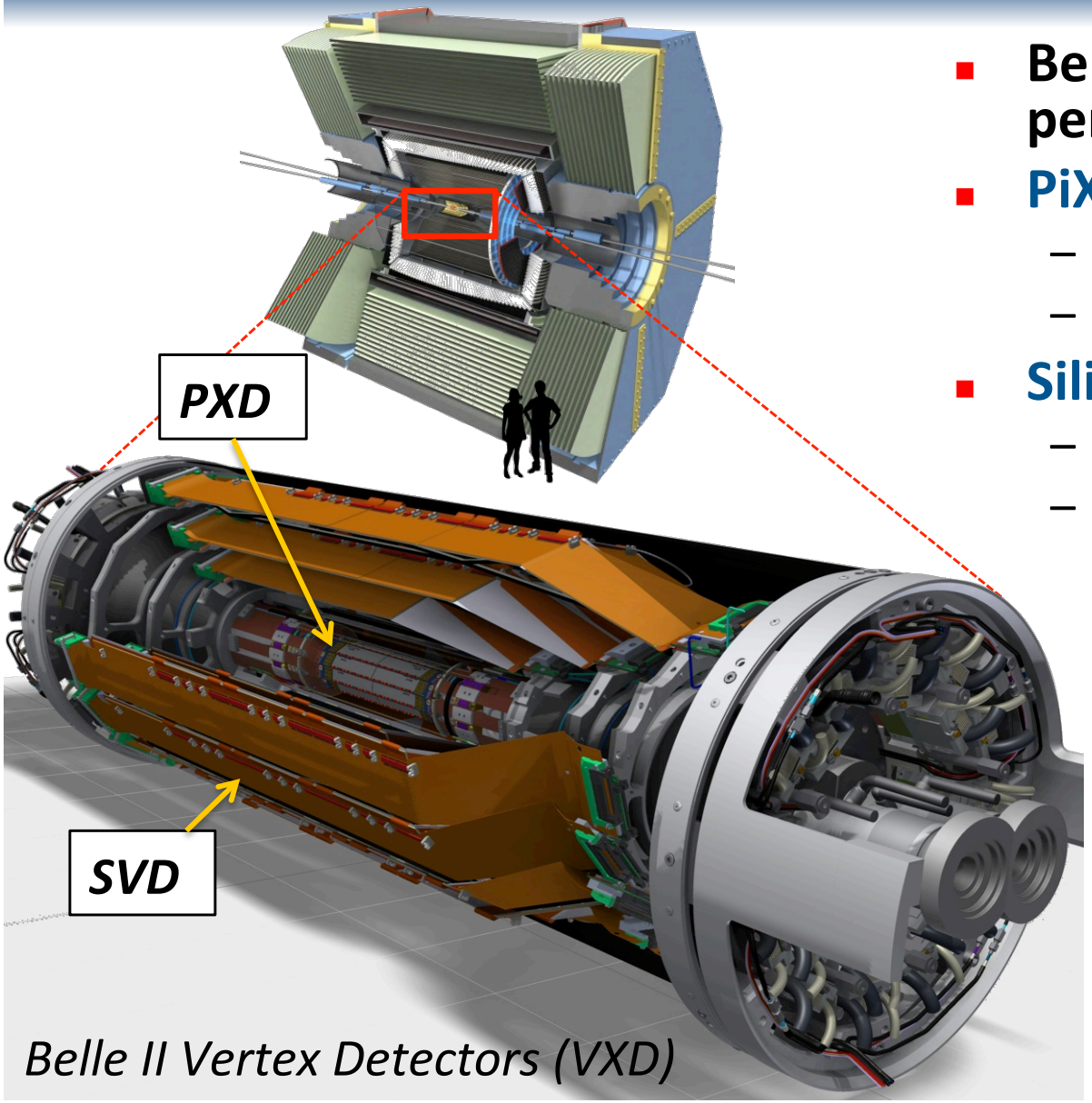
KEK in bird's-eye view



Belle II detector



Belle II Vertex Detectors



Belle II Vertex Detectors (VXD)

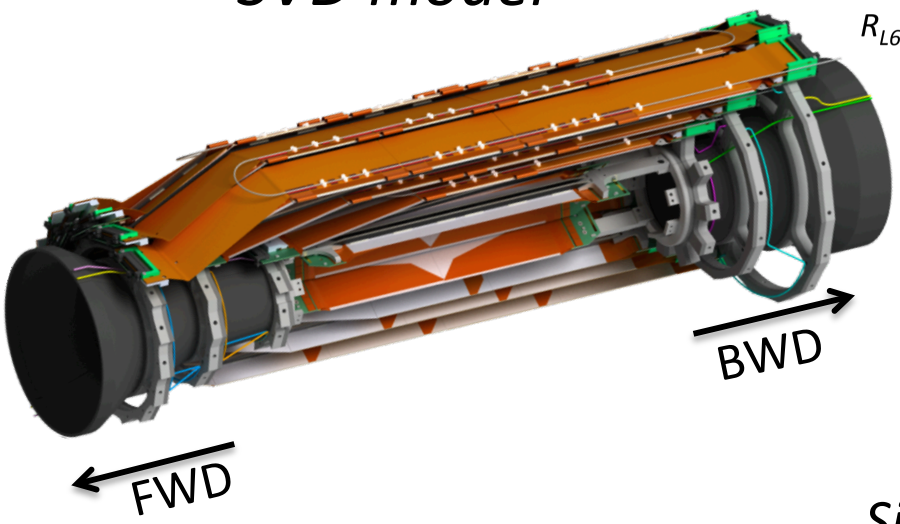
- **Belle II vertex determination is performed by 2 Si detectors.**
- **PiXel Detector (PXD)** *see previous talk*
  - Innermost 2 layers
  - Based on DEPFET pixels
- **Silicon Vertex Detector (SVD)**
  - Outer 4 layers
  - Double-sided Si strip detectors (DSSDs)

VXD requirements

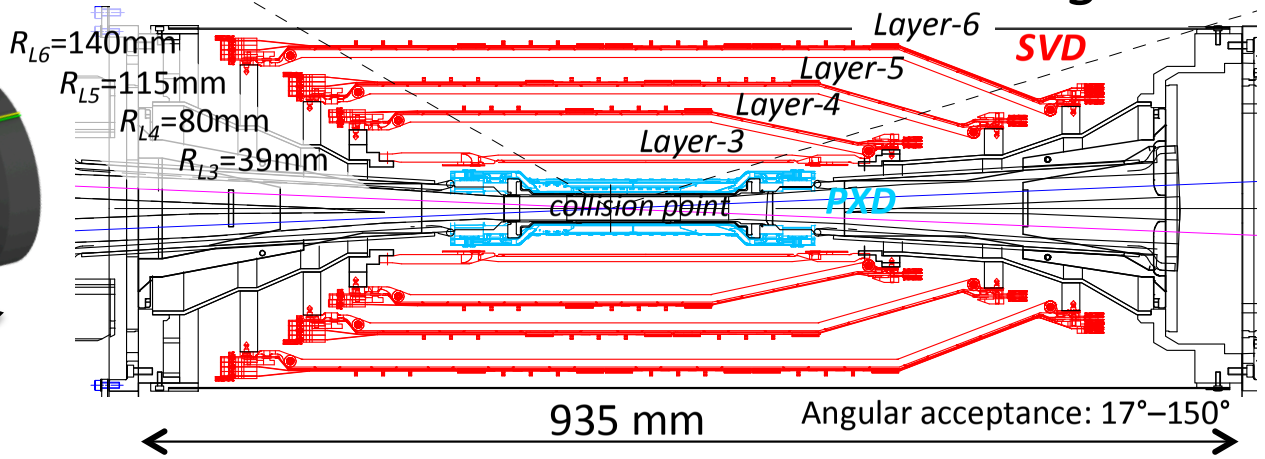
- Fast – to operate in high background environment
- Better resolution at IP – to compensate reduction of boost wrt. Belle I
- Radiation hard (up to 100 kGy)
- Self-tracking capable – to track particles down to 50 MeV in p_T

SVD Detector Overview

SVD model

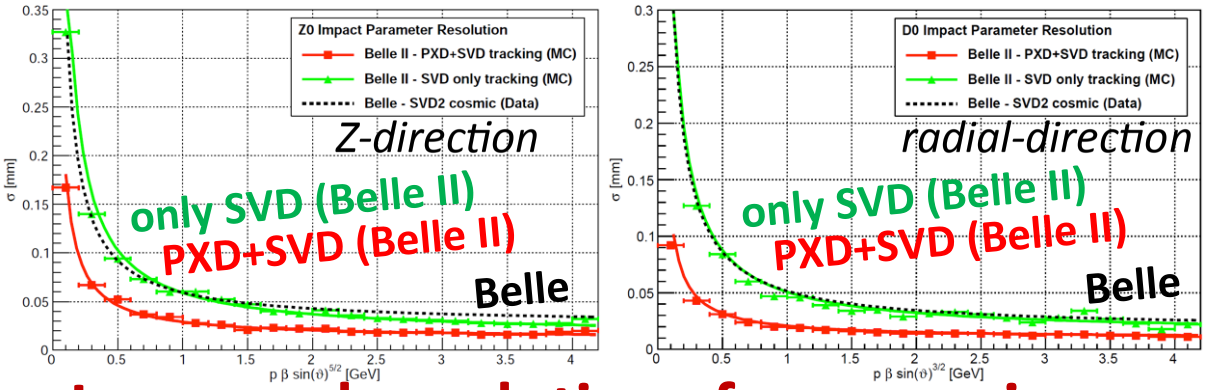


PXD+SVD cross section drawing



- **4 SVD layers (Layer-3 to -6) consist of ladders.**
- **The ladders are composed of several DSSD modules.**
- **Slant shapes in FWD region for the material budget reduction.**
- **Average material budget: 0.7%X_0 per layer**

Simulated resolution for track impact parameter (IP)

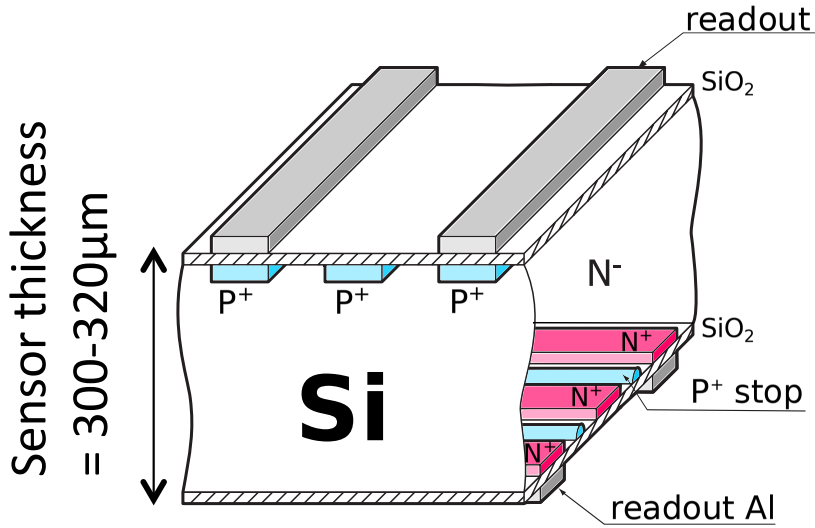


Improved resolutions from previous Belle experiment are expected.

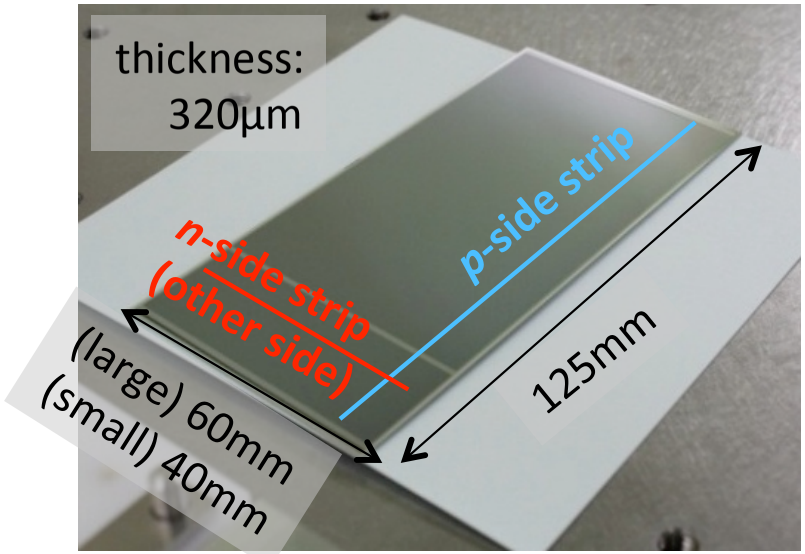
σ_{IP} ~ 20um at p_T = 2GeV/c

SVD Silicon Sensor

DSSD (Double-sided Si strip detector)



Rectangular sensor (HPK)

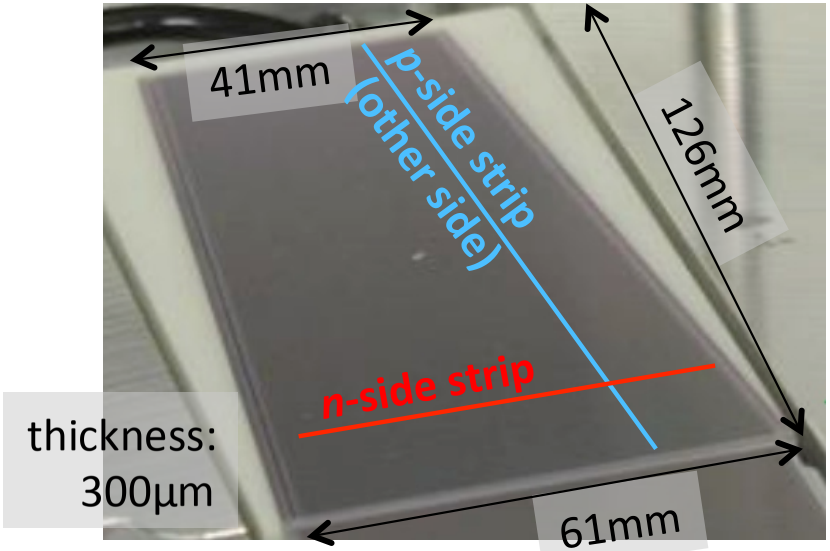


Strip numbers and pitches

- **3 types of DSSD sensors**

Sensors	Rectangular (Large)	Rectangular (Small)	Trapezoidal
# of *p*-strips	768	768	768
***p*-strip pitch**	75μm	50μm	50…75μm
# of *n*-strips	512	768	512
***n*-strip pitch**	240μm	160μm	240μm

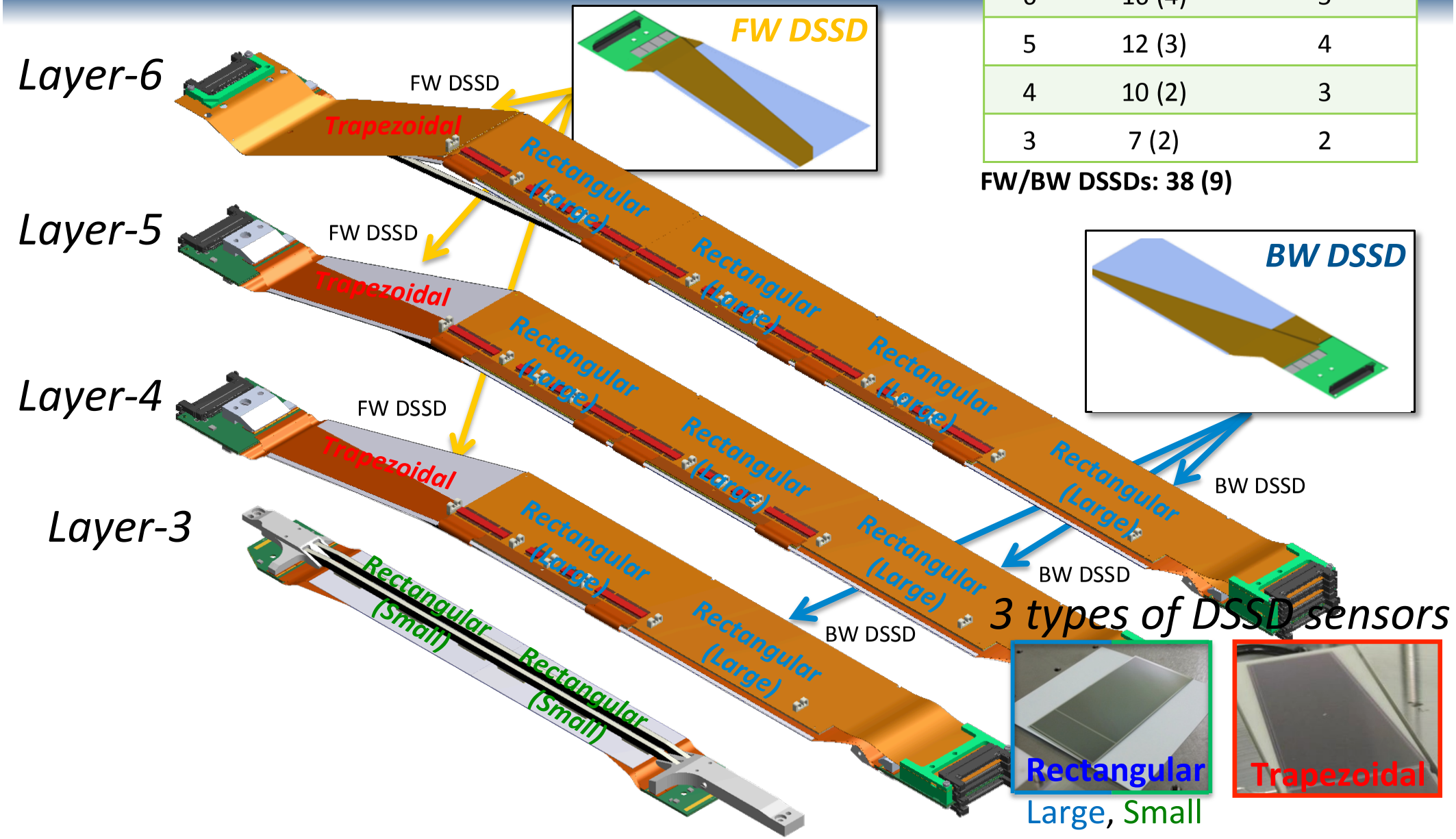
Trapezoidal sensor (Micron)



DSSD Locations in Ladders

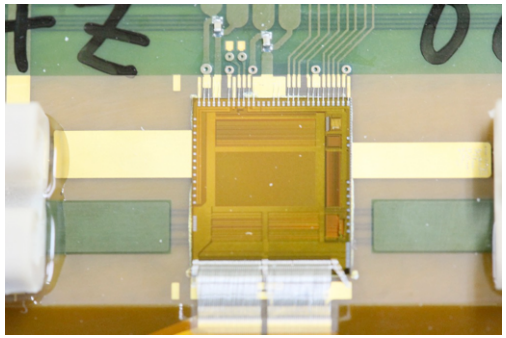
Layer	Ladders (spares)	DSSDs / ladder
6	16 (4)	5
5	12 (3)	4
4	10 (2)	3
3	7 (2)	2

FW/BW DSSDs: 38 (9)

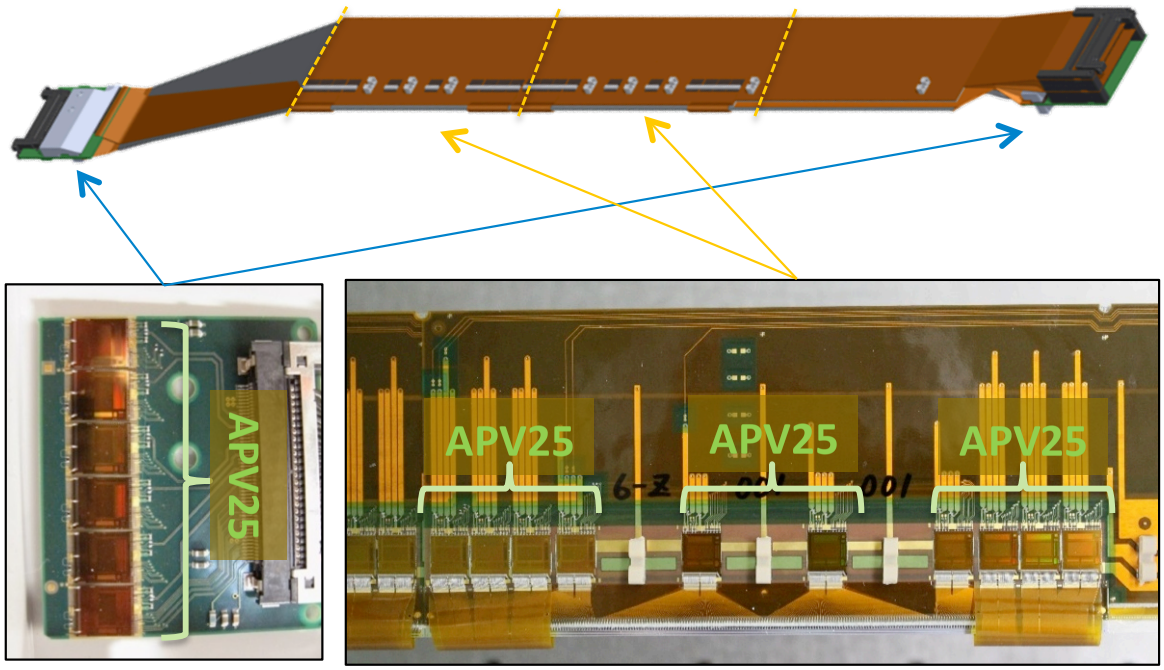


Front-End Readout ASIC

APV25 chip



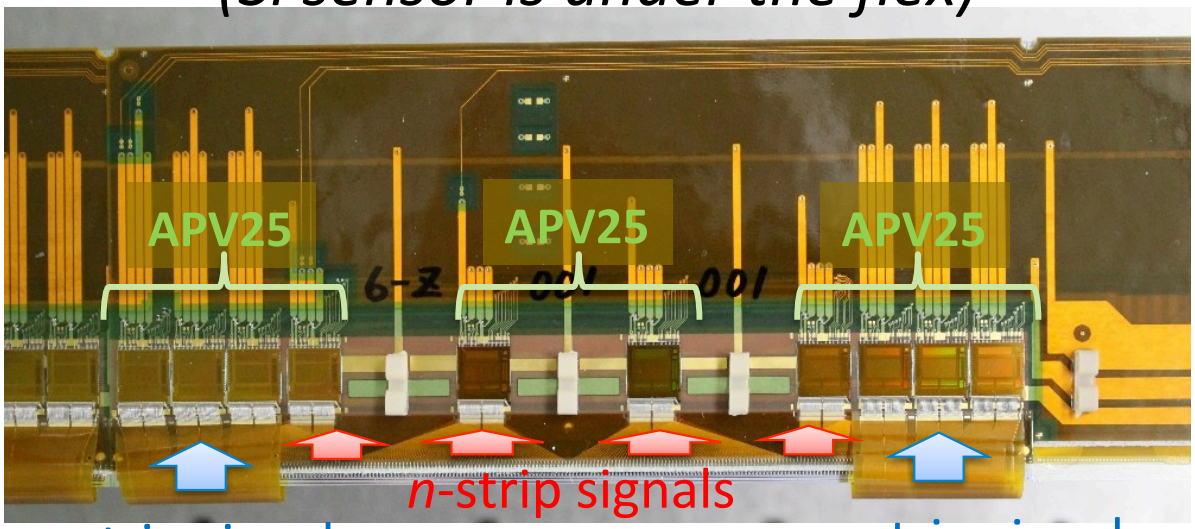
APV25 chips in ladder



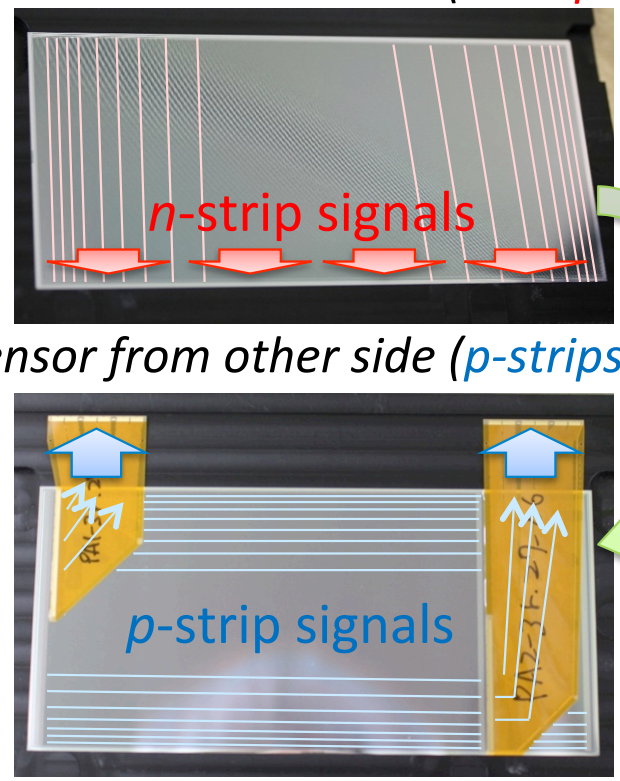
- **APV25 chip**
  - A high background in Belle II requires short signal shaping time and a good radiation hardness.
  - APV25 chip is a suitable solution for SVD.
    - Originally developed for CMS.
- **APV25 Specification**
  - # of input channels: 128 ch.
  - Shaping time: 50nsec
  - Radiation hardness: > 1MGy
- **Chip-on-Sensor (see next slide)**
  - Thinned to 100μm thickness for the material budget reduction.
  - Max. heat dissipation: 0.4W
    - → Necessity of cooling

Chip-On-Sensor Concept

ORIGAMI flex
(Si sensor is under the flex)

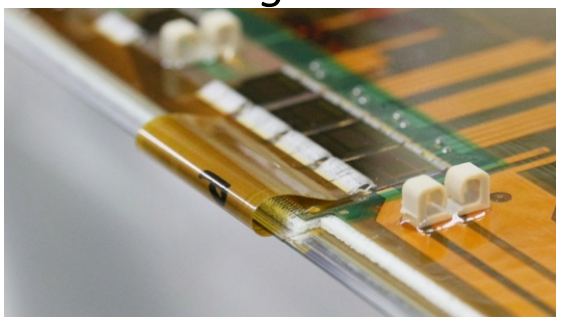


Sensor under ORIGAMI (n-strips)



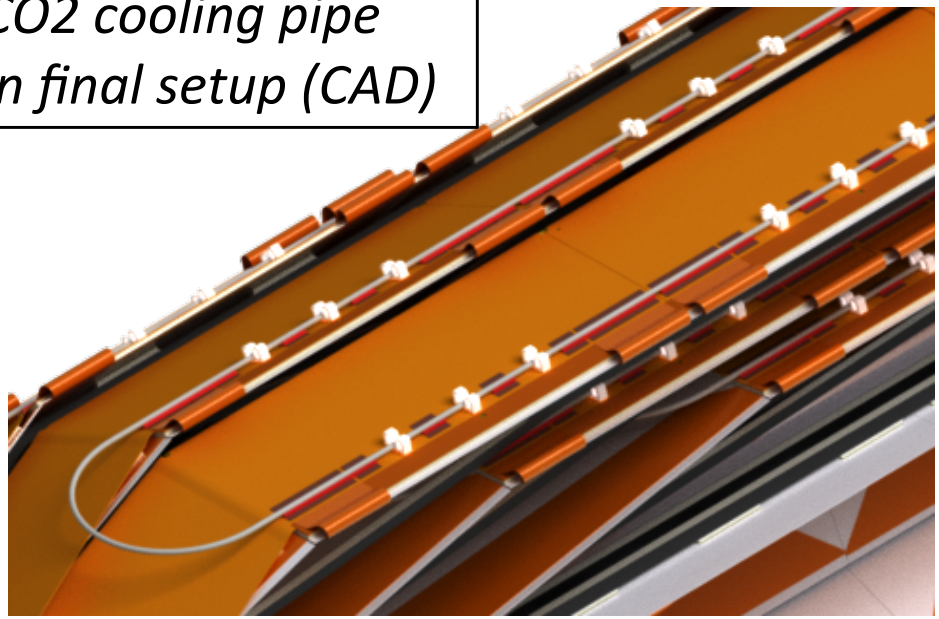
- **Flex circuit (ORIGAMI flex) is glued on sensor *n*-strip surface with an electrical/thermal-isolation foam.**
- **APV25 are placed on the ORIGAMI flex to minimize the analog path length (capacitive noise).**
  - Sensor strips and ORIGAMI flex are connected with Al wire-bonding (ϕ25μm).

Wire bonding with Al wires.

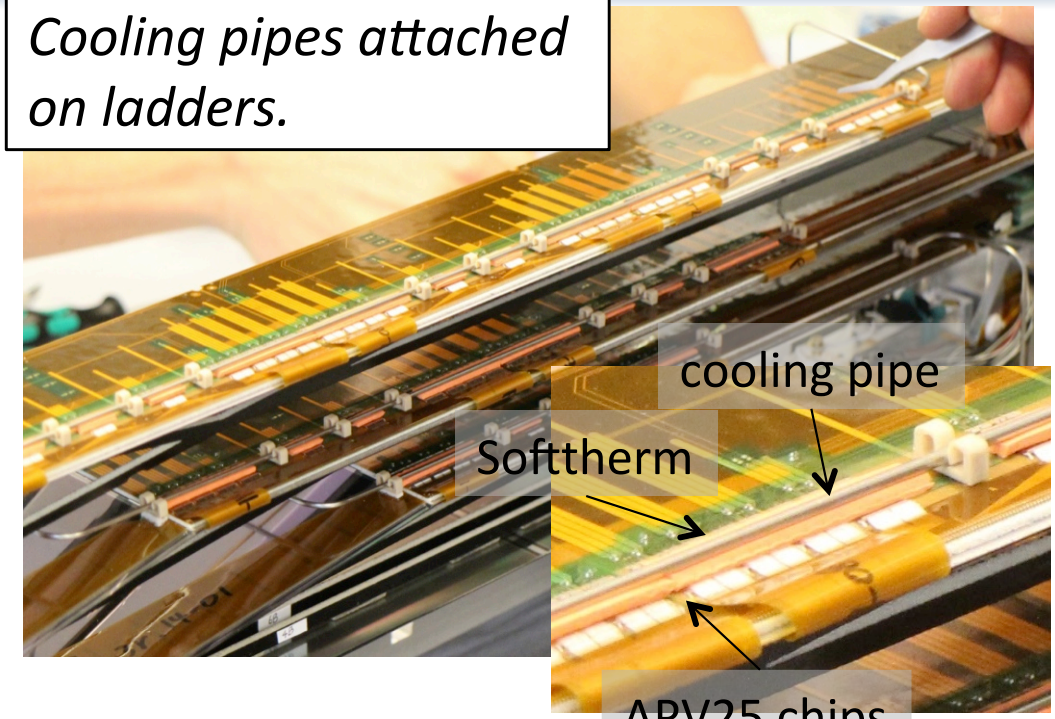


CO2 Cooling for Ladders

CO2 cooling pipe in final setup (CAD)



Cooling pipes attached on ladders.



- **Necessity of cooling**
  - SVD total heat dissipation from all APV25 chips can be 700W in max.
- **2-phase (liquid and gas mixture) CO2 cooling system**
  - Efficient and low mass cooling
  - Simple control of coolant temperature (only with pressure)
  - Small pressure loss in tubes
- **Thin stainless tube (OD:1.6mm, thickness:0.1mm) is employed.**
  - Less material budget

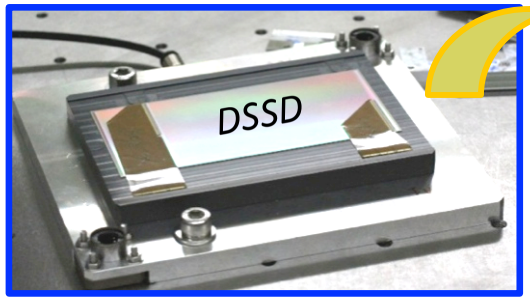
Softtherm 86/125

thermal-conductive dielectric pad.

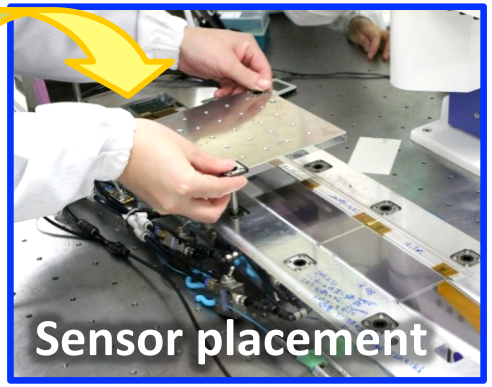
SVD Ladder Assembly (1)

1. Precision DSSD alignment

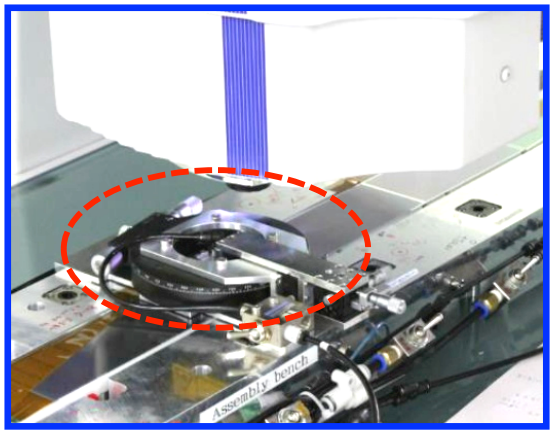
DSSDs are handled with precision assembly jigs (*O*(50μm)), on which the sensors are fixed by vacuum chucking.



Sensor fixed on a jig



Sensors are aligned in *O*(10μm) by a position tuning jig with monitoring through a CMM.

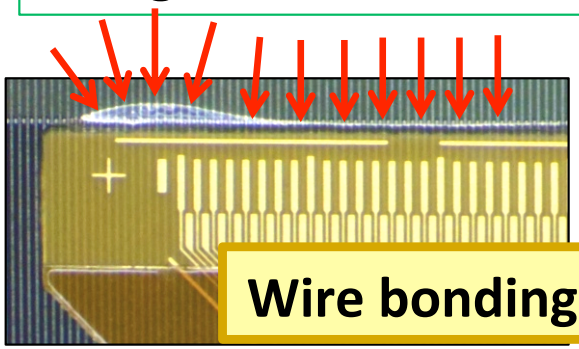


SVD Ladder Assembly (2)

2. Ladder fabrication: gluing

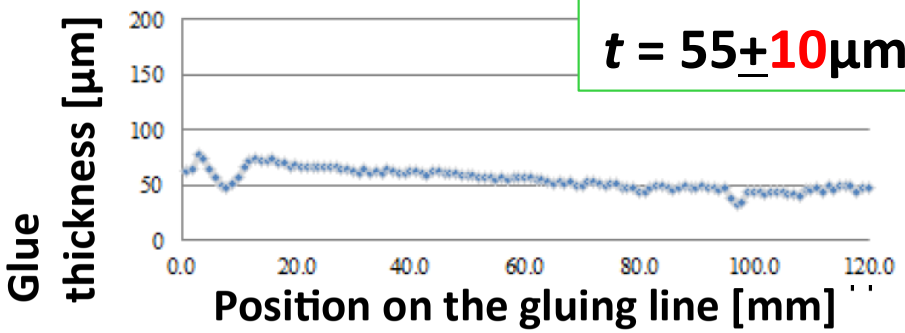
Ladders are fabricated by gluing the components by Araldite®2011.

Glue spread below bonding pads affects to the bonding yield and pull strength → glue amount and glue lining are controlled by a gluing robot.



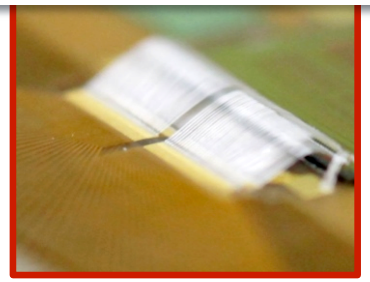
Appropriate spread of glue to the flex edge

Wire bonding pads



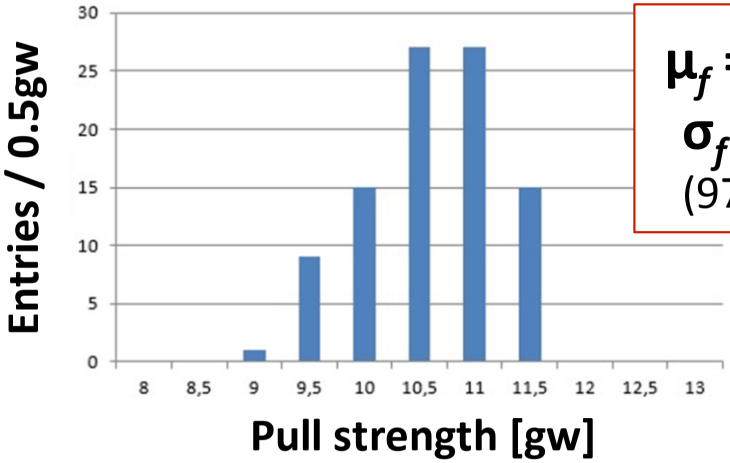
t = 55±10μm

3. Electrical connection: wire bonding



The flex↔DSSD strips and flex↔APV25s are electrically connected by the wire bonding with Aℓ(99%) wire(ϕ=25μm). Number of total bonds = 450k.

Bonding machine parameters are so tuned to realize yield>99% and pull strength f: μ_f>5gw, σ_f/f<20%.



μ_f = 10.7gw
σ_f = 0.6gw
(97 samples)

Please see more details in Hyebin Jeon's poster presentation.

Distributed Assembly Sites

@HEPHY (Austria):
- **Layer-5** assembly

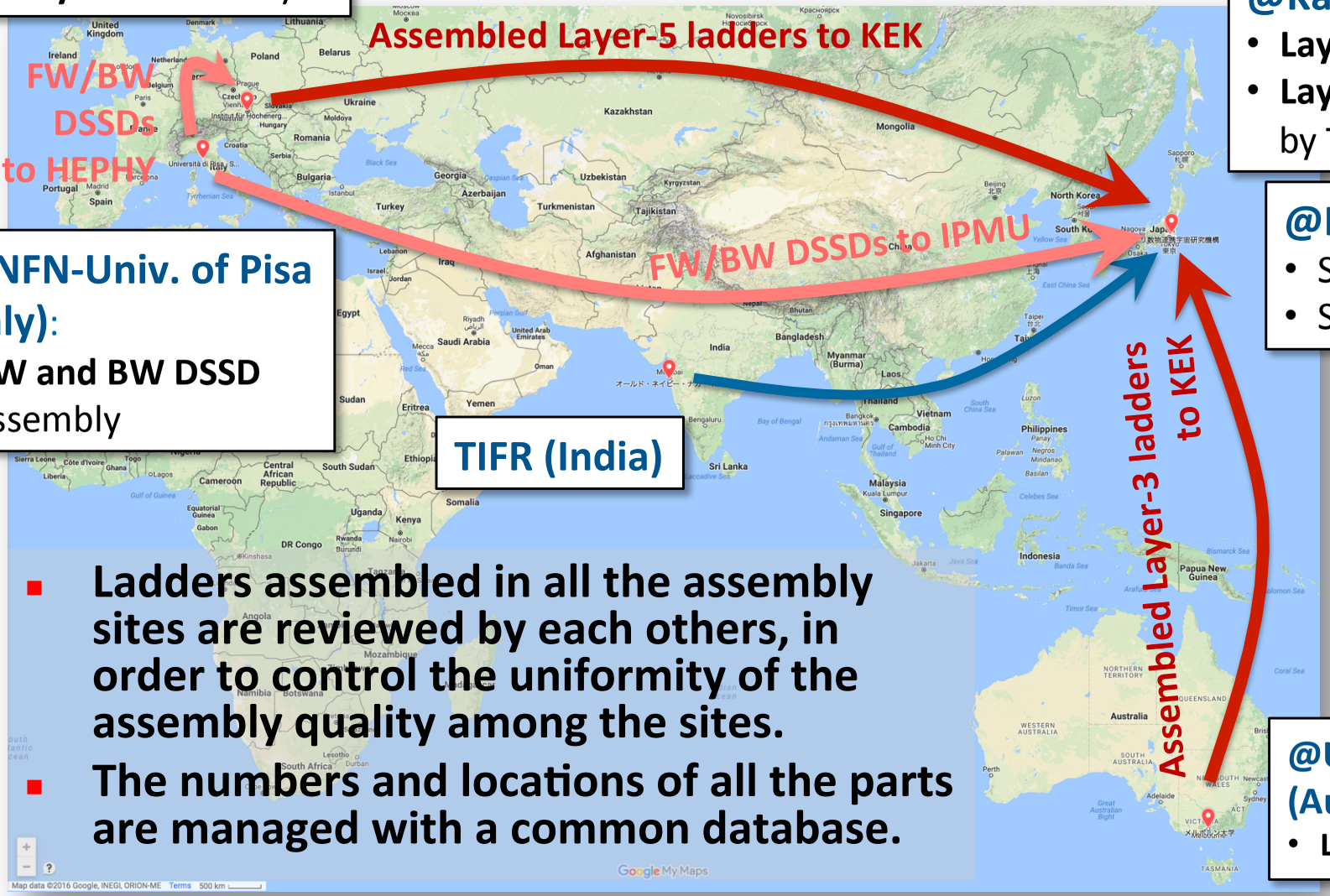
@Kavli IPMU (Japan):
- **Layer-6** assembly
- **Layer-4** assembly by TIFR

@KEK (Japan):
- SVD assembly
- SVD installation

@INFN-Univ. of Pisa (Italy):
- **FW and BW DSSD** assembly

TIFR (India)

@Univ. of Melbourne (Australia):
- **Layer-3** assembly



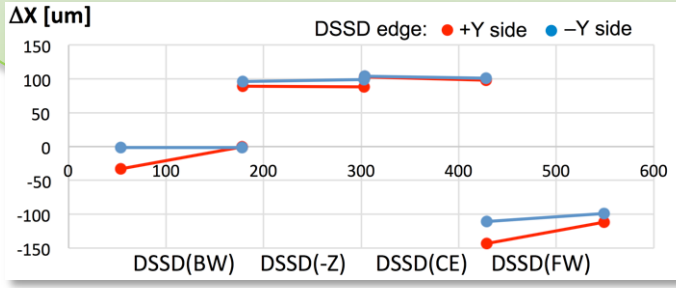
- **Ladders assembled in all the assembly sites are reviewed by each others, in order to control the uniformity of the assembly quality among the sites.**
- **The numbers and locations of all the parts are managed with a common database.**

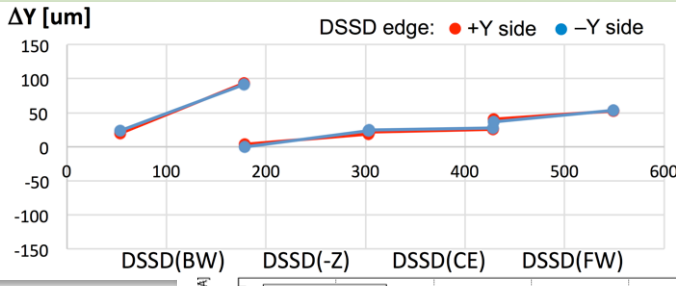
Ladder Quality Assurance

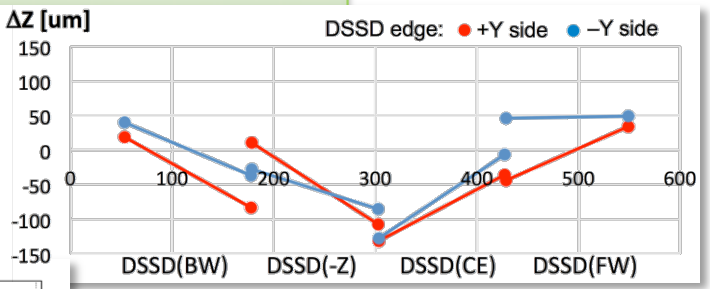
We perform the following quality assurance tests for every assembled ladder.

1. Mechanical precision measurement with CMM

- Measure shifts of DSSD sensors in XYZ directions. Typically less than 150um.

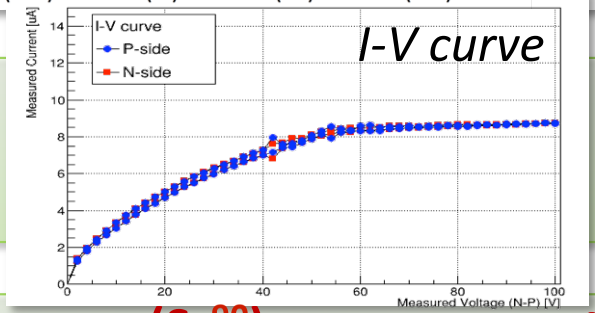






2. I-V curve measurement

- Confirm the sensor functionality for biasing.

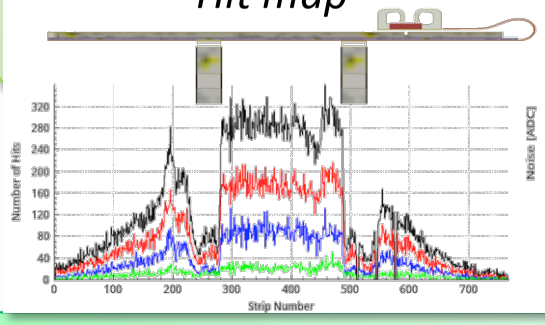


I-V curve

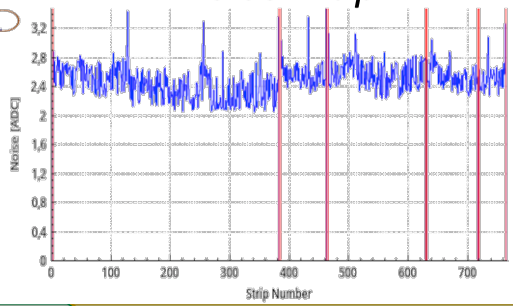
3. Electrical qualification laser/β-source (Sr^{90}) measurement

- Check defect strips and DSSD performance for particles.

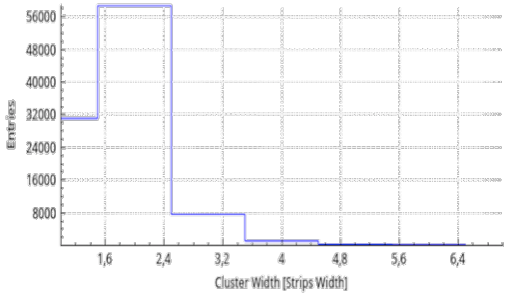
Hit map



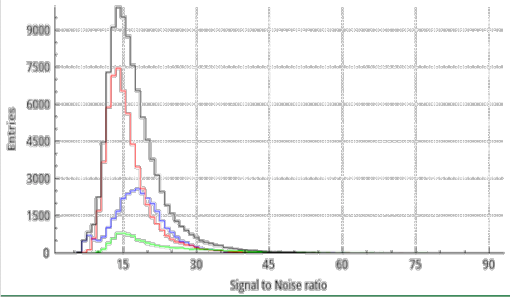
Noise map



Cluster size distribution



S/N ratio distribution

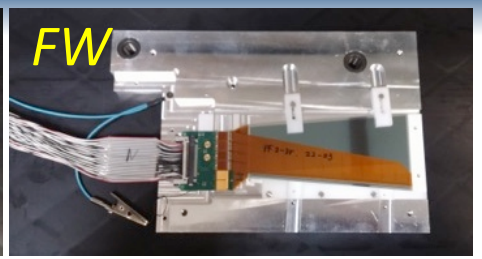


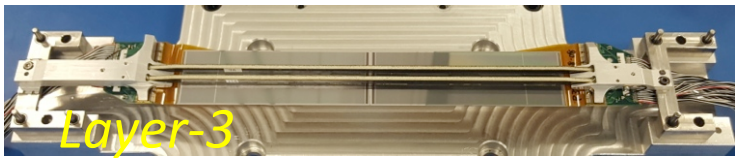
Ladder Production Status

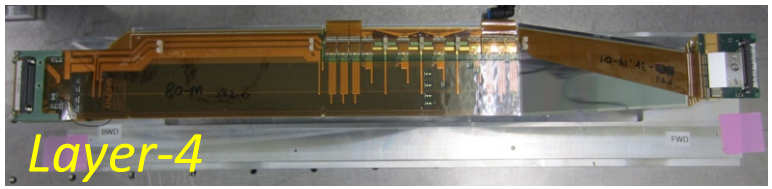
- **Now all the ladder assembly sites are in mass-production stage.**
  - Ladder mass-production was started from early 2016.
- **FW/BW DSSD**
  - BW: 100% completed
  - FW: 94% completed
- **Layer-3 Ladder**
  - 5 out of 7+2 ladders (56%) completed
- **Layer-4 Ladder**
  - 3 out of 10+2 ladders (25%) completed
- **Layer-5 Ladder**
  - 4 out of 12+3 ladders (27%) completed
- **Layer-6 Ladder**
  - 3 out of 16+4 ladders (15%) completed

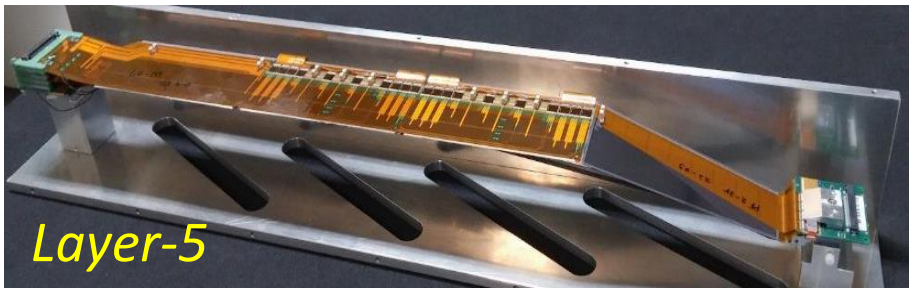
(at the mid of Sep., 2016)

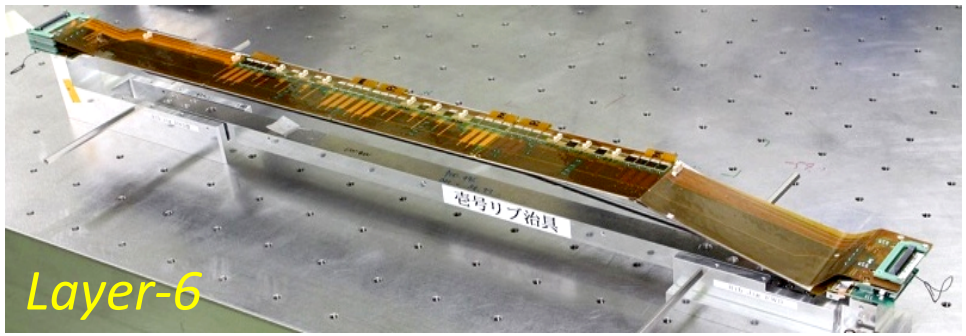
- **Completion of the ladder production by Nov. 2017 is expected.**









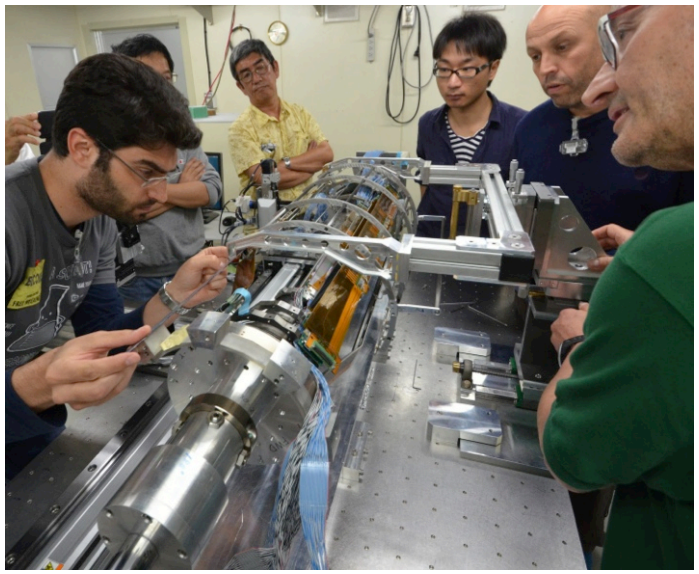


SVD Assembly

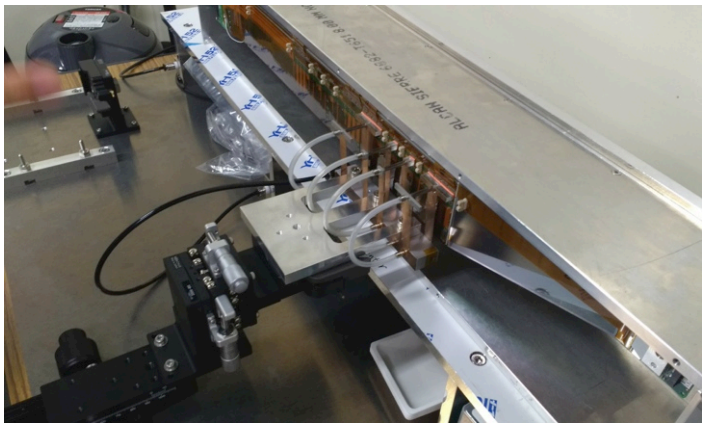
- **SVD assembly at KEK is our final step to complete the construction of SVD.**
  - SVD assembly procedure must be safe and well established, otherwise any mistake can destroy all mounted ladders at once. Now tools for the safe SVD assembly are being developed.
- **Prototypes of all necessary assembly tools have been produced. The preliminary procedure was reviewed by a review-committee including external members.**
- **We will finalize the tool by Feb. 2017 and consequently will start the SVD assembly.**

Ladder mount tool

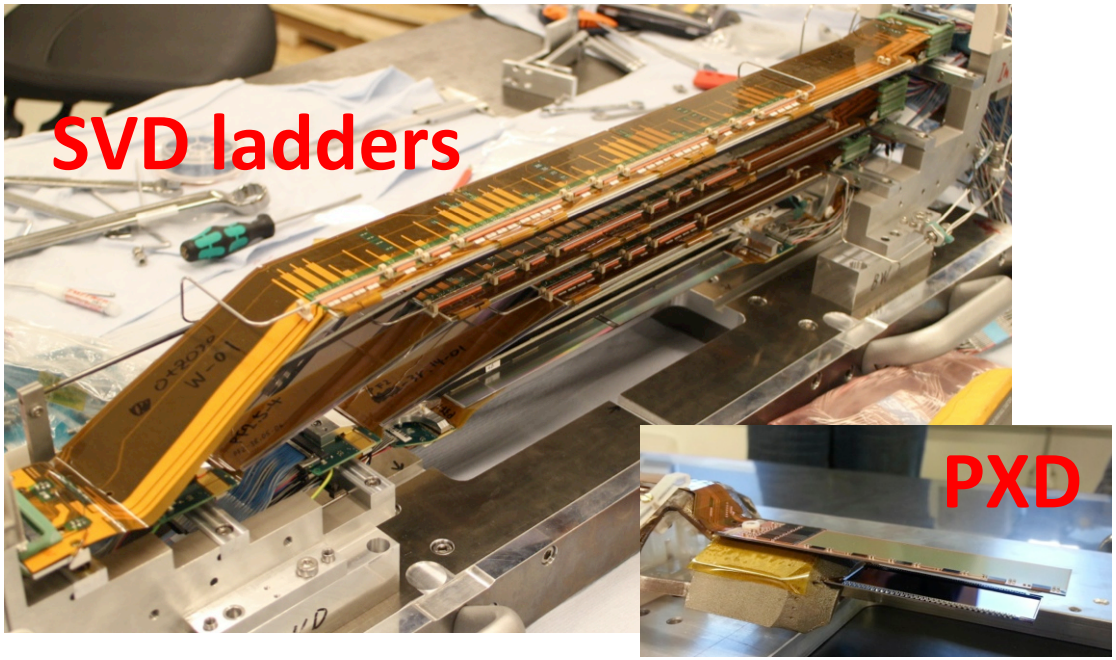
CO2 pipe attachment tool



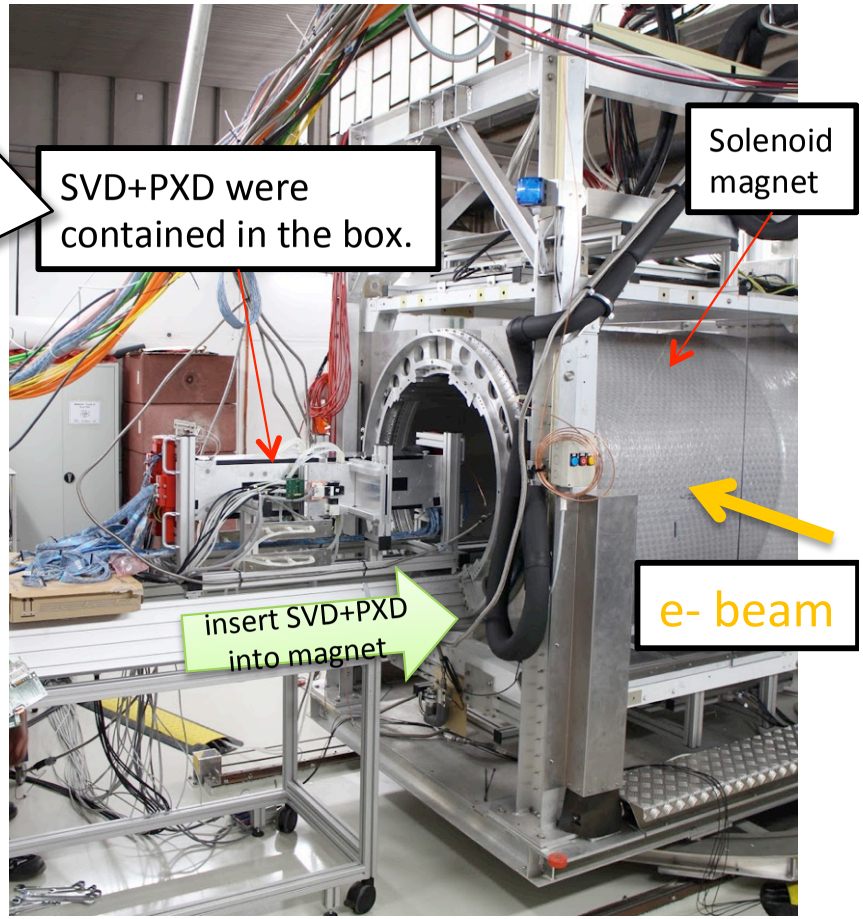
Softtherm attachment tool



Beam Tests for Ladder Performance Study



SVD + PXD detector setup on Apr. 2016

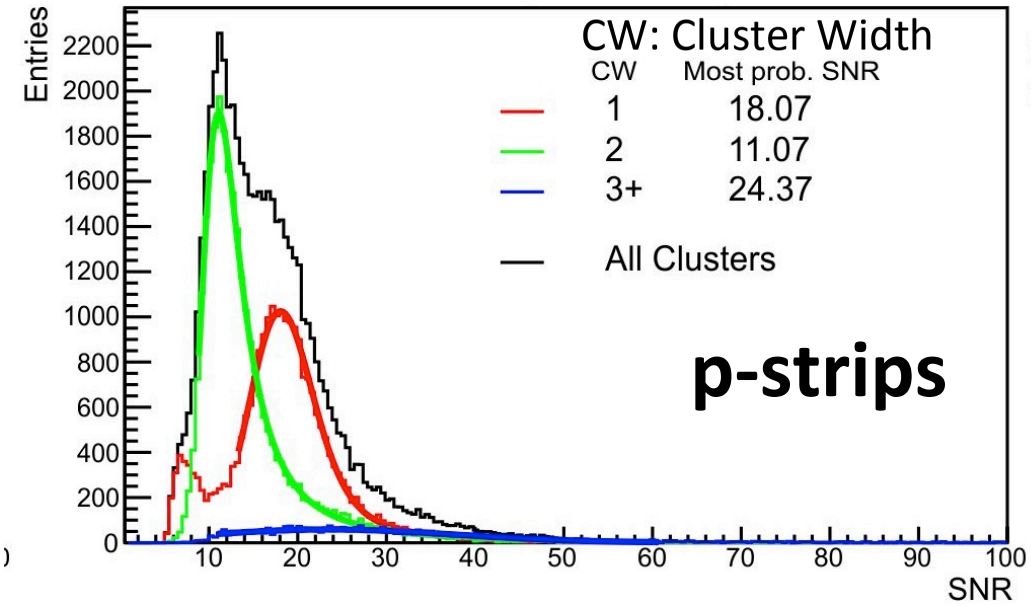


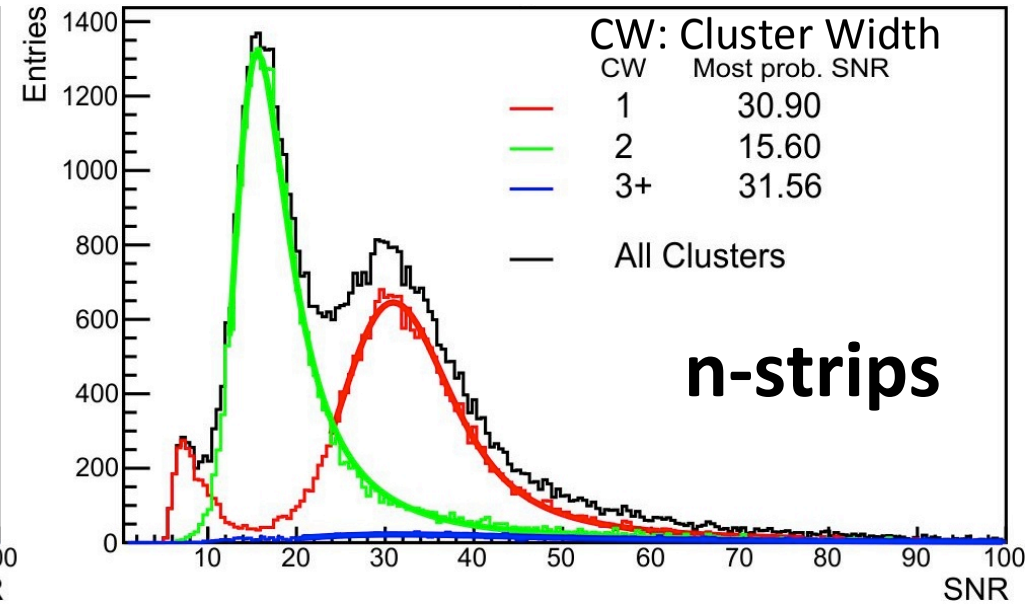
Beam test setup (@ DESY T24/1 hall)

- **Hadron beam (120 GeV/*c*) at CERN-SPS in Jun. 2015**
  - Test for a Layer-5 ladder.
- ***e*$^-$ beam (2-5 GeV/*c*) at DESY in Apr. 2016**
  - Test for ladders in all 4 layers (Layer-3 – 6).
  - SVD + PXD combined setup

SVD Ladder Performance (CERN-SPS results)

Signal-to-noise ratio (SNR) of a tested DSSD (O-Z)





- **SNRs in both p- and n-strips are well higher than 10.**

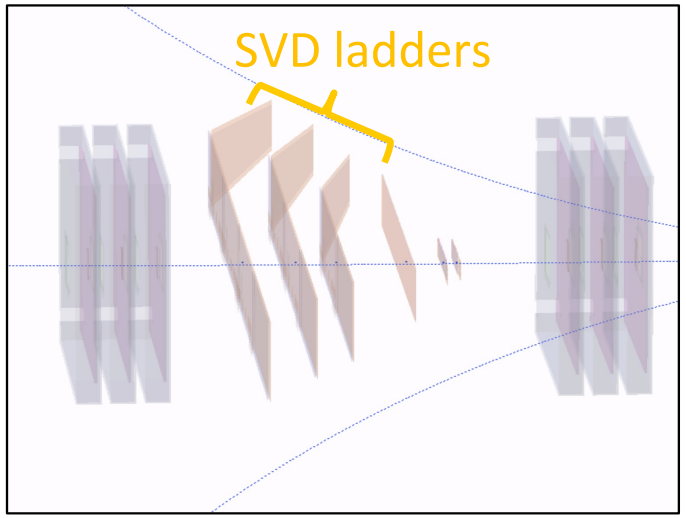
SNR before and after CO2 cooling (-20°C)

CW = 1	w/o cooling	w/ cooling
p-strips	18.1	21.1
n-strips	30.9	35.1

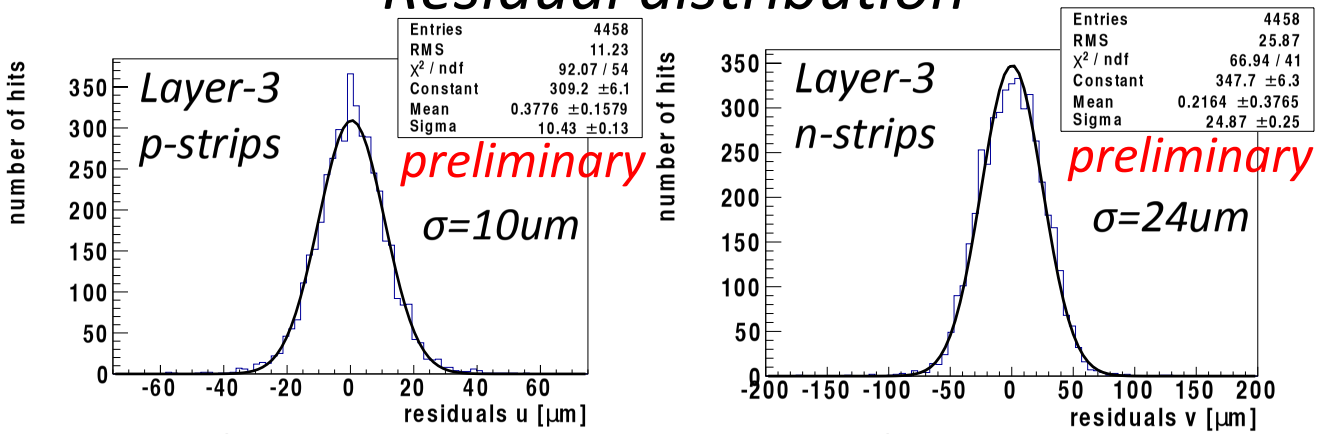
CO2 cooling improves the SNR

Ladder Performance for Tracking (DESY results)

Tracking event display



Residual distribution



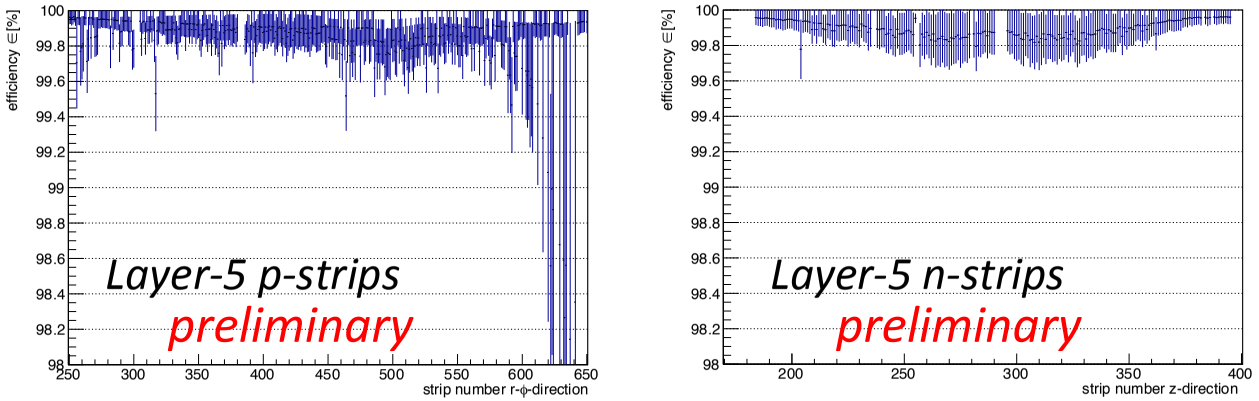
Observed good position resolutions.

They are consistent with our expectation.

- **Excellent SVD performance was confirmed from beam test data.**
  - **See more details in Thomas Lück's poster presentation.**

SVD analysis software development will be presented in poster session by Giacomo Caria.

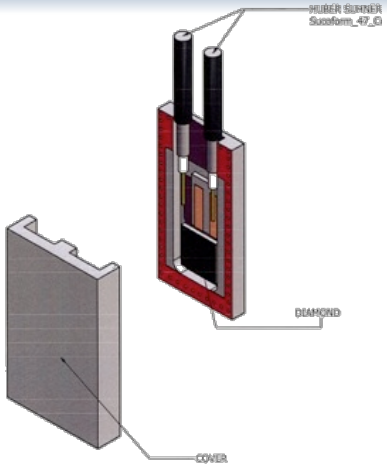
DSSD hit efficiency

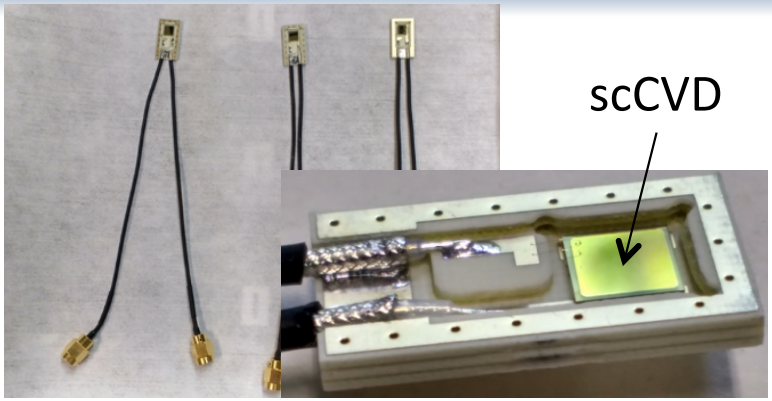


Excellent hit efficiencies more than 99%.

Radiation Monitoring for Beam Abort

- **Single Crystal Diamonds, scCVD 4.5x4.5x0.5 mm³**
  - High radiation tolerance
  - Small temperature dep.
  - Simple and compact detector structure
- **Current measurement with long high-quality cabling**





Prototype sensors are produced. They were tested in SuperKEKB beams.

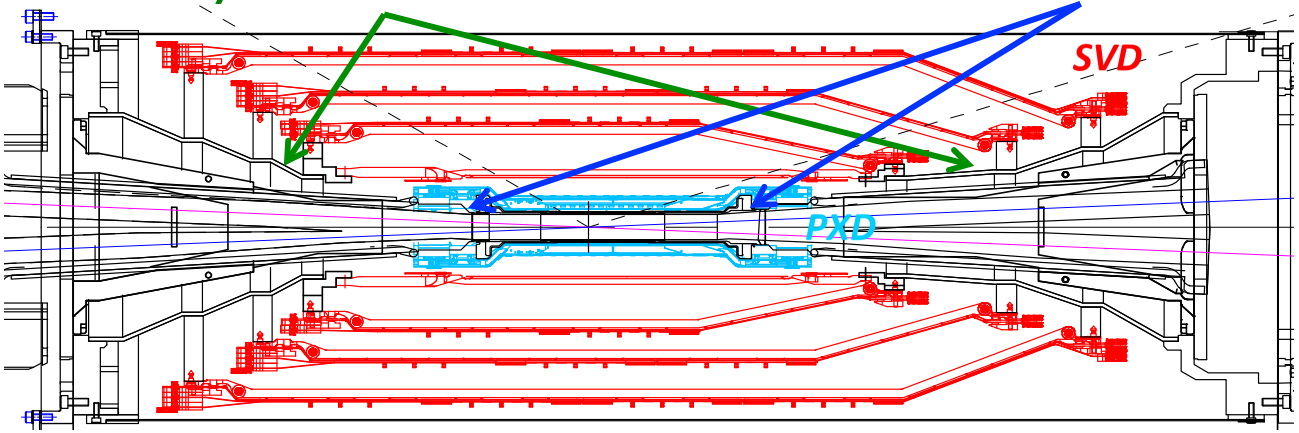
Installation locations

6 + 6 diamond sensors

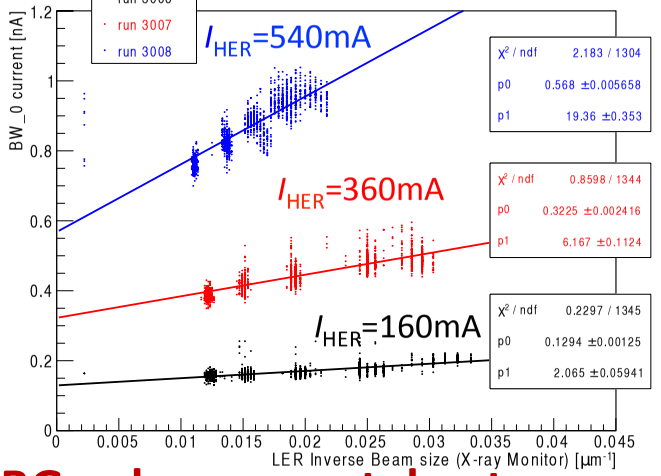
SVD Layer-3 and -4

4 + 4 diamond sensors

PXD-beam pipe



Hit counts vs. Beam size



BG enhancement due to Touschek effect was detected.

SVD Global Schedule

High Level Milestones	Date
Ladder mass-production	ON GOING
Start of SVD assembly at KEK	Feb. 2017
SVD readiness at KEK	Dec. 2017
Start of PXD+SVD integration	Dec. 2017
Start of VXD installation	Jun. 2018
Start of physics run	4Q 2018

Summary

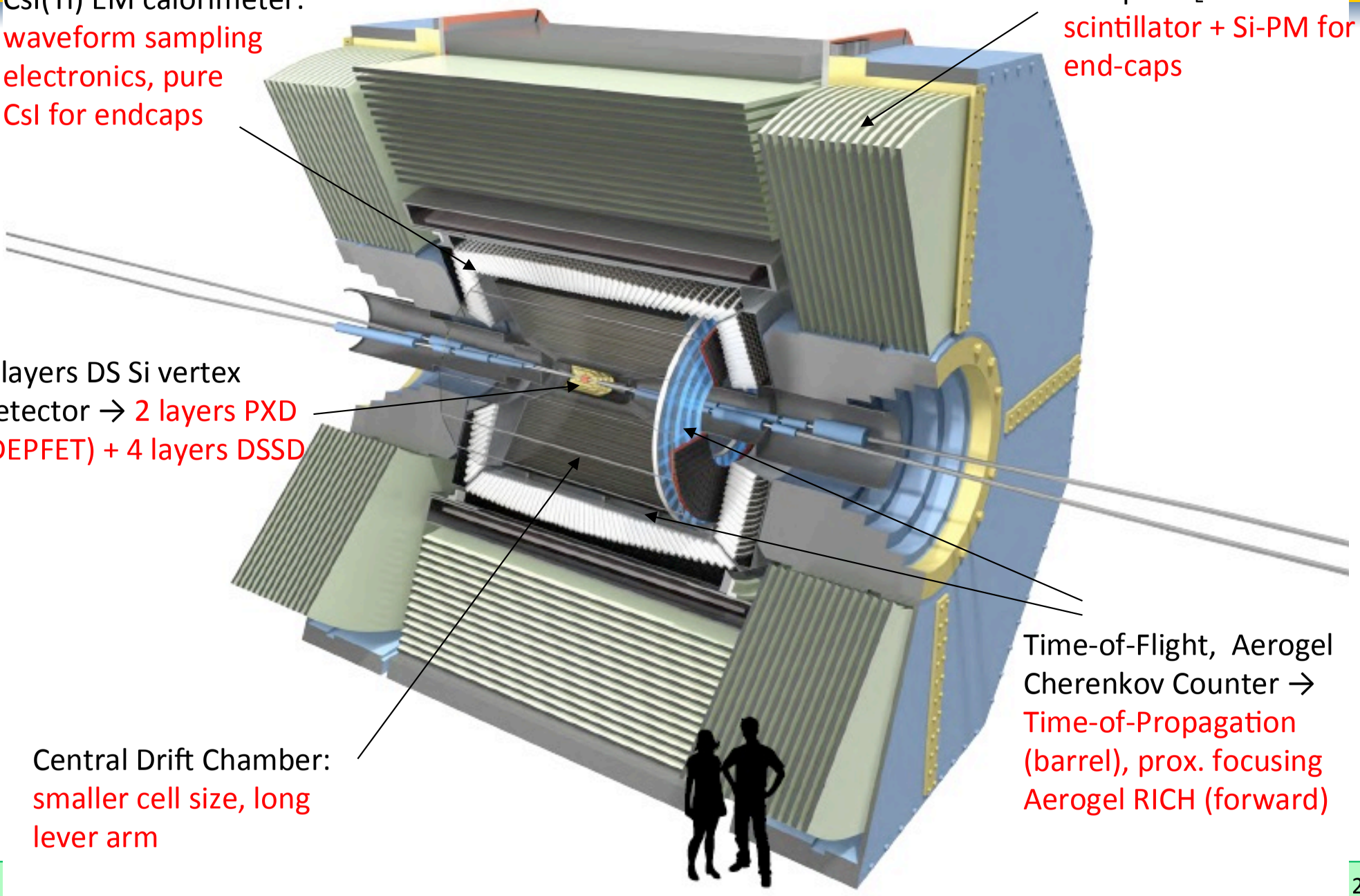
- **SVD, which is essential for the Belle II experiment, consists of 4-layer DSSD ladders.**
- **SVD ladder production**
  - The ladder mass-production at all assembly sites is on going.
- **SVD assembly at KEK**
  - All prototype tools were produced and reviewed.
  - This will be finalized by Feb. 2017 to start the SVD assembly at KEK.
  - The SVD assembly will be completed by Dec. 2017.
- **Performance study in beam test**
  - We obtained successful performances of the tracking, position resolution, and hit efficiency for final SVD ladders.

backup

Belle II Detector

CsI(Tl) EM calorimeter: waveform sampling electronics, pure CsI for endcaps

RPC μ & K_L counter: scintillator + Si-PM for end-caps



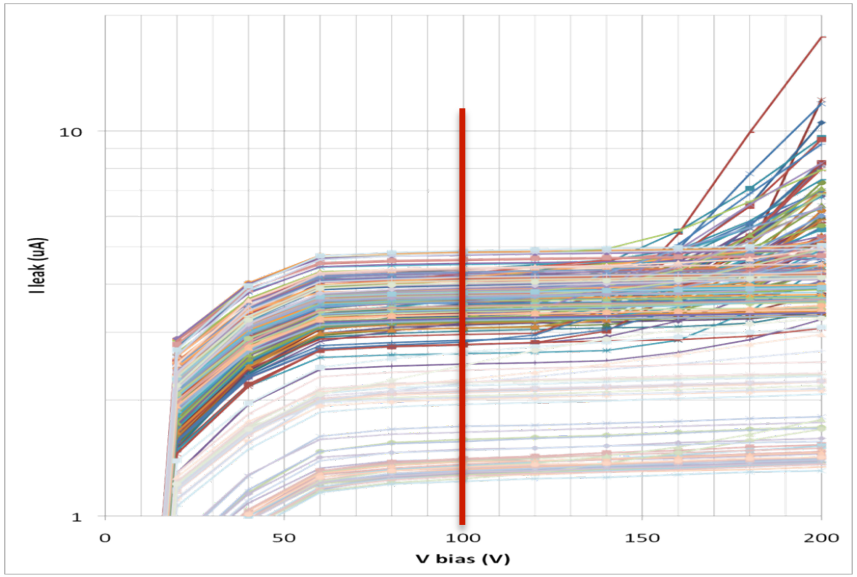
4 layers DS Si vertex detector → 2 layers PXD (DEPFET) + 4 layers DSSD

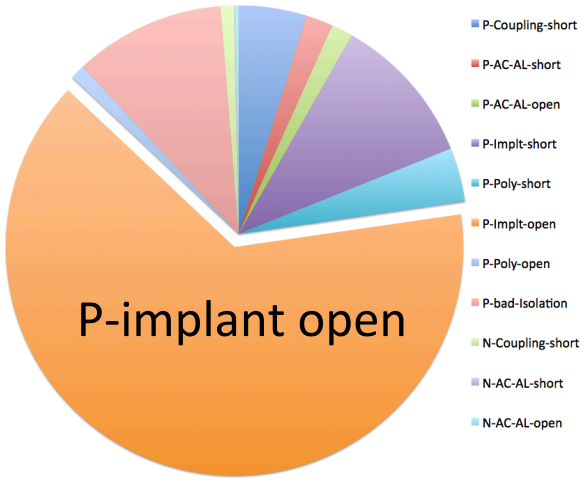
Time-of-Flight, Aerogel Cherenkov Counter → Time-of-Propagation (barrel), prox. focusing Aerogel RICH (forward)

Central Drift Chamber: smaller cell size, long lever arm

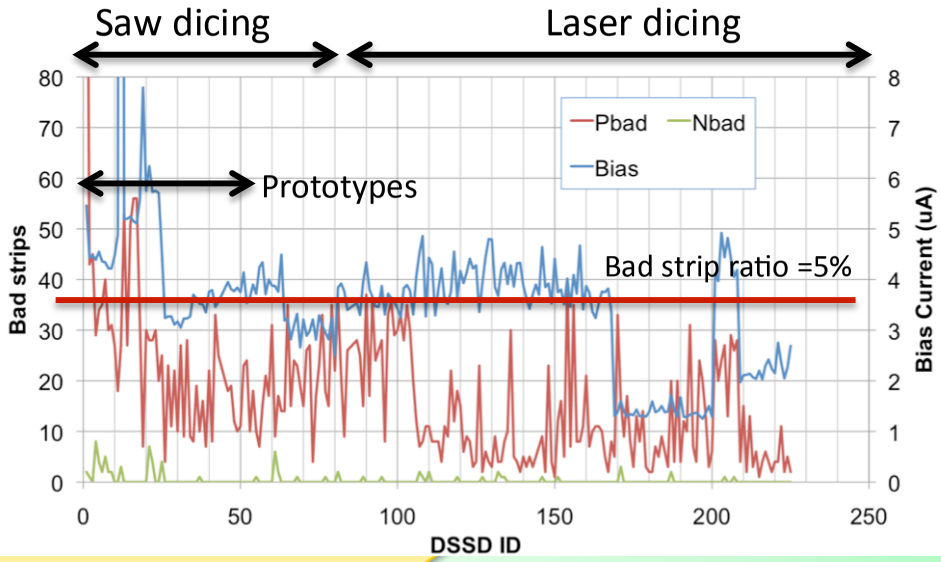
Rectangular sensors (HPK)

- **Small DSSDs**
  - Delivery of 24 pcs. scheduled for end of September
  - Two mechanical samples available
- **Large DSSDs:**
  - Production finished
  - 150 pcs in hand

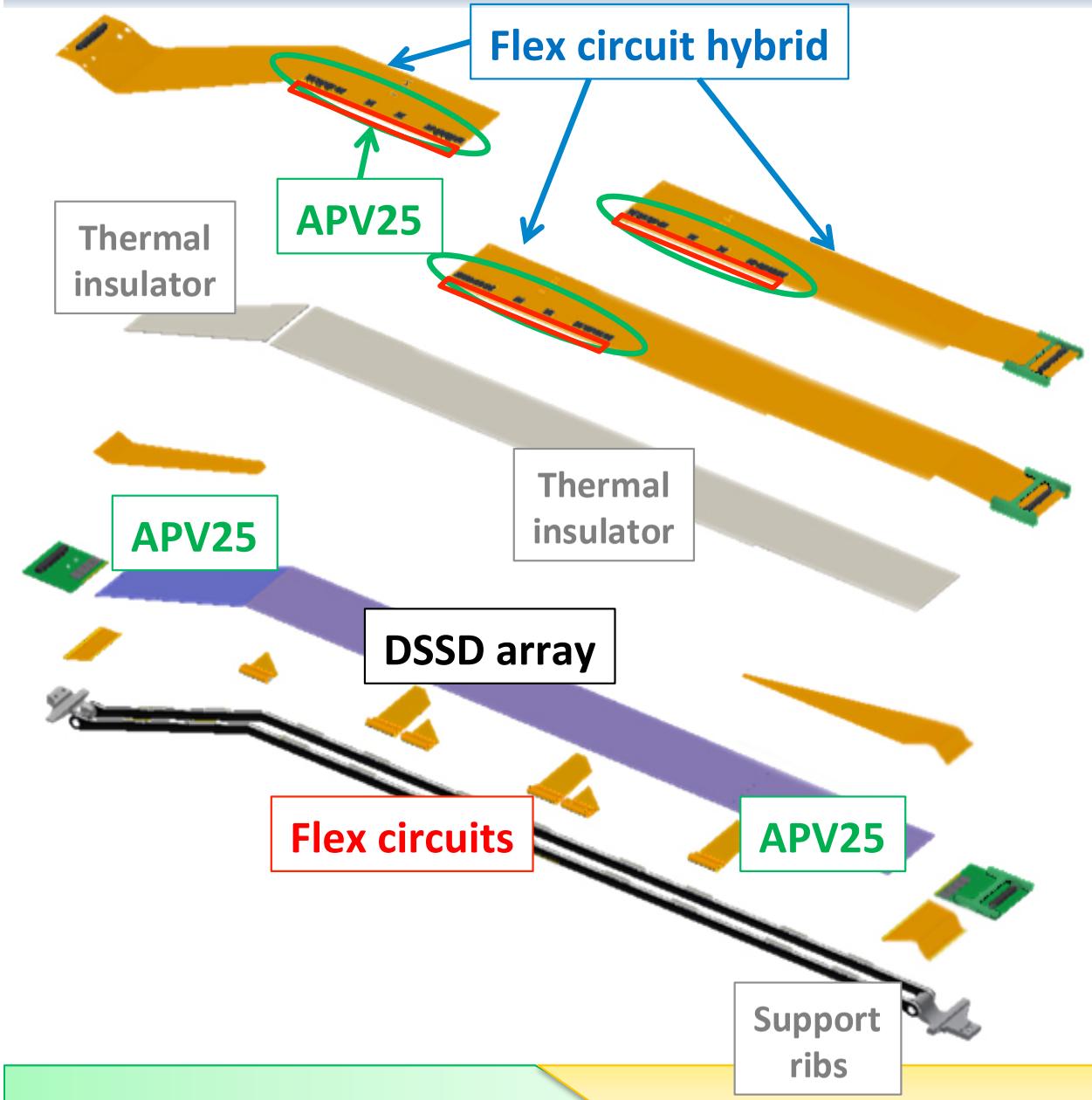




Classification of bad strips (ID>26)

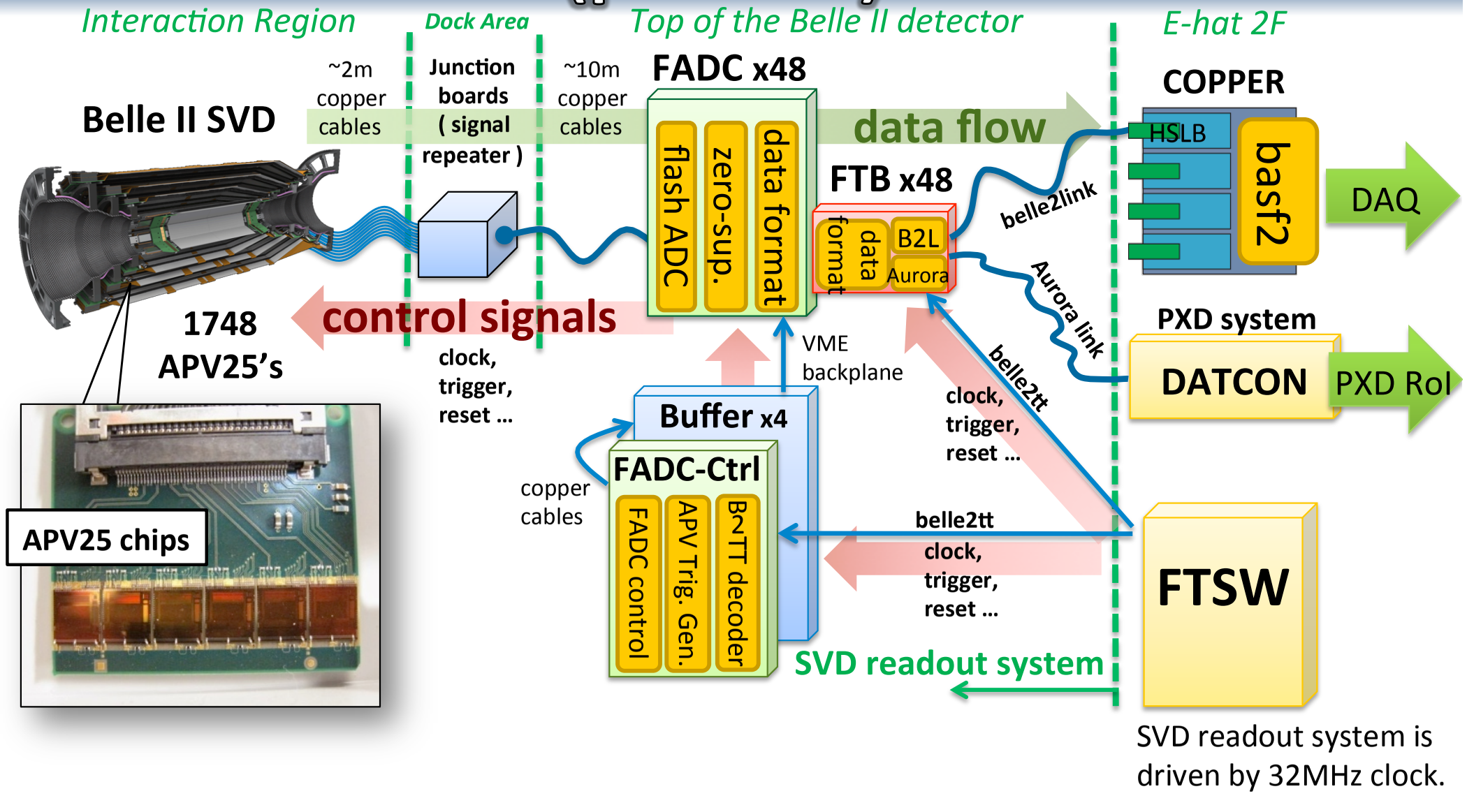


SVD Ladder Structure



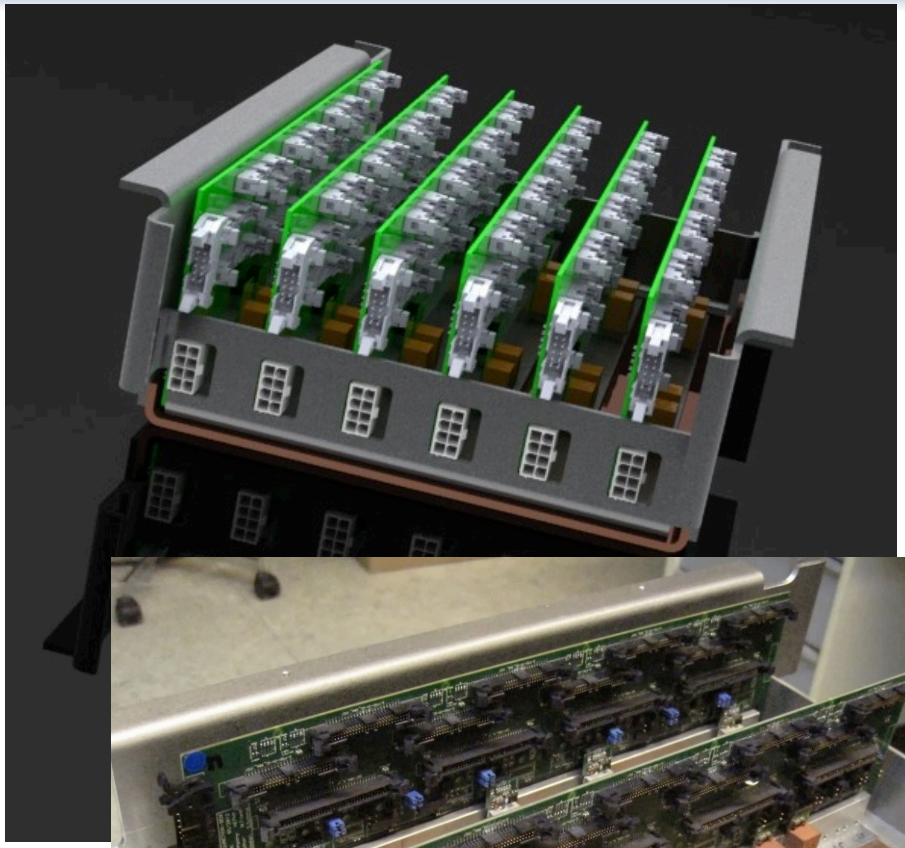
Layer	Institute
3	Melbourne (AUS)
4	TIFR India @ IPMU
5	HEPHY Vienna
6	IPMU Tokyo U
FW & BW	INFN Pisa

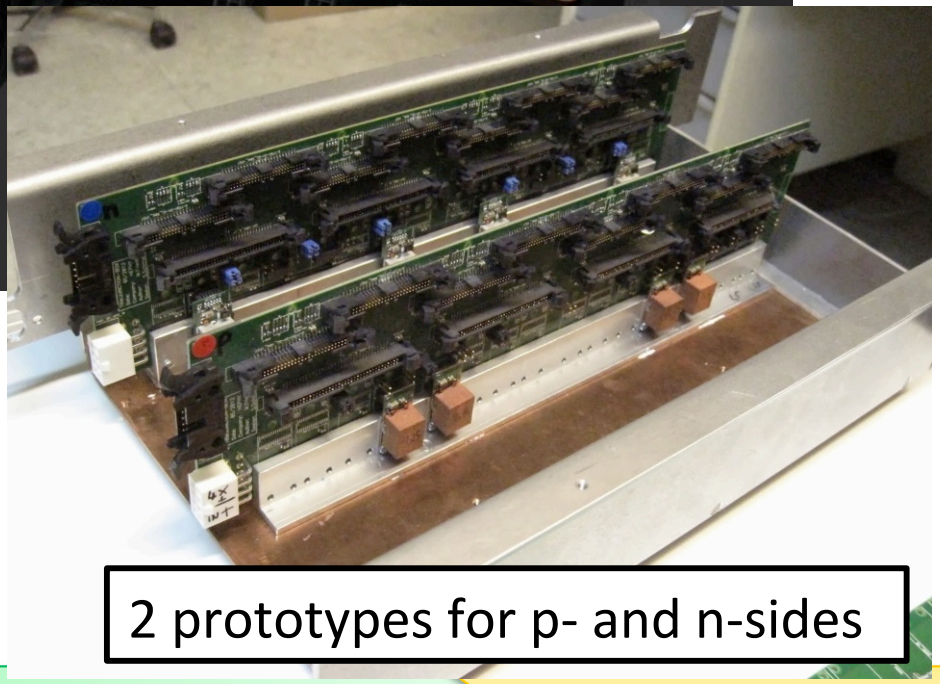
SVD Readout System Overview (phase-3)



SVD readout system is driven by 32MHz clock.

Junction box

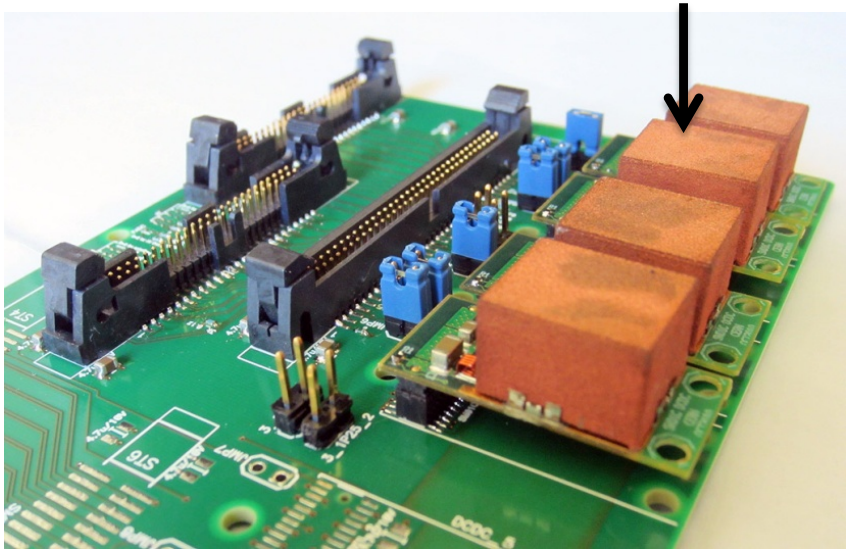




2 prototypes for p- and n-sides

- Supply HV and LV to DSSD and APV25.
  - DC/DC converter
- Joint signals between APV25 and FADC board.

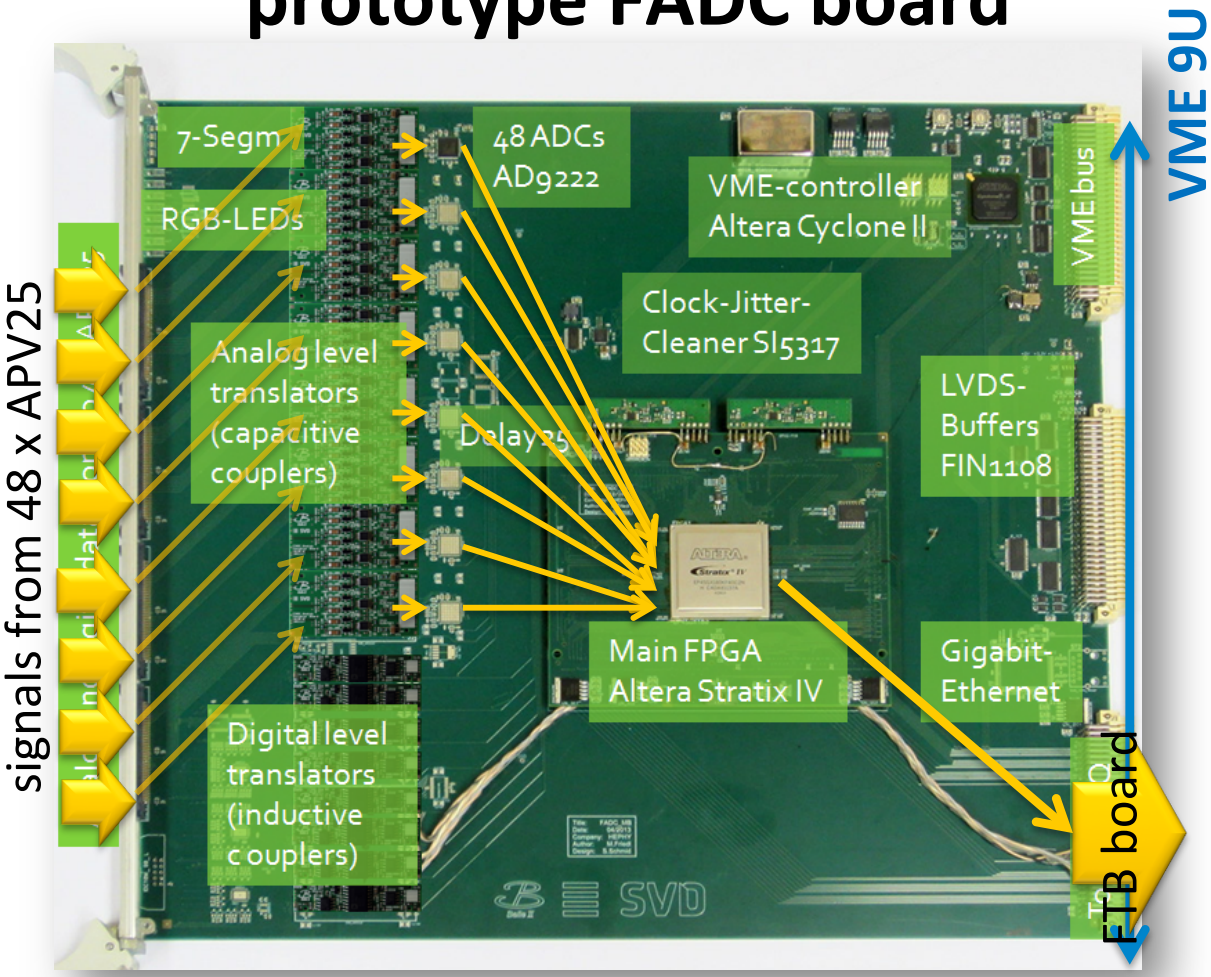
DC/DC converters



Development of Prototype FADC Board

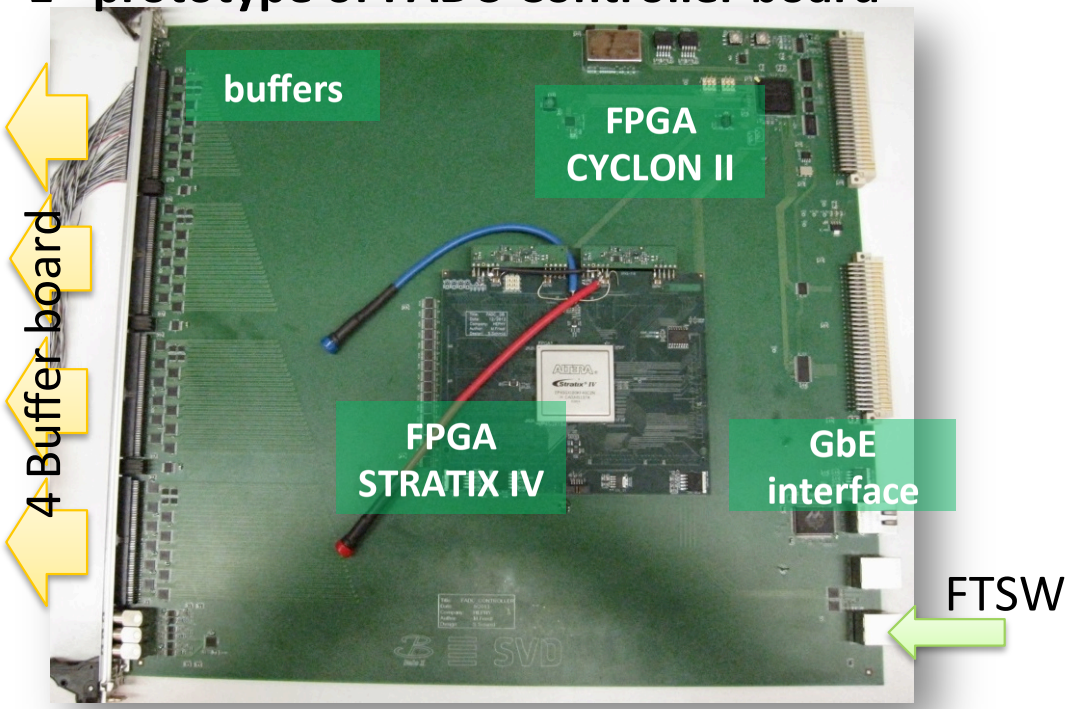
- **High signal density**
  - readout 48 APV25 outputs
- **APV25 signal processing on FADC**
  - analog level conversion (AC coupling)
  - 10-bit ADC
  - FPGA (Stratix IV) data processing
    - FIR filter
    - Common-Mode Correction
    - Zero-Suppression
  - data transmission to FTB

prototype FADC board

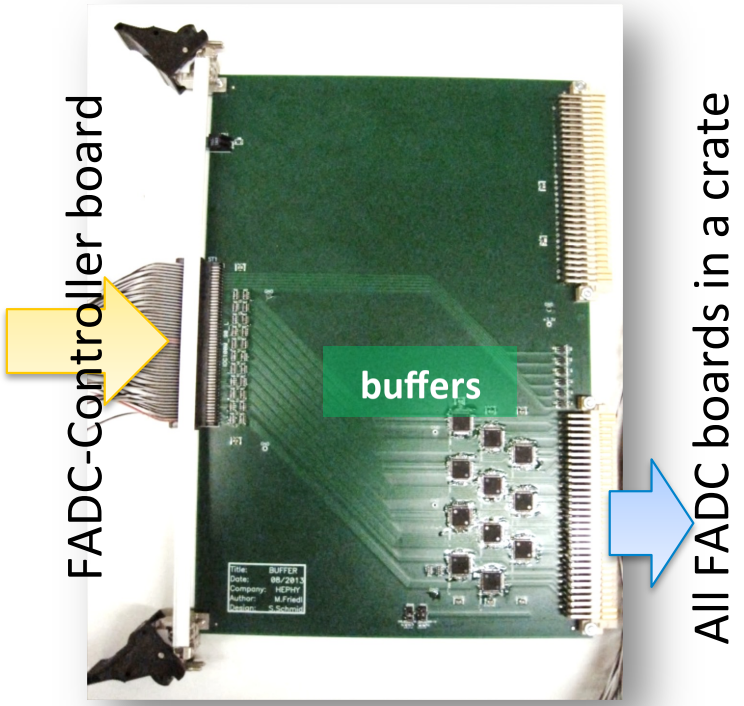


FADC-Controller and Buffer boards

1st prototype of FADC-Controller board



Buffer board



- **We will have 4 crates with FADC modules**
- **One has single FADC-Controller**
  - Receives FTSW signals
  - Distributes clock, trigger and other controls to all Buffer
- **Each crate has single Buffer module**
  - Receives FADC-Controller signals
  - Distributes signals to FADCs through backplane bus