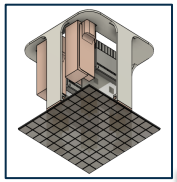
DS-20K DAQ&Trigger Status

Napoli, 20/7/2018

Marco Rescigno/INFN Roma1

DS20K DAQ Overview

PS Veto + S1&S2 Waveform readout



XX PSV + YY LAr PMT/ SiPM ?

Cryo

PE Receivers

Control Room

VETO r/o boards

Run Control

FIFO Full

O(10) Gbps

Trig & Daq

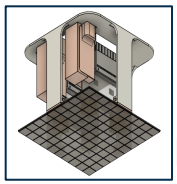
Event Builder and Trigger Farm

~50 Hz constant

Temporary Storage

30/500 MB/s (raw data, no compr.)

O(40 TB/day (raw data)



8210 PDM (Tile + FEB) ?? channels

Vessel +Cryo

Control Room

PE Receivers

O(30) Gbps

Timing Module

External Trigger Module

Permanent Storage (T2/T1)

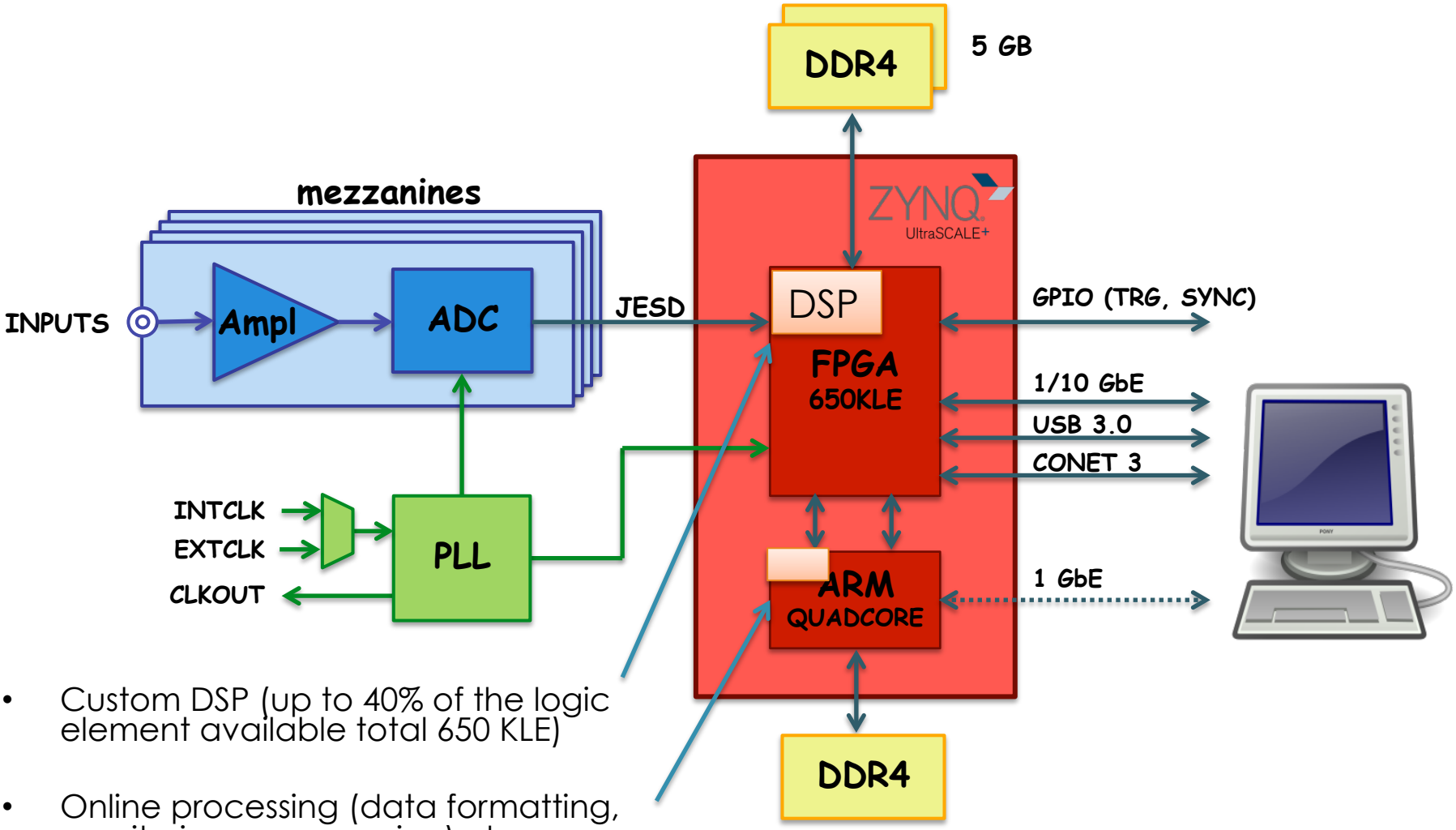
TPC r/o boards

GPS

He3 det.

Lasers

CAEN board architecture

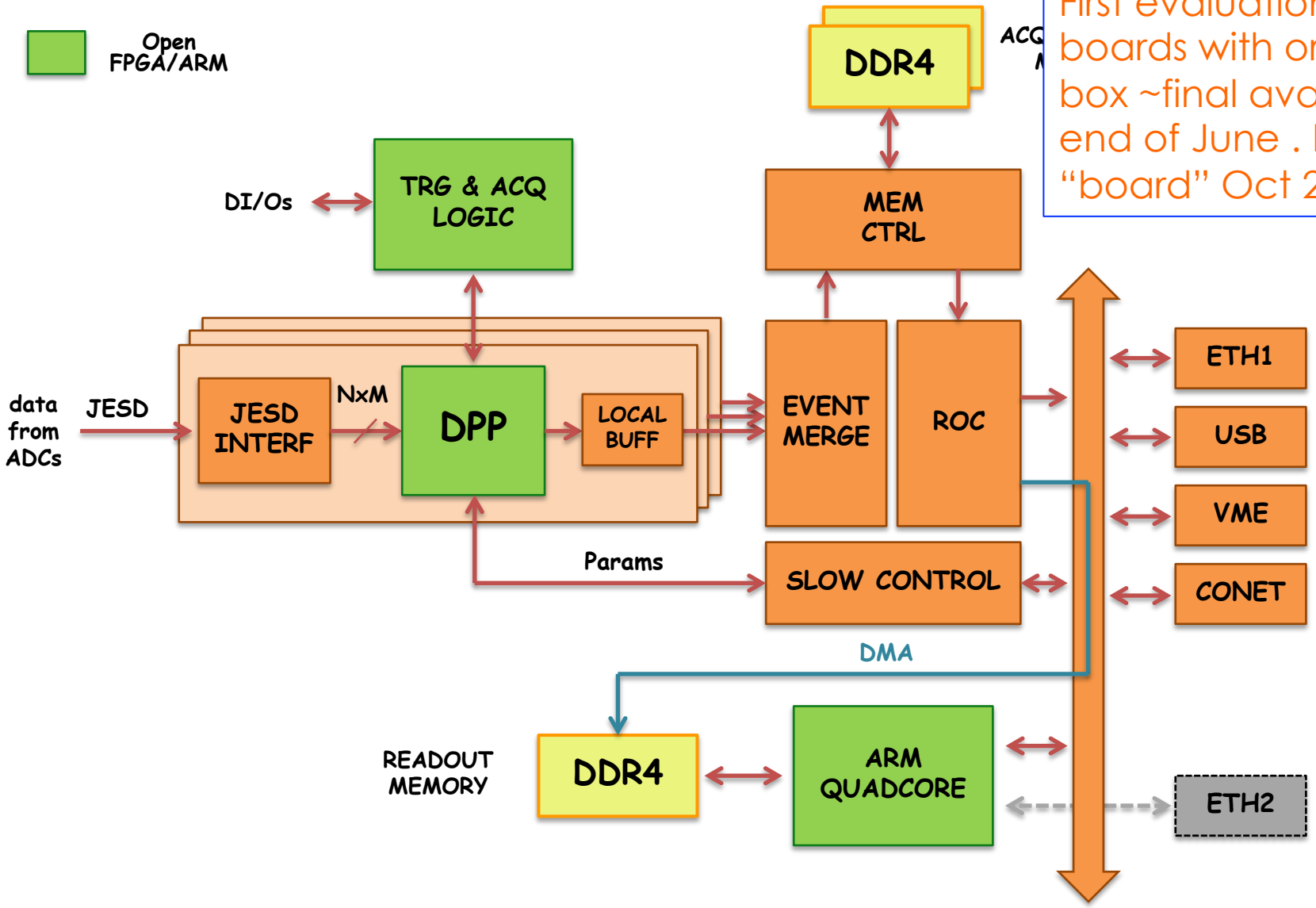


- Custom DSP (up to 40% of the logic element available total 650 KLE)
- Online processing (data formatting, monitoring, compression) also available on the Linux cores

CAEN digitizer update

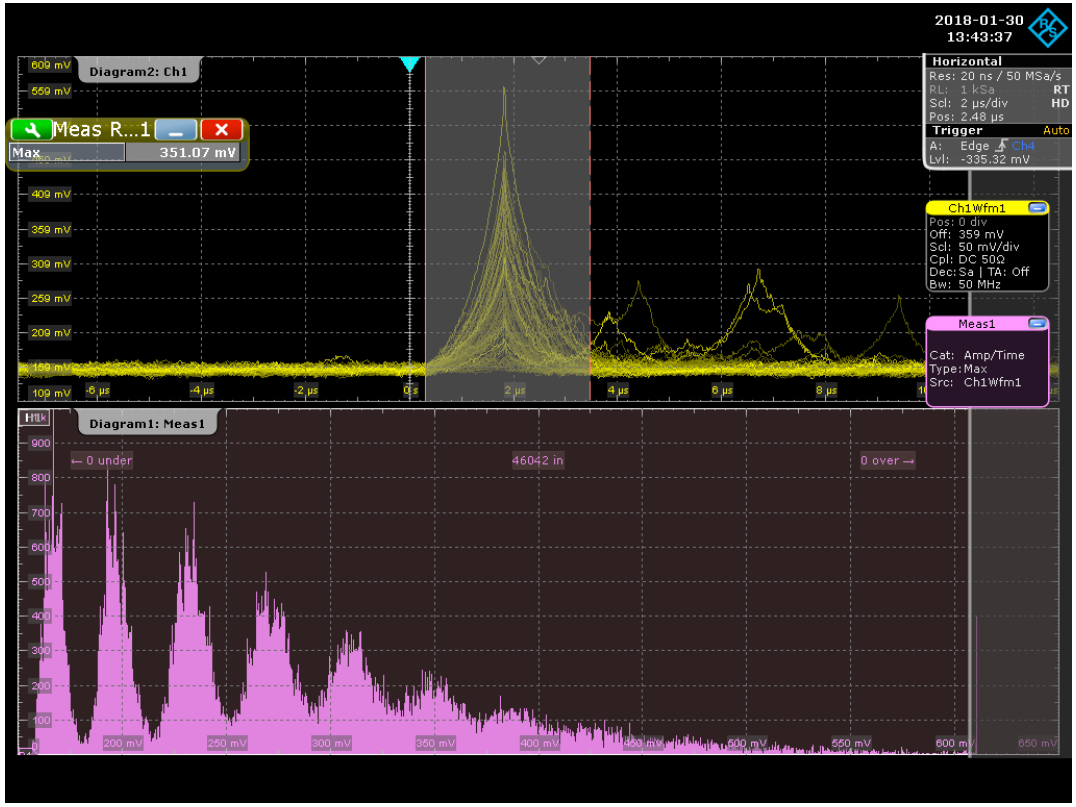
- Meet with CAEN team end of May
  - Steady progress reported on firmware/software/board design
  - ADC choosen → 14 bit/125 MHz
  - Integration of an ADC unit within an evaluation board for the FPGA done
  - Implemented JESD high speed interface b/w ADC and FPGA
  - Most of the pieces into place → will need to proceed with DS specific implementation
- Man power limited so far from our side (later)
- First evaluation board available now (two channlel and same FPGA)
- By IEEE Nuclear Science Symposium and Medical Imaging Conference (NISS/MIC) Sidney, 9-17 November the board would be in the catalog → can be aquired within the INFN Accordo Quadro

FPGA Block Diagram



Status of DSP

Bologna, LNGS



DSP algorithm tested on real SiPM tiles for 1 channel on a RedPitaya…
LNGS (+GSSI soon) group studying several alternatives compatible with h/w resources. Encouraging result, no final report yet

Implementation in firmware on the real device will be done from September

DSP to do

- Need to implement/tune S2-like algorithm
- Need to test using realistically simulated pulses and study performances
  - What happen for photons falling on the same tile within O(1 us) (overlap)?
  - How to tune the algorithm, what is the window of the digitized waveform to be saved
  - How to set threshold ? What parameters should be set
- Trigger logic for a given board can be foreseen, useful?

Including the VETO

- Several exercise done to understand the impact of the new VETO design on the DAQ design
- According to the different hypothesis it could be a simple expansion of the TPC system or something with a profound impact
- From the point of view of the share of the capital cost the h/w would be mostly a Canadian contribution.
- Impact on the event/builder and software trigger (CSN2) may also be important, but at this point difficult to quantify

Readout Channel Reduction

Pros

- Reduction in complexity of penetrations
- Reduced number of fibers and optolink to handle
- Reduced readout channel in daq/offline

Contra

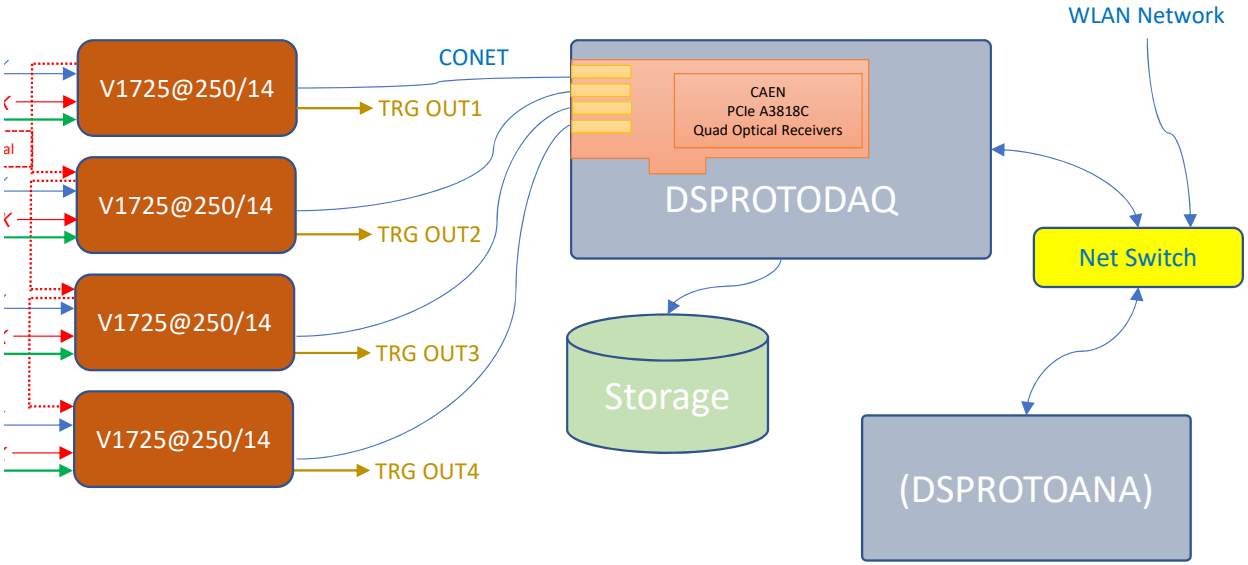
- Trade-off between SiPM performance parameters should be studied with simulation
- 5x5 MB may not be optimal for every ganging scheme

2018/2019 Milestones

- At the end of 2018 we want to read-out 50 PDMs in DS-proto → MIDAS/ DEAP like daq from TRIUMF group
- At mid (April) 2019 we need a revamp of MIDAS to use new digitizer board from CAEN
- Later in the year a system running on the 370 channel DS-proto with the new board integrated

DEAP like readout for DS-proto

Pierre Andree Amaudruz

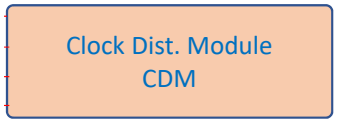


Applications running on DSPROTODAQ

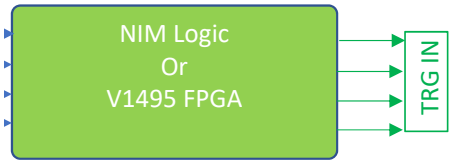
Midas frontend: V1725 readout
Midas data server (mserver)
Midas web server (mhttpd)
Midas data logger (mlogger)
Midas data monitor (mdsproto, root base

Applications running on DSPROTOANA (o

Root
Online/Offline data analyzer (root based)
Custom package



Clock sync. option
- From V1725 (internal)
- From CDM (external)



Trigger option
- NIM logic including Veto (S1, S2)
- V1495 FPGA (requires NIM for S1, S2)

System:
- Up to 64 input (including Veto)
- Midas event composed of data collecte trigger generation.
- Each event composed of 4 Midas bank
- Each bank is dedicated to a HW modul
- Each bank is composed of ZLE fragmen

- HW clock Sync.
- Timestamps across banks are checked

ZLE encoding format

EVENT DATA FORMAT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
CHANNEL EVENT SIZE																																HEADER
EVENT TRIGGER TIME TAG																																
BASELINE VALUE																																

0	0	NUMBER OF SKIPPED SAMPLES (N_{S0}) * 8		
1	1	SAMPLE 2 (ROI 1)	SAMPLE 1 (ROI 1)	SAMPLE 0 (ROI 1)
1	1	SAMPLE ... (ROI 1)	SAMPLE ... (ROI 1)	SAMPLE ... (ROI 1)
1	1	SAMPLE J (ROI 1)	SAMPLE J-1 (ROI 1)	SAMPLE J-2 (ROI 1)
0	0	NUMBER OF SKIPPED SAMPLES (N_{S1}) * 8		
1	1	SAMPLE 2 (ROI 2)	SAMPLE 1 (ROI 2)	SAMPLE 0 (ROI 2)
1	1	SAMPLE ... (ROI 2)	SAMPLE ... (ROI 2)	SAMPLE ... (ROI 2)
1	1	SAMPLE K (ROI 2)	SAMPLE K-1 (ROI 2)	SAMPLE K-2 (ROI 2)
...				
0	0	NUMBER OF SKIPPED SAMPLES (N_{Slast}) * 8		

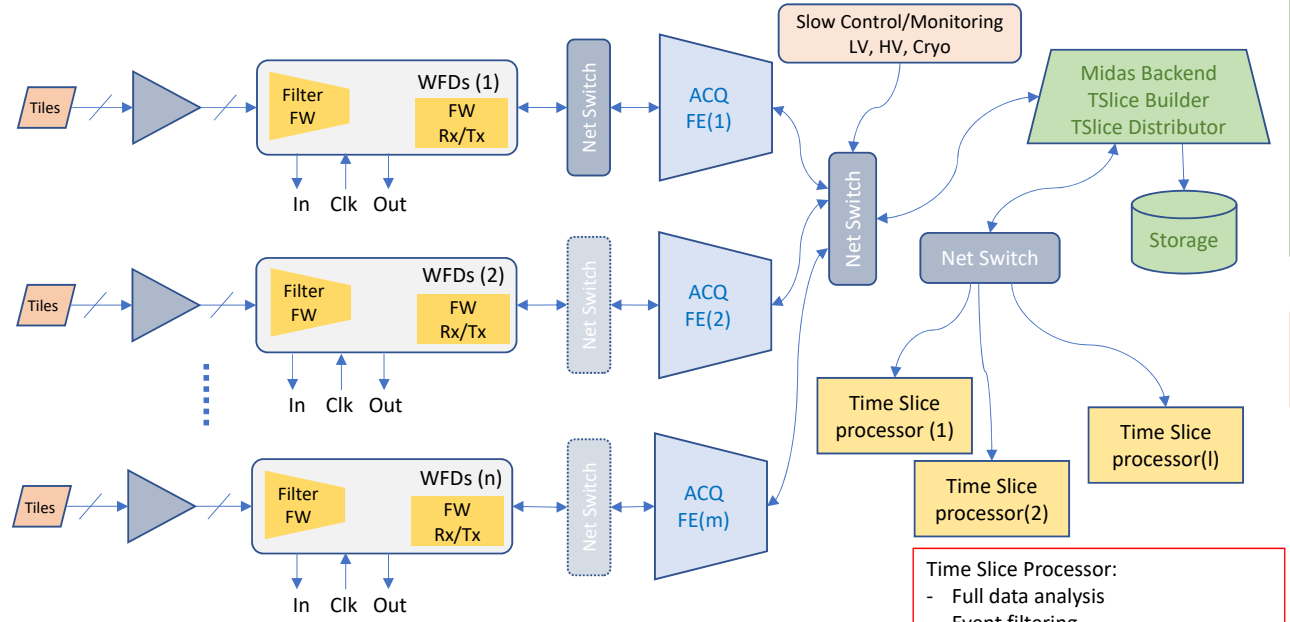
EVENT DATA

- Could reduce a factor 10 if samples of 20 us width are saved and #npulses ~5
- Decide soon, should procure h/w and have the TRIUMF group work on is before moving the setup to CERN

DS-proto DAQ with new boards

Pierre Andree Amaudruz

Initial DAQ Architecture proposal for DS, from April'19 -



Midas Backend:
- HW configuration
- Run control
- Fragment collector
- Time slice builder based on fragment feature (variable time slide)
- Time slice distribution
- DAQ monitoring
- Data logging

Other system Required:

- Experiment DB

Time Slice Processor:
- Full data analysis
- Event filtering

- *To be specified: Data logging*

FW:
- HW monitoring
- Filter algorithm
- Data transmission
- HW WFD feature extraction

ACQ FE:
- WFD Acquisition
- Time sorting
- Fragment feature extraction

DSP for Proto

- The foreseen DSP would work for DS-proto
- Should use simple waveform recording firmware and try S1/S2 discrimination for data reduction..
- Still, will be able to trigger efficiently on noise hit (differently that with regular digitizer in the first phase)
- Will be limited by data logging rate. Need to introduce specific h/w or s/w triggers to select most useful data.

Evolution scheme

- Need to adapt MIDAS frontend to include an acquisition front-end handling a connection from one/more boards
- Need to include and connect within a MIDAS a smarter Event Builder and then an Event reconstruction/filtering process
- This has strong ties with software framework for Event reconstruction !
  - In principle we want to have prompt online reconstruction for monitoring/event classification/logging using the same algorithm as in the offline
  - Will also greatly reduce the resource needed for offline

Further milestones

- Beyond step 1 and 2 discussed so far, we will need
  1. Ds-proto phase 1 : DEAP-style daq deployment for 50 channels (by end 12/2018)
  2. Ds-proto phase 2 for 50 channels: New board imply revamping MIDAS and a new event builder (by 6/2019)
  3. Ds-proto phase 2 for 370 channels: expand system, add online monitor start 6/2019, timeline to be connected to DS-proto completion
  4. Ds-proto operations in LNGS: 2020 (?) to be defined
  5. Partial system implementation in LNGS: include cabling, infrastructure, DB, GPS and other features, capability to test TPC in the test dewar (2020/2021?)
  6. Final implementation

Available man-power

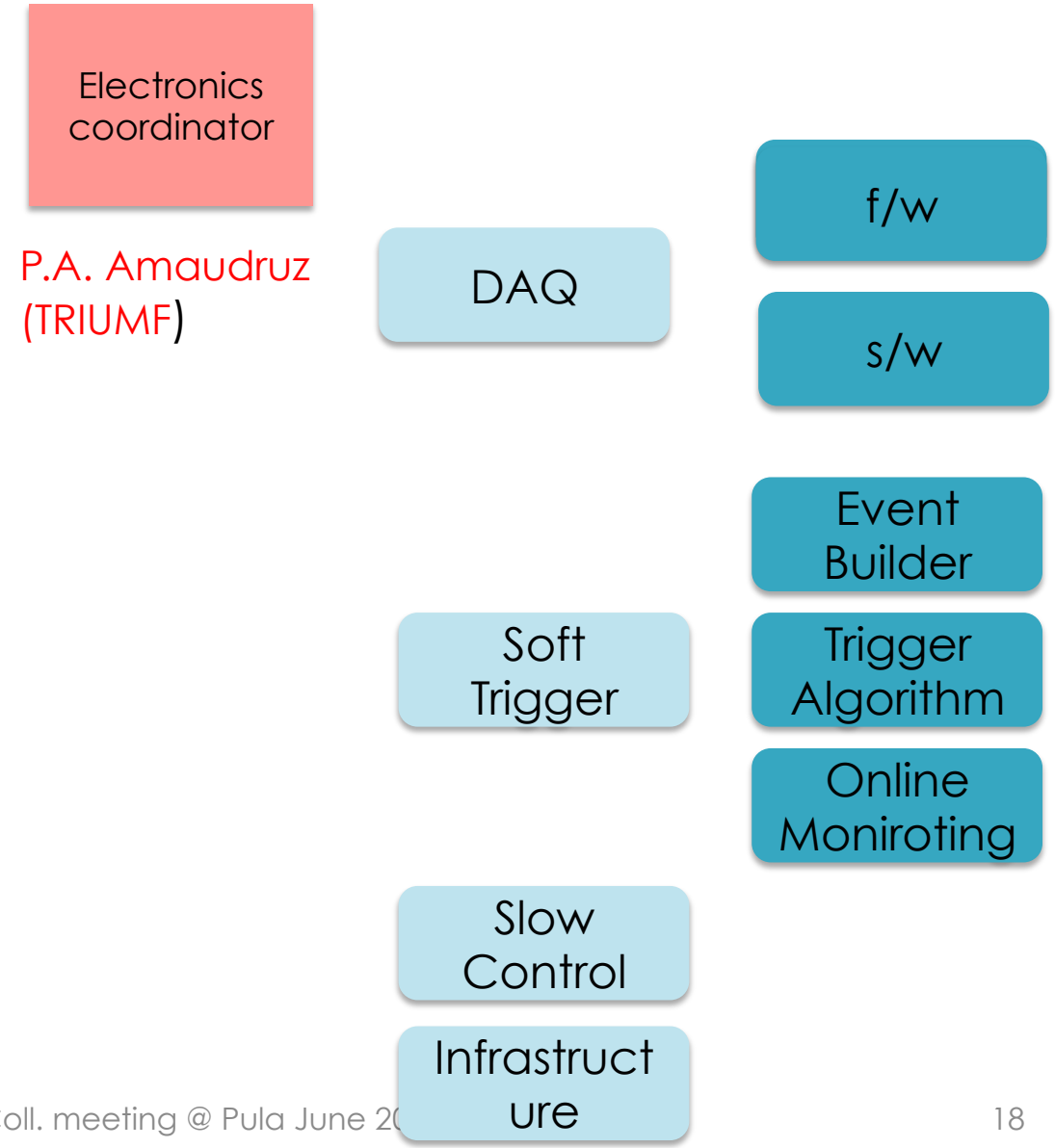
- TRIUMF group includes several permanent physicist and have requested support from the director for software and firmware engineers on the project. Response is positive, we have already met with Thomas Lindner who will be in charge together with Pierre-Andree Amaudruz of the MIDAS porting for DS-proto and the further evolution to accommodate the new readout scheme for DS20k. A firmware expert also available sometime later this summer.

- The Rome group will maintain the responsibility for the software trigger. Andrea Messina has significantly increased his participation to DarkSide and joined the effort.

- The new group at GSSI with the help from Alessandro Razeto is planning a major involvement both in the firmware development and in the DAQ software and trigger algorithm. Several people student, post-doc, senior will be part of the team.

New Group Structure

- DAQ task will have oversight both in the integration of the digitizer board in the system and related f/w evolution (in connection with CAEN) and on the software part providing basic readout functionality and all the services already available in MIDAS



New Group Structure

- Soft Trigger task will oversight the implementation for event building and identification from the hit fragments in time slices provided by the DAQ, the study and implementation of a full event reconstruction and trigger selection and provide a way to monitor online data with key performance parameters based on full reconstruction

Electronics coordinator

P.A. Amaudruz (TRIUMF)

DAQ

f/w

s/w

Event Builder

A.Messina (RM1)

Soft Trigger

Trigger Algorithm

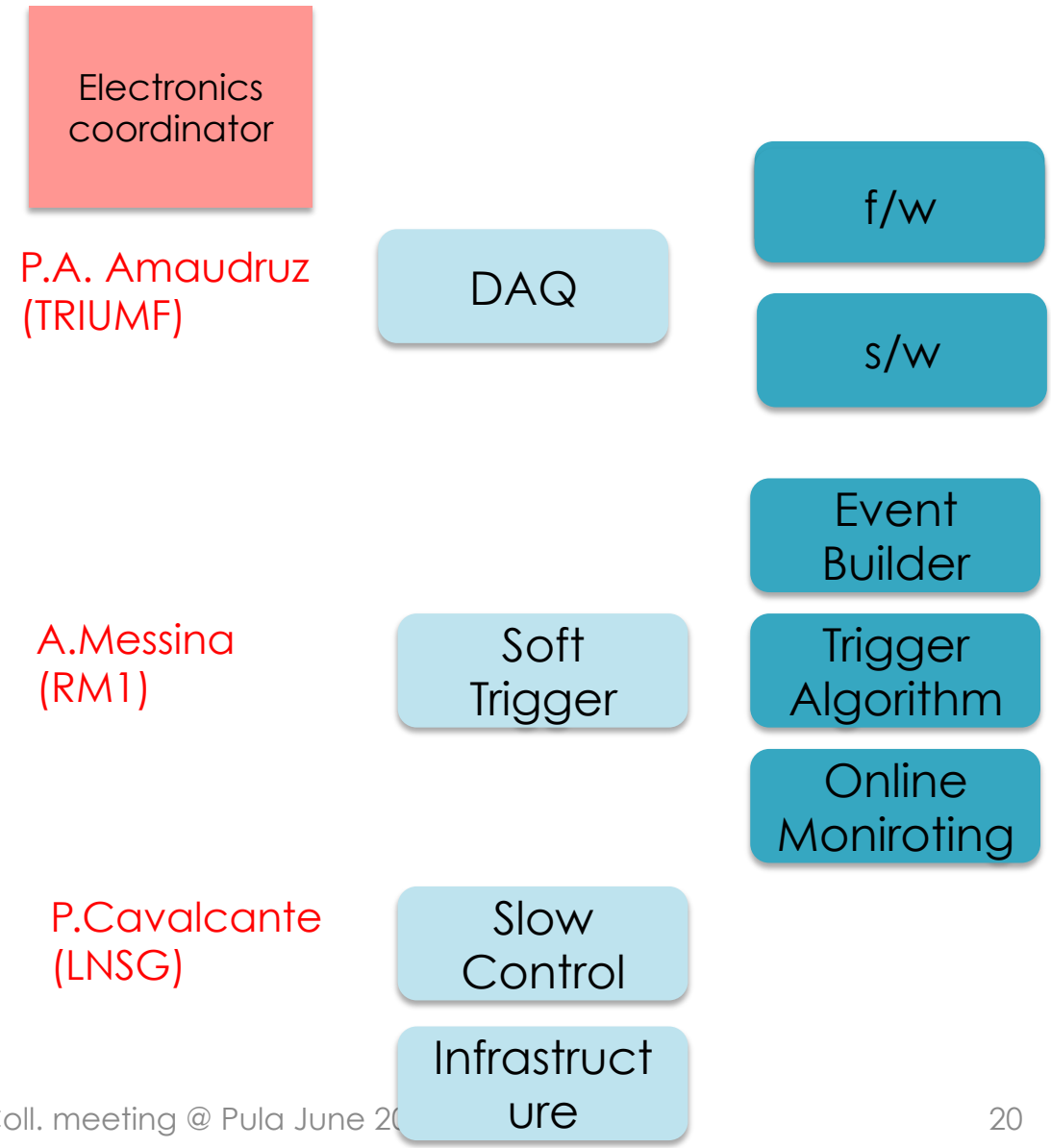
Online Moniroting

Slow Control

Infrastructure

New Group Structure

- Slow Control task is responsible to deploy the hardware for cryogenics control and other key control checks and provide monitoring data to MIDAS though e.g. an OPC service interface
- Infrastructure coordination will need to oversight at control room/ electronic room building including all services and need to interface with the main infrasctructure group of DS20k



WBS 1.06 & 1.9.2
PREVENTIVI 2019

Development of a DS digitizer

LNGS

APPARATI	1. 1.6.1.3 Digitizer per DAQ development 2 schede	25.00
	2. 1.1.7.2.2 + 1.1.5.1.12 Procurement of fiber bundles for the prototype 5x17 k€	85.00

- Two prototype boards on 2018 budget (RM1), one will be in use @ TRIUMF/CERN the other at RM1/CERN
- The new group at GSSI plan to contribute to algorithms at both the firmware and software level. Request to finance a test stand at GSSI with 1/2 new digitizer boards
- Saturate WBS line **1.6.1.3** (Prototype boards)

Trigger & Event Builder

- GSSI + RM1

LNGS

INVENTARIO	1. 30 TB storage for SiPM/PDM characterization & testing (waveforms)	6.00
	2. Riparazione dewar	3.00
	3. 1.6.2.3 Cluster per smart trigger/data reduction	20.00

- RM1 group so far worked on inherited resources from previous projects
- Will be heavily involved in DS-proto DAQ and tests and use that as a test-bed for integration within the MIDAS s/w of the new proposed readout scheme
- In parallel, a prototype trigger farm will also be deployed at GSSI with the specific goal of implementing algorithm for trigger and data reduction for DS20k – not present specifically in WBS, included now
  - Given the time line of DS20k construction the bulk of the procurement for the trigger farm will be required in late 2021. Unwise to rely for DS20K on CPU purchased in early 2019

DS-Proto Server/Slow Control

RM1

	-- Nuova voce -- Caratteri rimanenti: 280			+		
INVENTARIO	6+1 schede 64 ch per full readout Prototipo [WBS 1.6.1.1.1] Caratteri rimanenti: 221	90.00	0.00		Set	-
	Completamento Slow Control [WBS 1.9.2.3] Caratteri rimanenti: 240	5.00	0.00		Set	-
	DAQ Server per Prototipo [WBS 1.9.1.2] Caratteri rimanenti: 241	10.00	0.00		Set	-
	Storage dati Prototipo (100 TB) Caratteri rimanenti: 249	20.00	0.00		Set	-
				125.00 0.00		

- In 2018 5k for a server allocated. Will be ok for the 50 channel readout. Need more CPU and temporary disk space for the full, 370 ch readout.
- Longer term plan for DS-proto imply also need to have separated system for development/test/integration for Ds20K @ GSSI and RM1
- Some disk space for long term raw-data and reconstructed data storage of Ds-Proto is also needed (not included in WBS so far). Propose to have resources for 100 TB of data available at CERN or elsewhere

DS-Proto digitizer for 370 ch readout

RM1

	-- Nuova voce -- Caratteri rimanenti: 280			+		
INVENTARIO	6+1 schede 64 ch per full readout Prototipo [WBS 1.6.1.1.1] Caratteri rimanenti: 221	90.00	0.00		Set	-
	Completamento Slow Control [WBS 1.9.2.3] Caratteri rimanenti: 240	5.00	0.00		Set	-
	DAQ Server per Prototipo [WBS 1.9.1.2] Caratteri rimanenti: 241	10.00	0.00		Set	-
	Storage dati Prototipo (100 TB) Caratteri rimanenti: 249	20.00	0.00	125.00 0.00	Set	-

- To fully equip DS-proto need 6+1(spare) 64 ch board (if tests successful on the first prototypes already foreseen in 2018 budget)
- Longer term plan for DS-proto imply also imply this to be a separate budget line in WBS distinct from the procurement of digitizers for DS20k

FOR BACKUP

"Typical" needed throughput

Warning: Typical means in the typical DM signal range! Working on a detailed simulation to ascertain the average rate…

	TOTAL AGGREGATE DATA INTO EVENT BUILDER (EB) OR STORAGE (DISK/TAPE)					EB	DISK	TAPE
	NOISE HITS		SIGNAL HITS		Packet Size			
	Assumption	Total (kHz)	Typical	Total (kHz)	(B)	(Gbps)	(MB/s)	(TB/day)
S1	250 Hz x 8280 channels	2070	500 Hits x 50 Hz	25	8	0.13	2.7	0.23
S2	N/A	0	4000 Hits x 50 Hz	200	206	0.33	41.2	3.56
VETO	250 Hz x 1000 channels	750	Negligible?	0	8	0.05	0.2	0.01
						0.5	**44.0**	**3.8**

Typical = DM range of interest

Assume 100 mHz/cm2 (best achieved 5 mHz/cm2)

Assume 50 Ton active Ar39 (35 Hz) + 15 Hz other (tbd)

Assume ganging 100 mHz/cm2 * 3

Lack other radioactivity ?

Assume 0.5 ms veto capture window

	TOTAL AGGREGATE DATA INTO EVENT BUILDER (EB) OR STORAGE (DISK/TAPE)					EB	DISK	TAPE
	NOISE HITS		SIGNAL HITS		Packet Size			
	Assumption	Total (kHz)	Typical	Total (kHz)	(B)	(Gbps)	(MB/s)	(TB/day)
S1	250 Hz x 8280 channels	2070	500 Hits x 50 Hz	25	1256	21.05	421.4	36.41
S2	N/A	0	4000 Hits x 50 Hz	200	206	0.33	41.2	3.56
VETO	250 Hz x 1000 channels	750	Negligible??	0	1256	7.5	23.6	2.03
						28.9	**486.1**	**42.0**

Assume 0.5 ms veto capture window

Typical=50 keVee

Max TPC data streaming to EB for 64 ch. =

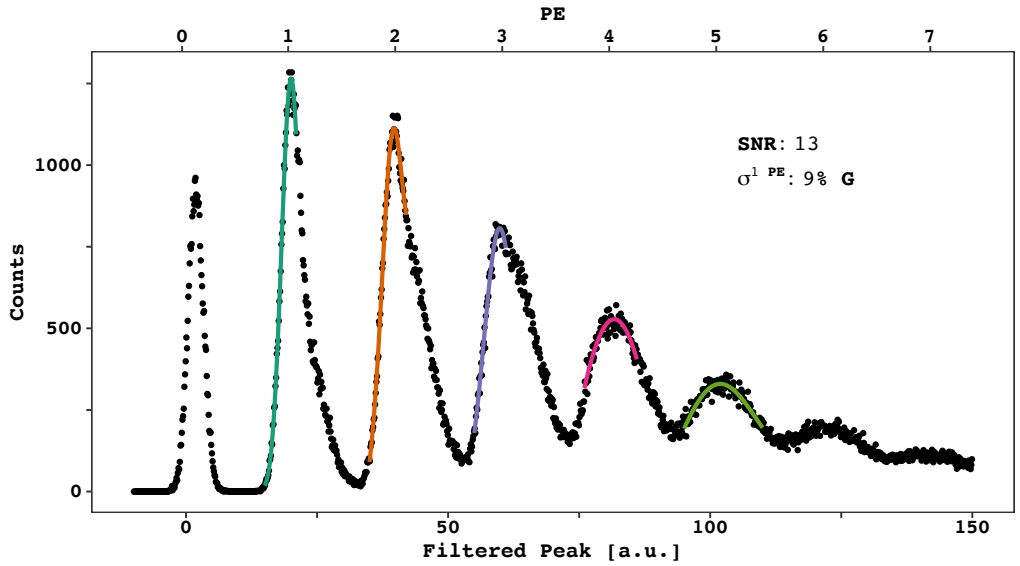
0.17 Gpbs
21.00 MB/s

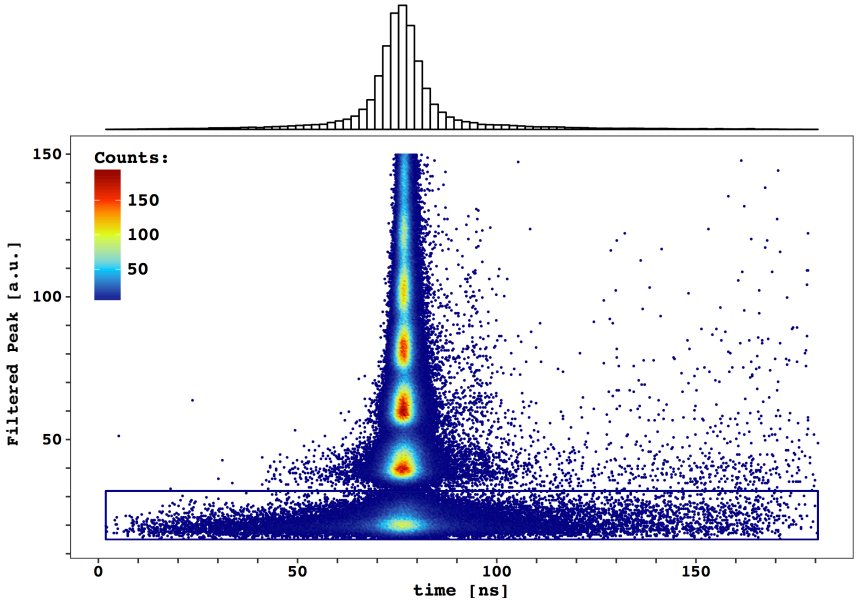
Some safety margin/ space for higher rate

- Upper table is with onboard determination of time and charge for small pulses (S1), lower table assume no onboard reduction of data for small pulses but a copy of ~5us worth of 124 MS/s around the peak for small pulses
- Data reduction at the Event Builder is crucial:
  - Could detect physical pulses by analyzing whole TPC (discard DCR related hits in the quiet window between S1 and S2, dominating the actual output rate
  - Could/should optimally fileter S1 waveform to extract physics information
  - Could compress data
  - Could prescale uninteresting events

Pulse Height Spectra After DSP

arxiv:1706.04220





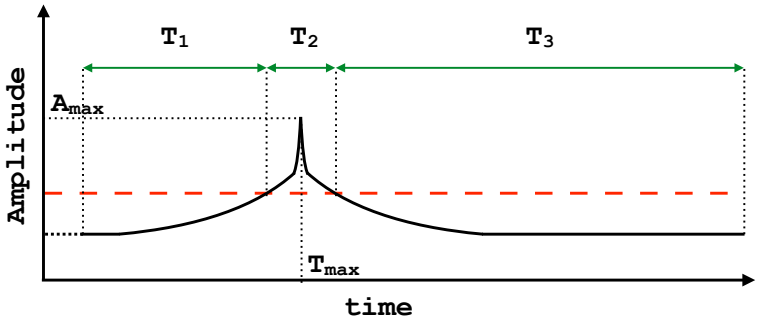
16 ns resolution (RMS) for 1PE peak

Signal acquired with a fast digitizer and processed offline with a cross correlation filter with τ of 400 ns

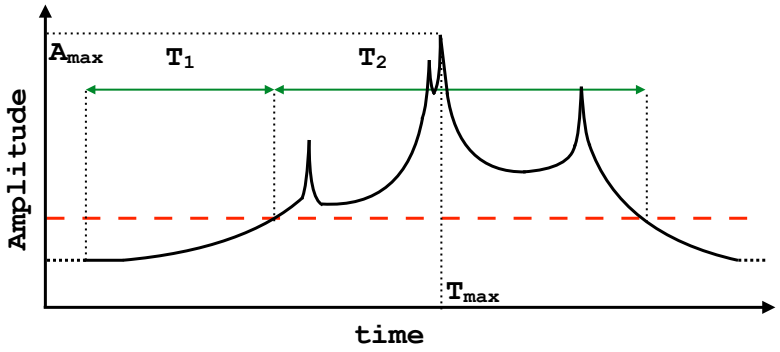
To obtain the needed S/N and time resolution on single PE for online trigger purposes a DSP need to be foreseen at the digitizer board level

S1/S2 digitization

Filtered signal



From C. Savarese Phd thesis



- On-board algorithm to distinguish S1 from S2-like algorithm
- Possibly based based on Time over Threshold (e.g. S1<5 μs, S2>5 μs)
- Allow raw waveform to be digitized for single PE hits and a reduced sampling rate digitization for S2-like signals

DAQ boards & man power

- For the digitization hardware two path are currently pursued:
  - A project for a 12 channel digitizer from INFN/Roma that could be adopted at least as a development platform or for early prototype readout, since a board prototype available this month. Project developed independently for the BDX dark matter experiment at JLAB.
  - A partnership with CAEN for a new digitizer lineup (first prototype Oct 2018 + development kit available April 2018)
- Both project have a target price/ch <150 € and share basic architecture → can mutually benefits of sharing expertise
- CAEN giving priority to DS needs and started development of a 14 bit 100/125 MS/s digitizer model with 64 channel per board first
- Input should be fully differential, a proposal for connectors expected coming soon from CAEN
- Output over ethernet connections to a PC in a streaming mode:
  - ✧ 900 Mb/s reached over 1Gb/s /link
  - ✧ Enabling also 10 Gb/s link soon (reached 2.4 Gb/s) in

- Established direct links between the TRIUMF group which may take responsibility for online daq software and the Rome and CAEN groups (meeting on Jan 31st)
- Work on integrating the specialised firmware that is being developed in Bologna with LNGS help will be started soon

12-Channel Digitizer from Rome LABE

- Analog front end (AFE)
  - SiPM and PMT compatible
  - Signal amplifier on board
  - True differential to the ADC
  - HV provided on board for SiPM (Control for PMT base)
- AFE Connectivity:
  - MCX (SiPM: signal+HV)
  - nanoFIT (PMT: controls, DAC, ADC)
  - VME backplane
- FastADC features:
  - Up to 250 Msps
  - 12/14 bit pin compatible
  - Low power: 90 to 280 mW/ch
  - Low cost: 9€ to 65€/ch
- ARM Cortex-M4 on motherboard:
  - HV DAC & ADC
  - Offset DAC
  - gain selection
  - HV enable
  - Local USB for Board check and debug
  - UART communication with FPGA module
- Xilinx Kintex7-based Zynq SOM
  - Zynq XC7Z030 up to XC7Z045
    - Dual ARM Cortex-A9
  - 1GB DDR3, Flash-MEM, USB, …
  - Plug-on module, replaceable with proprietary FPGA module for cost effectiveness
- Timing protocol:
  - Resolution: ~100 ps
  - White Rabbit Compliant
  - GPS HW interface (dedicated link for CLK and IRIG)
- Board connectivity:
  - Optical (SFP laser)
  - Copper GbE
  - USB 2.0
- Form Factor: VME Size-B
  - Backplane for power and mechanical housing

Project Timeline

- Frozen Schematics, Started PCB: May 2017
- Board ready for production: Sep 2017
- Prototype Ready: Feb 2018

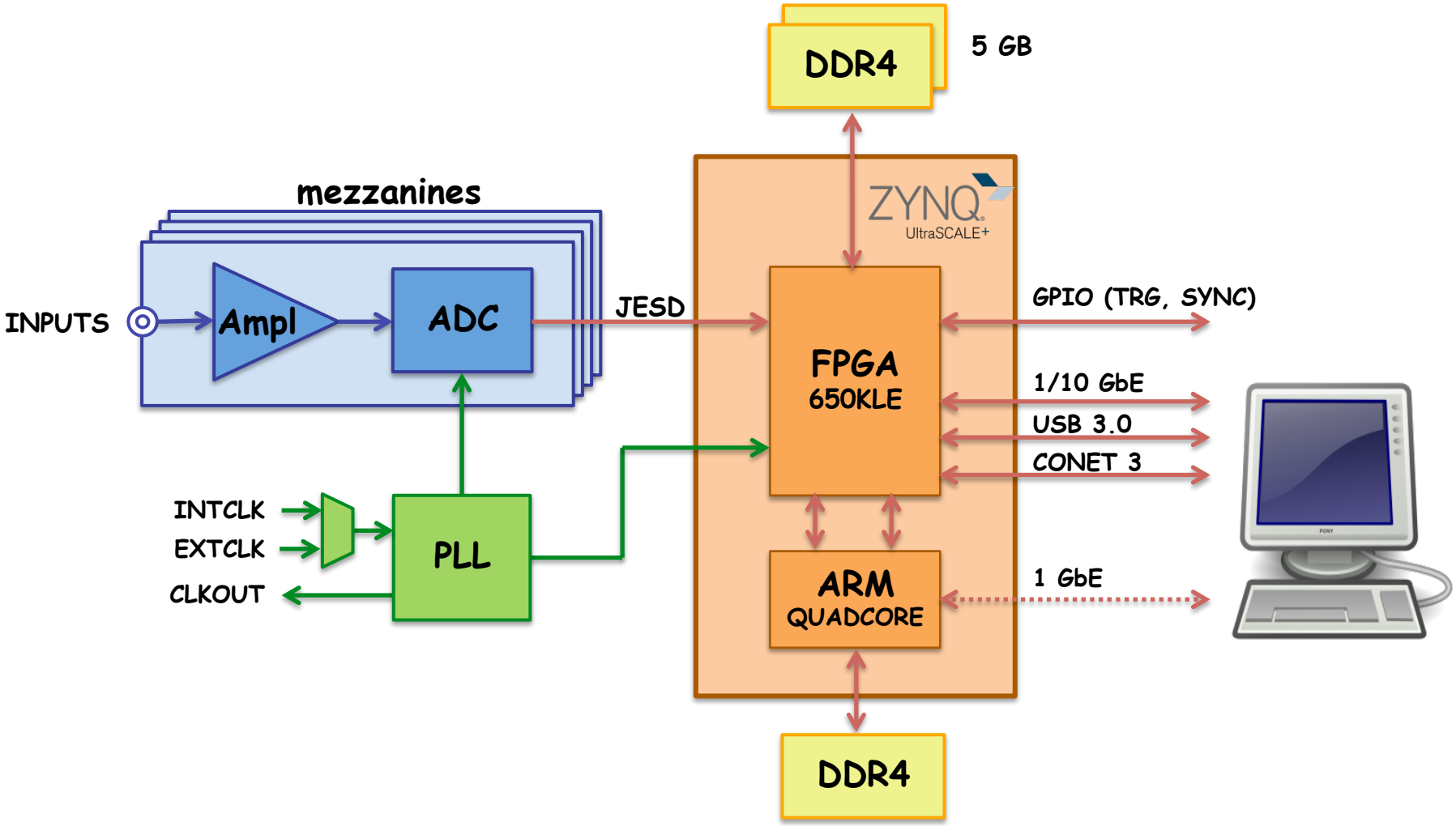
New Digitizers: motivation

- Increase readout bandwidth (from 1 to 10 Gbit/s)
- Ethernet interface (up to 10 GbE)
- Easy synchronization (clock and timing signals distribution)
- Increase memory size (migration from SSRAM to DDR4)
- Replacement of obsolete components
- Open FPGA (single FPGA architecture, SoC)
- Embedded ARM (quad core, Linux)
- New architecture to support state-of-the-art **JESD204D** A/D converters and extremely high data throughput to DDR4

New digitizers: preliminary specs

- **Communication**
  - **1/10 GbE**, Copper or Optical (TCP/IP? UDP?)
  - **CONET 3** daisy chainable optical link (expected ~300MB/s)
  - **USB 3.0**
  - Legacy VME interface
- **Memory buffers**
  - Acquisition Memory (FPGA): DDR4, 5 Gbytes, 384 Gb/s
  - Readout Memory (ARM): DDR4
- **Models**
  - 16 channel, 14 bit, 1 GS/s (replace x751)
  - 16 channel, 14 bit, 500/250 MS/s (replace x730/x725/x720)
  - 64 channel, 14 or 16 bit, 100 MS/s (replace x740/x724)
- **Firmware**
  - Single FPGA architecture; 650 kLE (Zync US+ XCZU11EG)
  - ARM (Quad Cortex, 1.5 GHz)
  - DPP modes: PSD/PHA/QDC/CFD
  - Raw Waveform mode with zero suppression capabilities (ZLE/DAW)
  - **Open FPGA** (template projects and kits for custom developments)

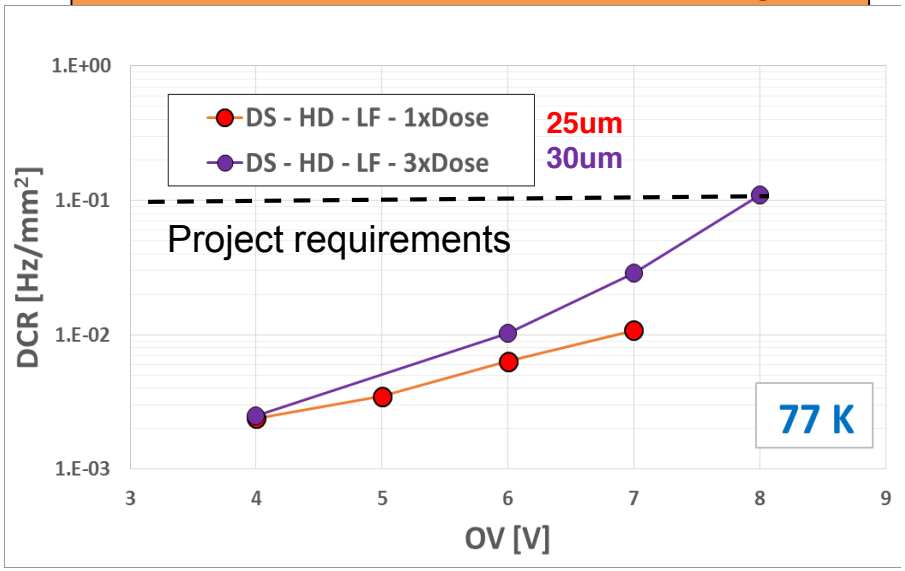
System Architecture



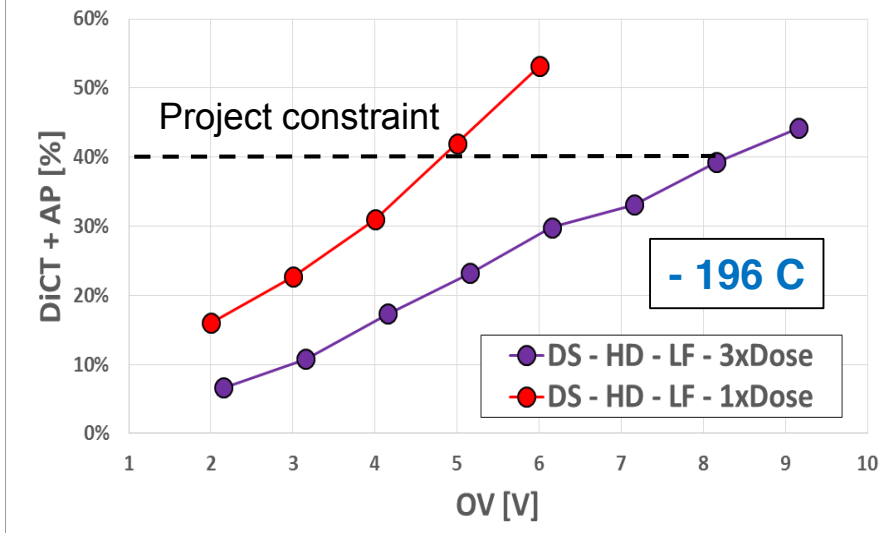
Note: Ethernet and CONET use the same SFP+ connector => mutually exclusive

Even if..

Comparison between technologies



Comparison between technologies



- 3xdose FBK SiPM vs 1xdose NUV-HD-LF

Rates

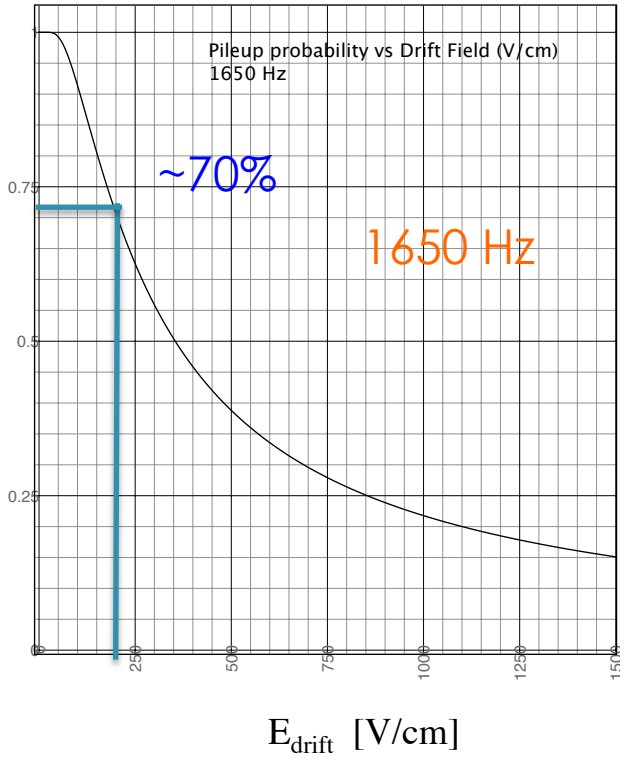
Expected rate in Ds-proto [Hz]			
Setup & location	On surface	LNGS HALL-C	LNGS HALL-C +1m water tank
^{39}Ar	400	400	400
Cosmic μ	210	-	-
External γ	10^4 [LUX] ?	250 ÷ 1000	1÷5
Cryostat γ Th,U,K	23-30	23-30	23-30
	> 1650	700 ÷ 1450	450

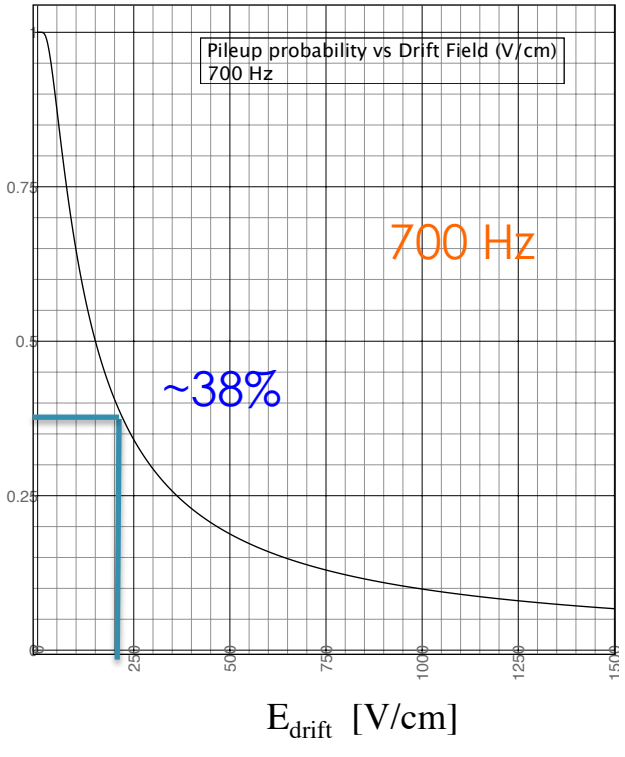
Cryostat assumed purity as in DS50 DB for the LSV Steel (sphere) :

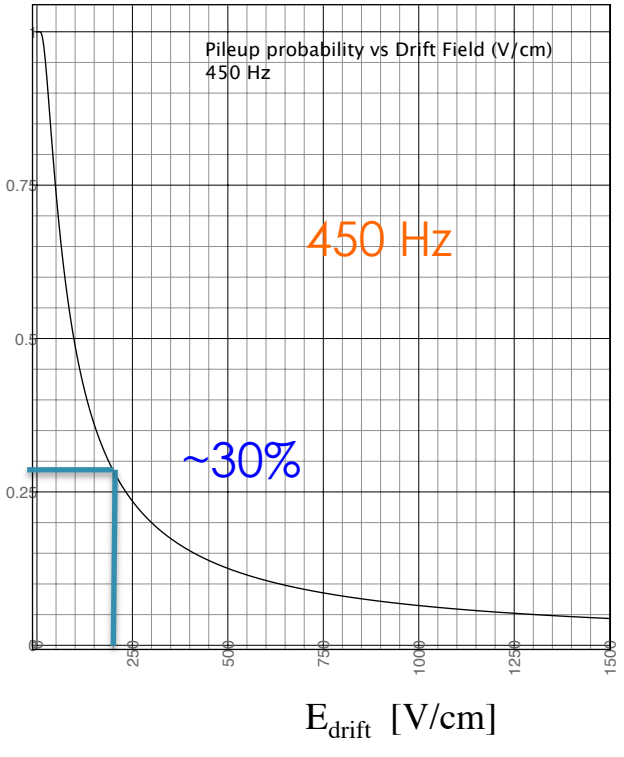
Th= 19 (mBq/kg) ; U = 43 (mBq/kg)

K = 2 (mBq/kg) ; Co =2.8 (mBq/kg)

Pile-up probability vs Drift Field



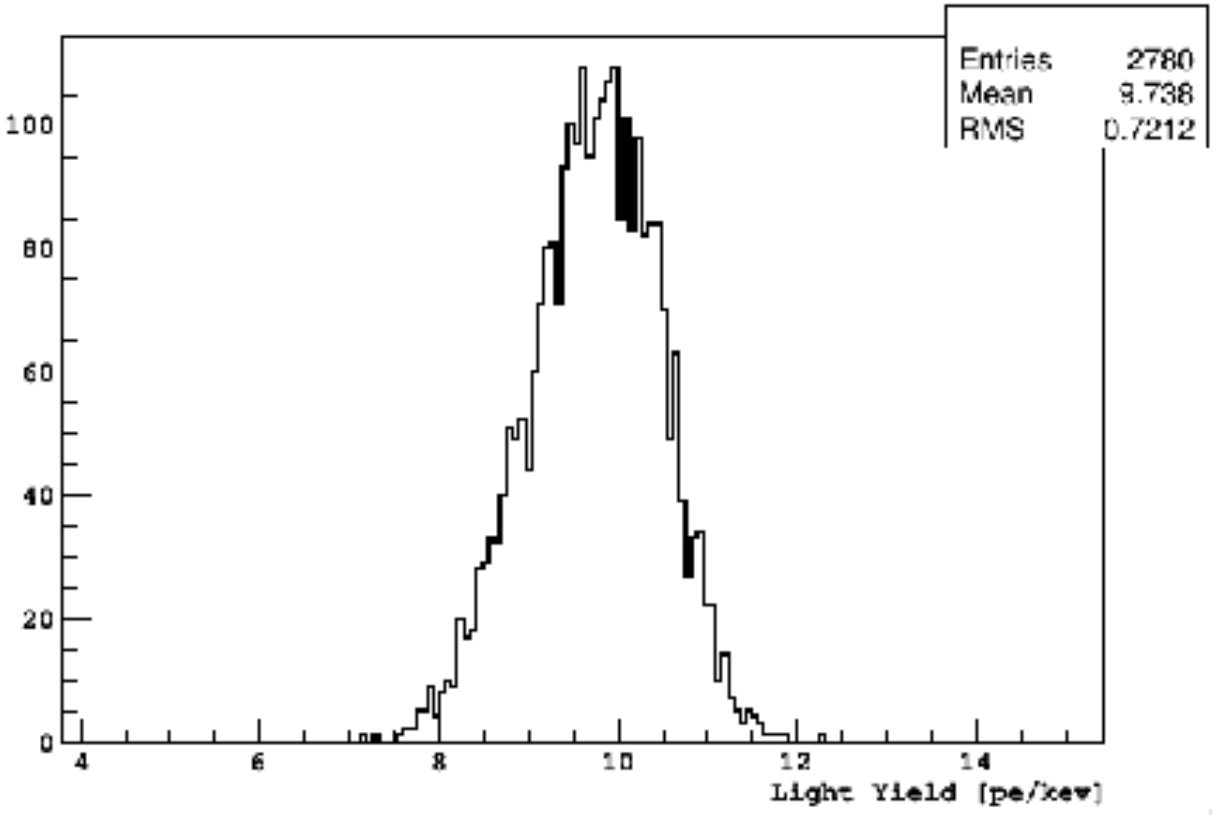




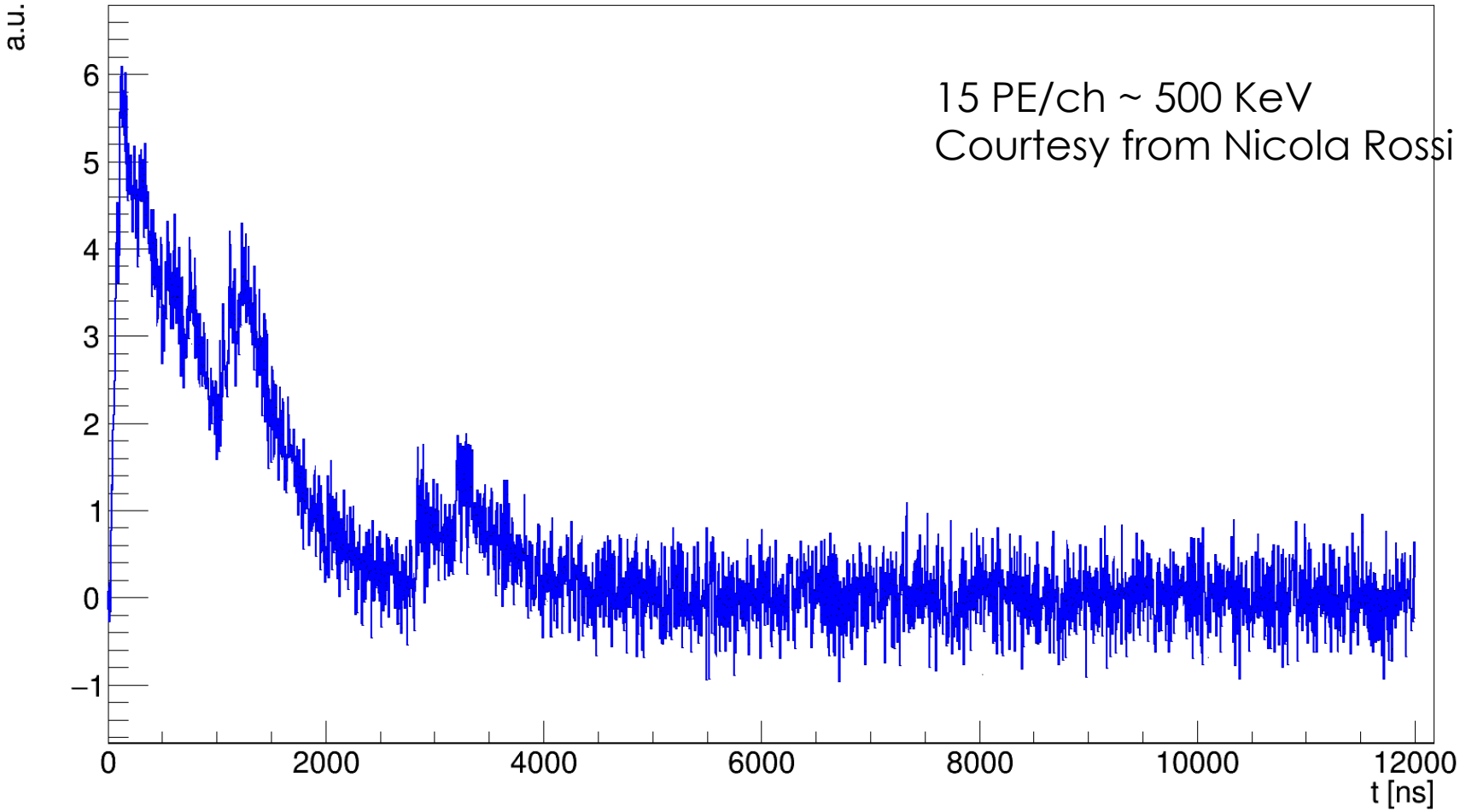
Difficult to operate in double face on surface

DS-Proto nominal LY

9.7 ± 0.1 pe/keV



“Typical” S1 waveform



DS-Proto readout cannot really be similar to DS-20k
Worse case scenario for current setup, after pulses?
Will need to readout

WBS 1.06 & 1.9.2
PREVENTIVI 2018

WBS 1.06 & 1.11.2

Work Package	Responsible	Group	NSF Funds	INFN-CSN2 Funds	Urania-2020 and INFN Giunta Funds	INFN-RAS and MIUR/CIPE Funds	INFN-RA Funds	INFN In Kind Contributions
		Units	[USD]	[EUR]	[EUR]	[EUR]	[EUR]	[EUR]
1.6 DAQ, Trigger, and Slow Control	M. Rescigno [E. Hungerford]		810	480	0	0	380	0
1.6.1 Readout	E. Hungerford	Houston	760	300	0	0	0	0
1.6.1.1 TPC Readout (US)	E. Hungerford	Houston	710					
1.6.1.2 TPC and Veto Readout (IT)	M. Rescigno	Roma1		300				
1.6.1.3 Prototype boards	M. Rescigno	Roma1	50					
1.6.2 Trigger	S. Giagu	Roma1	0	180	0	0	0	0
1.6.2.1 Clock distribution and trigger logic	M. Rescigno	Roma1		60				
1.6.2.2 Event Builder and Software Trigger	S. Giagu	Roma1		120				
1.6.3 Slow Controls	P. Cavalcante	VTech	50					
1.6.4 Infrastructure and Power Supply	A. Candela	LNGS	0	0	0	0	380	0
1.6.4.1 Electronics Infrastructure, Cabling, Cooling	A. Candela	LNGS					260	
1.6.4.2 SiPM Low Voltage and HV	A. Candela	LNGS					120	

- This element of the WBS need revisions…
- Was developed when SNR was unknown (simple timing by a discriminator and FPGA clock assumed, 100 $/ch)
- Some responsibility will shift also, new groups could absorb some costs
- Not ready to finalize at this point, but keep in mind

WBS 1.06 & 1.11.2

Work Package	Responsible	Group	NSF Funds	INFN-CSN2 Funds	Urania-2020 and INFN Giunta Funds	INFN-RAS and MIUR/CIPE Funds	INFN-RA Funds	INFN In Kind Contributions
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1.6.1.3 Prototype boards	M. Rescigno	Roma1	50					
1.6.2 Trigger	S. Giagu	Roma1	0	180	0	0	0	0
1.6.2.1 Clock distribution and trigger logic	M. Rescigno	Roma1		60				
1.6.2.2 Event Builder and Software Trigger	S. Giagu	Roma1		120				
1.6.3 Slow Controls	P. Cavalcante	VTech	50					
1.6.4 Infrastructure and Power Supply	A. Candela	LNGS	0	0	0	0	380	0
1.6.4.1 Electronics Infrastructure, Cabling, Cooling	A. Candela	LNGS					260	
1.6.4.2 SiPM Low Voltage and HV	A. Candela	LNGS					120	
1.11 Prototype	G. Fiorillo [L. Mapelli]	Napoli	0	721	0	0	0	0
1.11.1 Integration	G. Fiorillo	Napoli		61				
1.11.2 DAQ	M. Rescigno	Roma1	0	93	0	0	0	0
1.11.2.1 DAQ and trigger	TBD	Roma1		63				
1.11.2.2 DAQ server and data management	TBD	Roma1		10				
1.11.2.3 slow control	TBD	Roma1		20				

- The prototype DAQ cost assumed:
  - first phase readout with OTC components for ~50 channels
  - a prototype trigger farm
  - some slow controls for cryogenics and PS

Preventivi 2018/Proto. boards

Work Package	Responsible	Group	NSF Funds	INFN-CSN2 Funds	Urania-2020 and INFN Giunta Funds	INFN-RAS and MIUR/CIPE Funds	INFN-RA Funds	INFN In Kind Contributions
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CONSUMO	1. Consumi laboratorio e test-stand in sede	2.00		
	2. Consumi DS-proto DAQ + Criostato	5.00		
	3. Slow Control DS-proto [WBS 1.11.2.3] (all. 1 e 2)	10.00	17.00	0.00

INVENTARIO	1. RED: trigger logic board [WBS 1.10.5.1]	4.00		
	2. Flash ADC e trigger per DS-Proto [WBS 1.11.2.1] (CAEN, commercial modules) (all. 3-5)	75.00		
	3. 2 schede prototipo CAEN X onboard DSP [WBS 1.6.1.3 v12] Roma + DS-proto	25.00		
	4. DAQ server and data management [WBS 1.11.2.2]	10.00		
	5. Slow Control DS-proto [WBS 1.11.2.3] (all. 1 e 2)	10.00		
	6. Alimentazione HV/LV SiPM Tile e FEB per DS-Proto [anticipo su WBS 1.6.4.2]	20.00	144.00	0.00

Preventivi 2018/Proto. boards

- Item originally on NSF funding and Houston design
- New developments imply INFN take care of prototyping costs
- Requested budget would allow to mount a test stand in Rome for software development and data transport tests into HLST test machine (available) and to serve DS-proto readout for 50 channels as required in 2018; hypothesis:
  - 150 Eu/ch. X 64 ch/board = 12 kE /board → 2 boards

Preventivi 2018/DS-proto DAQ

Work Package	Responsible	Group	NSF Funds	INFN-CSN2 Funds	Urania-2020 and INFN Giunta Funds	INFN-RAS and MIUR/CIPE Funds	INFN-RA Funds	INFN In Kind Contributions
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	4. DAQ server and data management [WBS 1.11.2.2]	10.00		
	5. Slow Control DS-proto [WBS 1.11.2.3] (all. 1 e 2)	10.00		
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Preventivi 2018/DS-proto DAQ

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Preventivi 2018/DS-proto DAQ

- Based on commercial products
- Readout similar to current DS50 readout
- Budget based on CAEN price list to INFN (attached to DB):
  - 4 16 ch V1730B/V1725 (~1kE/ch) + 1 V2495 - Programmable Logic trigger board + 1 A3818A - PCIe 1 Optical Link + 1 VME Crate
  - Tot. 74kE
- Server, based on a Dell quote:
  - power edge R630 con 3 PCIe slots + 2 x XEON E5-2630 (10x2 = 20 cores = 40 hyper threads) + 128 GB RAM + 300 GB + 2x1.8 TB disk + dual hot-plug power supply: 7.4 kE
  - Rack and control PC to be added
- Cabling and other consumables included into Roma1 "DS-proto DAQ + criostato" entry

Preventivi 2018/Slow Control

Work Package	Responsible	Group	NSF Funds	INFN-CSN2 Funds	Urania-2020 and INFN Giunta Funds	INFN-RAS and MIUR/CIPE Funds	INFN-RA Funds	INFN In Kind Contributions
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	6. Alimentazione HV/LV SiPM Tile e FEB per DS-Proto [anticipo su WBS 1.6.4.2]	20.00	144.00	0.00

Preventivi 2018/Slow Control

- DS-proto cryo system is basically DS-20K
- Need complex slow control, based on NI CRIO system as described in YB for DS20K
- Re-use spare component to save, minimal setup required:

Slow Control parts list	Description	Quantity
Controller NI cRIO-9039	cRIO-9039, 1.91 GHz Intel Atom Quad-Core CompactRIO Controller, 8-Slot, Kintex-7 325T FPGA, Real-Time, -20 to 55 celsius	1
Expantion chassis NI-9149	NI 9149 8 Slot Ethernet Expansion chassis for C Series Modules	1
Power supply NI PS 16	NI PS-16 Power Supply, 24 VDC, 10 A, 100-120/200-240 VAC Input	2
NI 9485 (Solid state relays)	SSR Relay, 60 VDC/30 Vrms, 750 mA, 8 Ch Module	1
NI 9478 (Digital output)	48 V, Sinking Digital Output, 16 Ch Module	2
NI 9209 (analog input)	±10 V, Analog Input, 500 S/s, 16 Ch Module	1
NI 9208 (analog input)	±21.5 mA, Current Analog Input, 500 S/s, 16 Ch Module	1
NI 9264 (analog output)	±10 V, Analog Output, 25 kS/s/ch, 16 Ch Module	1
Ni 9266 (analog output)	0 to 20 mA, Analog Output, 1 kS/s/ch, 8 Ch Module	1

- Quote for ~20 kE for the above material included in the DB, 10 (inv) + 10 (consumable)
- N.B. if referee agree, it could a better split could be 15/5 (INV/CONS)