UNIVERSITY OF BIRMINGHAM
SCHOOL OF PHYSICS AND ASTRONOMY

The ATLAS Inner Tracker detector for the High-Luminosity LHC upgrade

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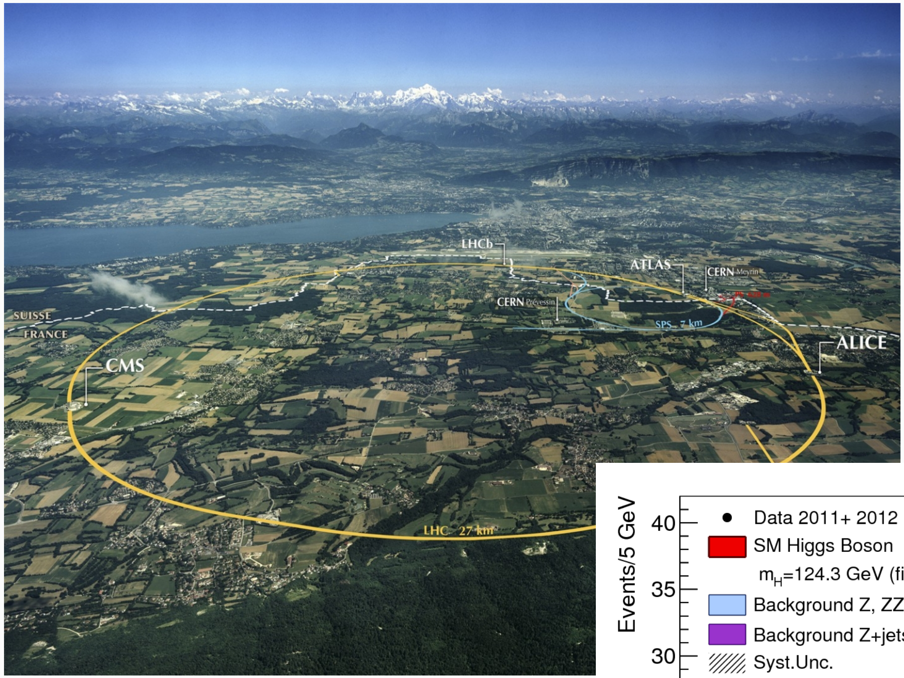
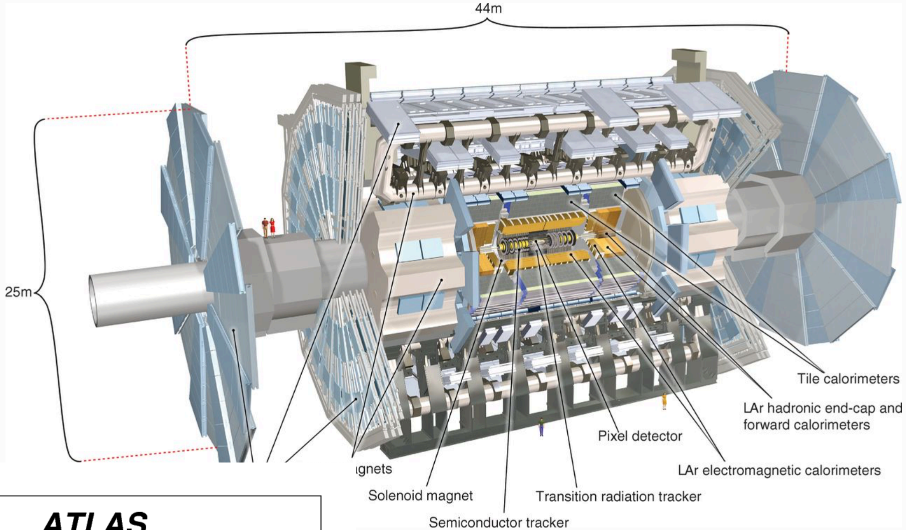
4 July 2018

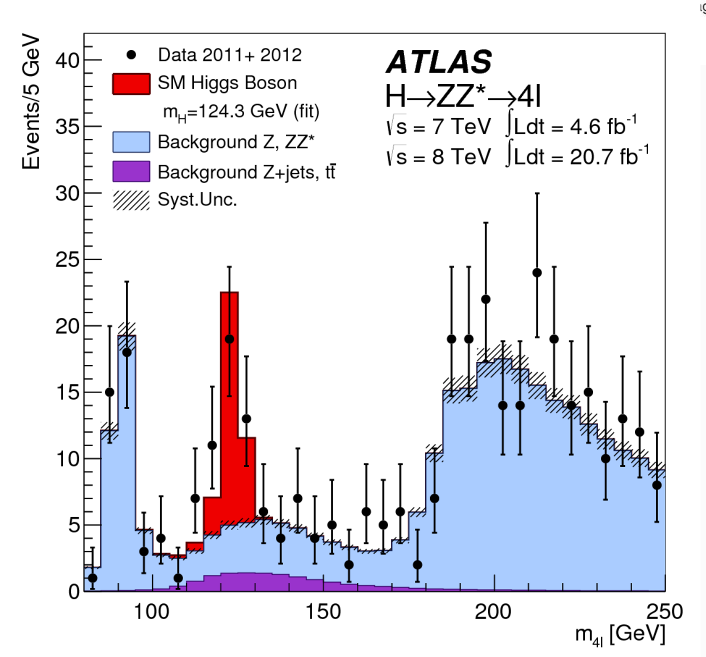
Outline

- The HL-LHC upgrade & challenges for detectors
- The ATLAS Inner Tracker (ITk) design and performance
- ITk detector modules
  - Sensor development
  - Readout electronics design
- Lightweight services
- ITk production
- Conclusion

LHC and ATLAS







The High-Luminosity LHC

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by Corinne Pralavorio

Posted by Corinne Pralavorio on 26 Jun 2018. Last updated 26 Jun 2018, 16.21. *Voir en français*

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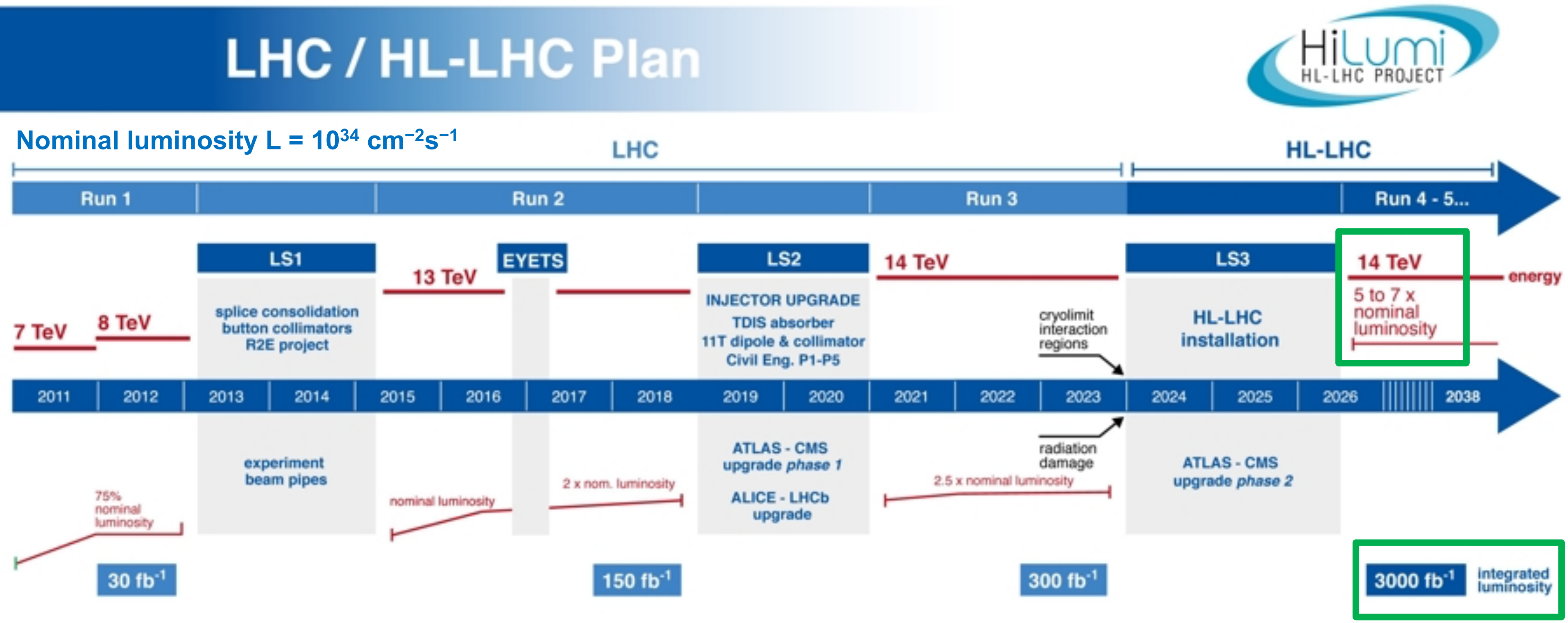
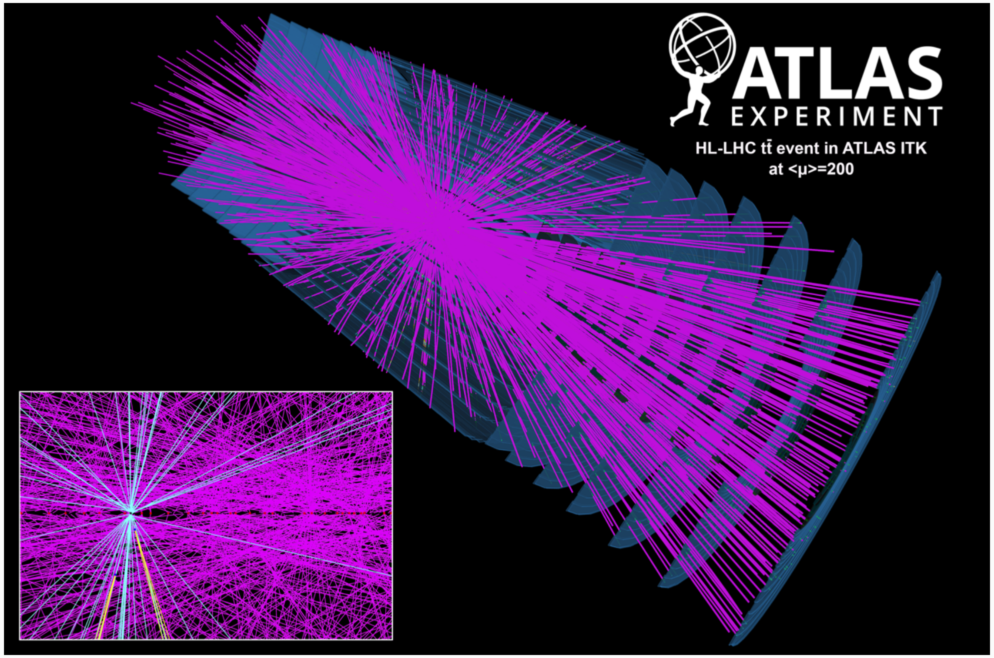


- **Higher energy and luminosity** benefit searches for new particles, precision measurements and study of rare processes but pose severe challenges to the detectors
- The **vertex and tracking detectors**, being the closest to the IP, will need significant upgrade

Particle density and data rate

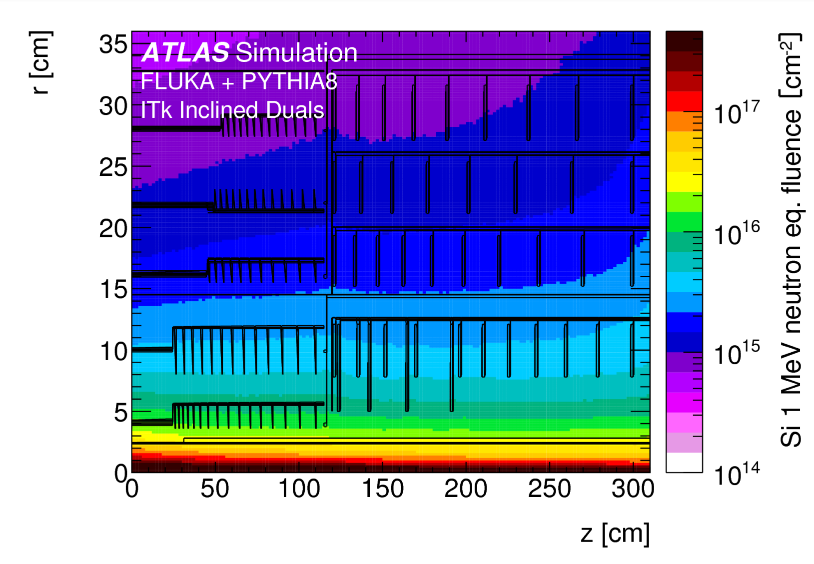
- With an instantaneous peak luminosity up to **7.5 x 10^{34} cm^{-2}s^{-1}** the mean number of interactions per bunch crossing (i.e. every **25 ns**) is **200** (pile-up) → **high particle density and data rate**

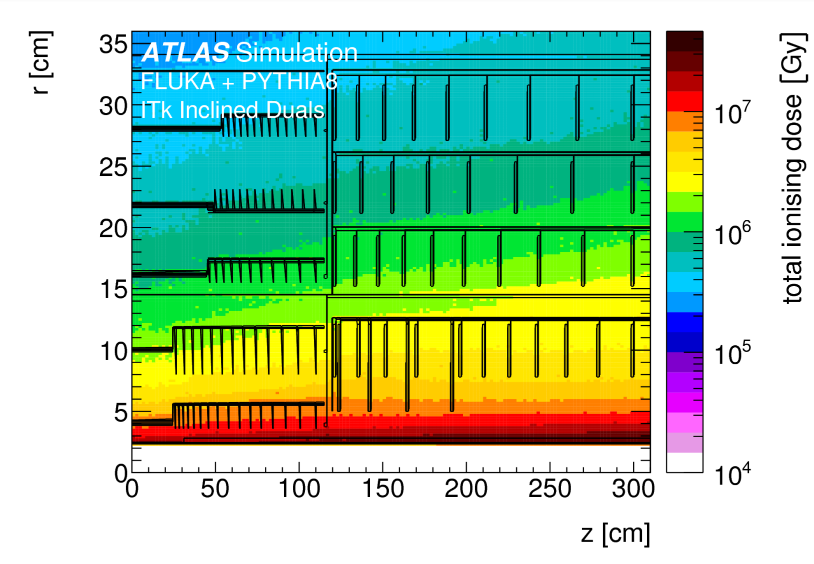


- **Finely segmented detectors** and **fast readout electronics** are needed to keep low hit occupancy [hits/cm^2/sec]

Radiation levels

- The integrated luminosity of **4000 fb^{-1}** results in x10 radiation damage with respect to LHC
  - Fluence up to **1.3 x 10^{16} 1 MeV n_{eq}/cm^2**
  - Total Ionising Dose up to **10MGy = 1 Grad**

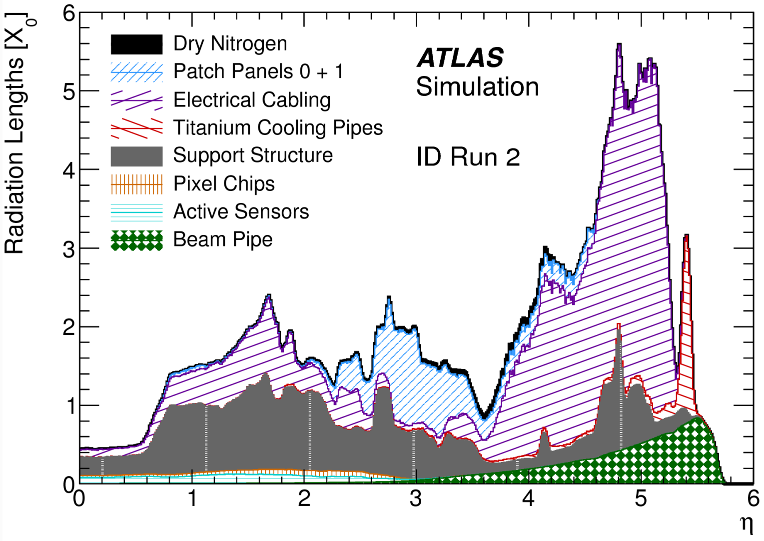




- **Radiation hard technologies** for sensor and electronics

More challenges

- **Material budget**
  - Multiple scattering and nuclear interactions in tracker material limit tracker and calorimeter performance
  - Dominant source of material are services and support structures

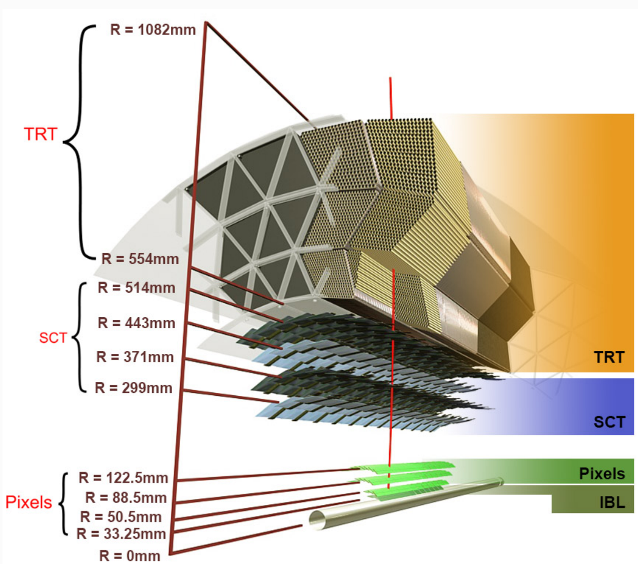


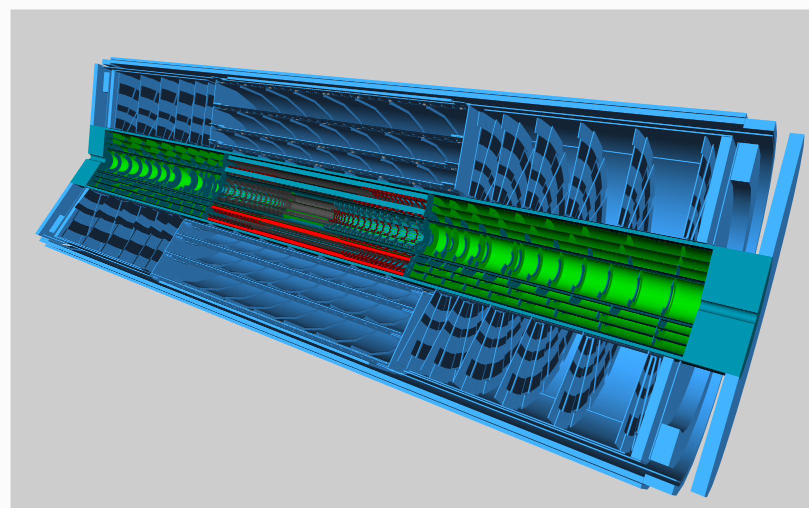
- **Hermeticity** and sufficient **number of hits** over **large angular acceptance**
  - Particles originating from within the 30cm-long beam spot should hit a sensor in each layer they traverse
  - A high number of hits is needed for good tracking efficiency but a trade-off with the amount of material has to be found
- **Cost** should be minimised

- All these challenges have to be met while keeping the same tracking performance of the current ATLAS tracking detector

ATLAS tracker upgrade

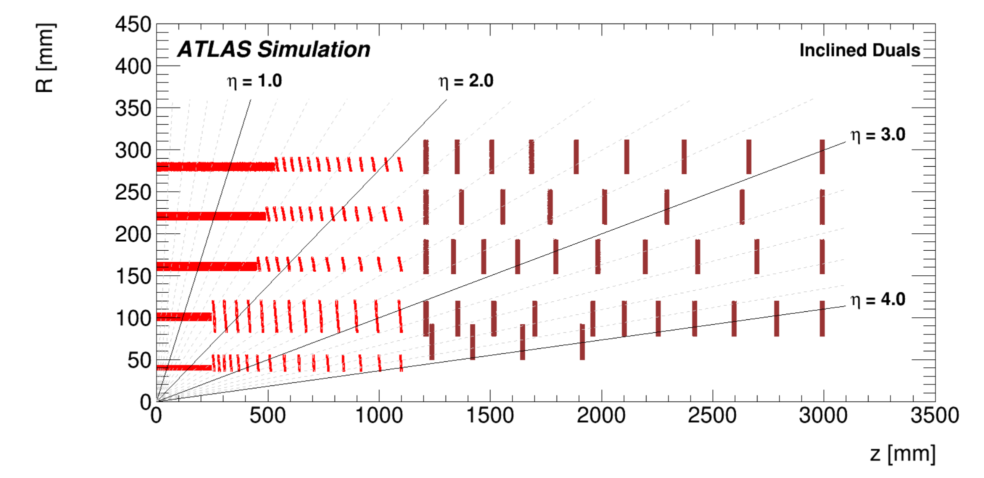
- The current ATLAS Inner Detector (ID) needs to be replaced for the HL-LHC
  - Severe radiation damage to all components
  - TRT technology cannot cope with hit occupancy
- ATLAS is planning a new **all-silicon Inner Tracker (ITk)** using **state-of-the-art silicon technologies** and **optimised design** of all detector components





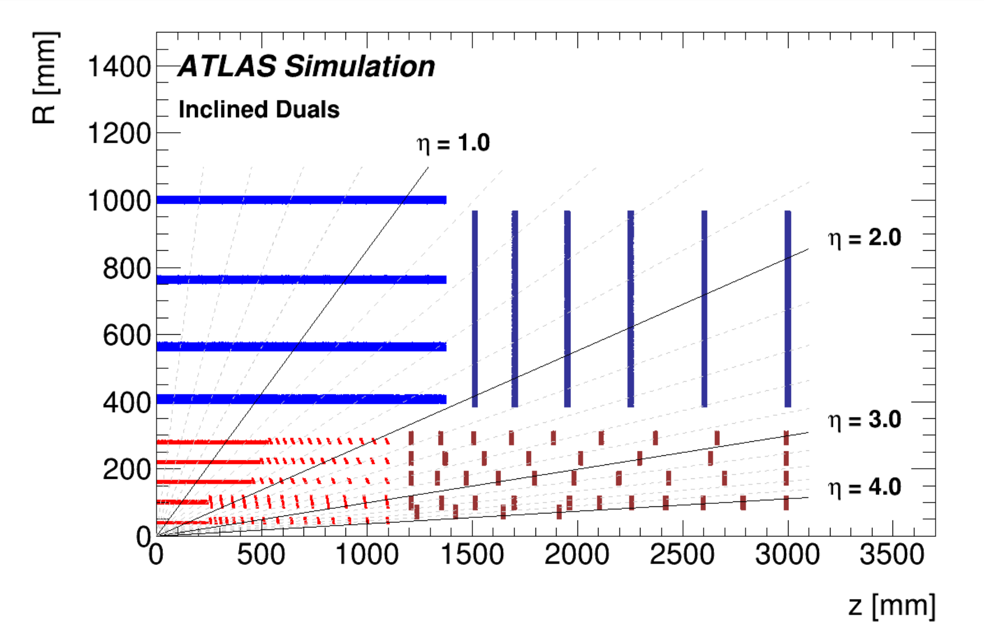
ITk layout

- **Pixel** detector
  - Cover to η **= 4.0**
  - **13 m²** of silicon sensors
  - Design optimised to **improve hit coverage with less material**
    - Inclined modules
    - Endcap-ring system
  - Two innermost layers designed to be replaceable to cope with radiation environment



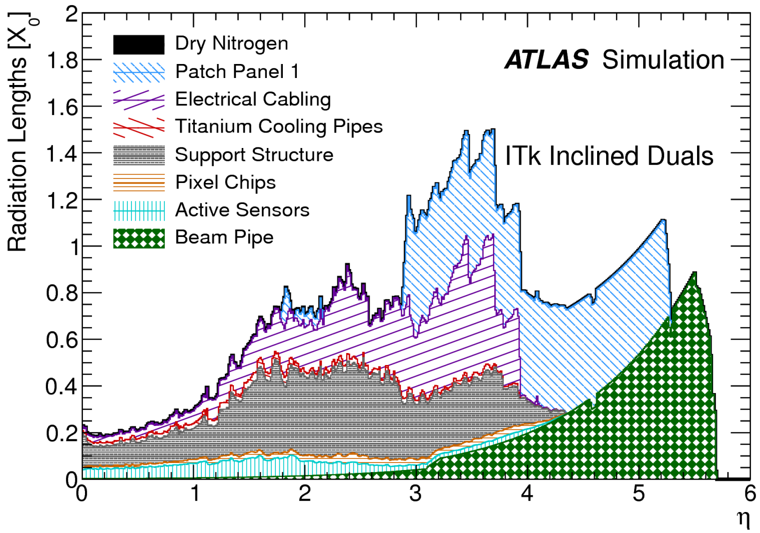
ITk layout

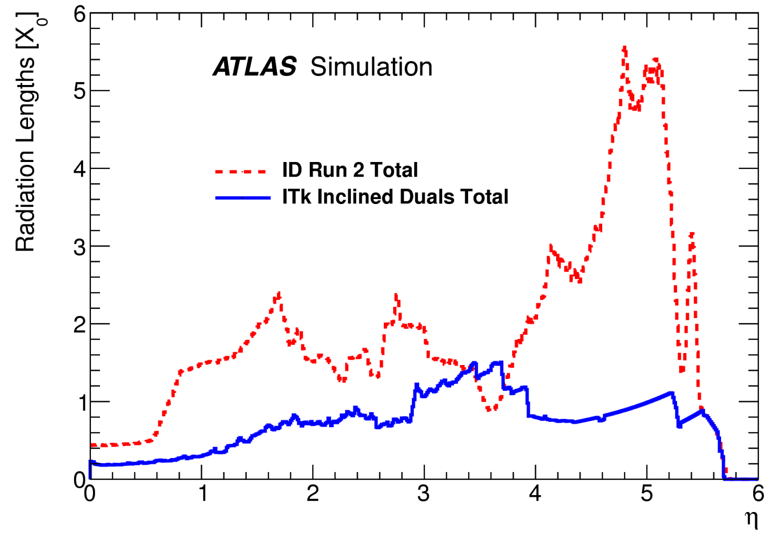
- **Strip** detector
  - Cover to η **= 2.7**
  - **165 m²** of silicon sensors
  - 4 barrel layers and 6 endcap
  - Modules loaded on both side of support structure with small stereo angle giving the second coordinate measurement



ITk material budget

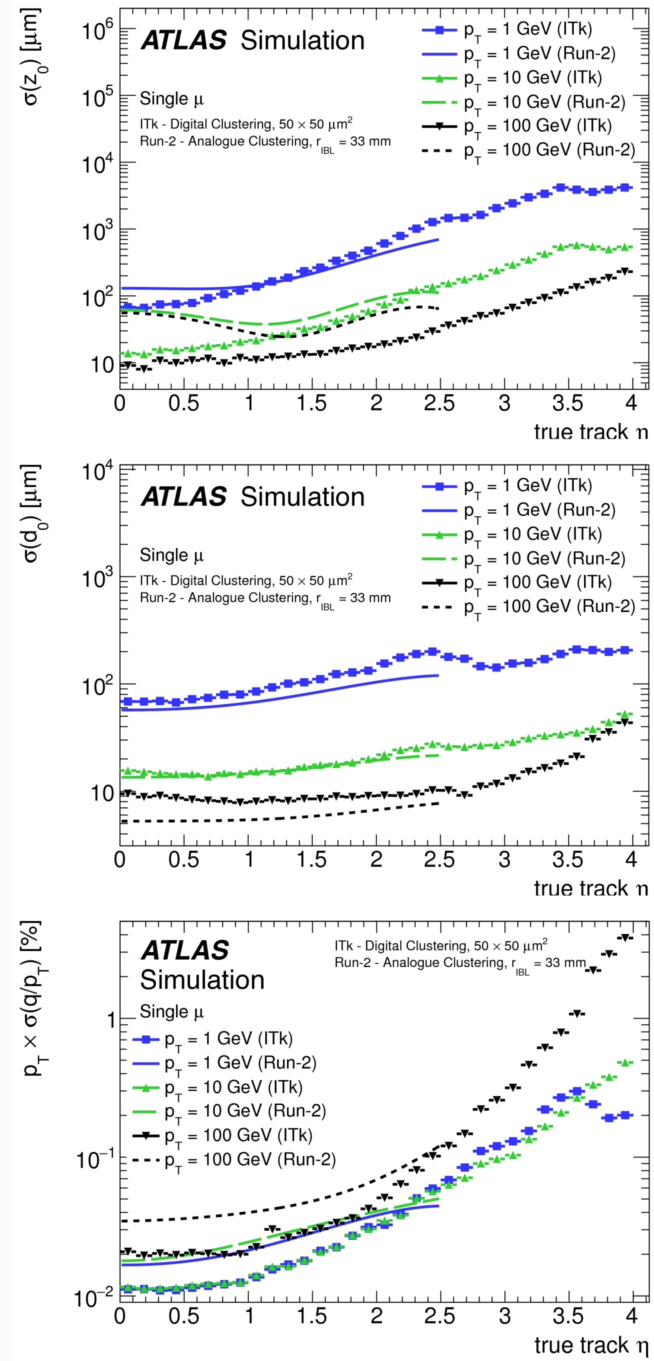
- The material of the ITk is significantly less than for the ID at almost all η
- The main drivers for the improvement are
  - Thinner silicon
  - Innovative power distribution schemes
  - Optimized routing of services
  - Rigid mechanical structure with lightweight carbon foam core





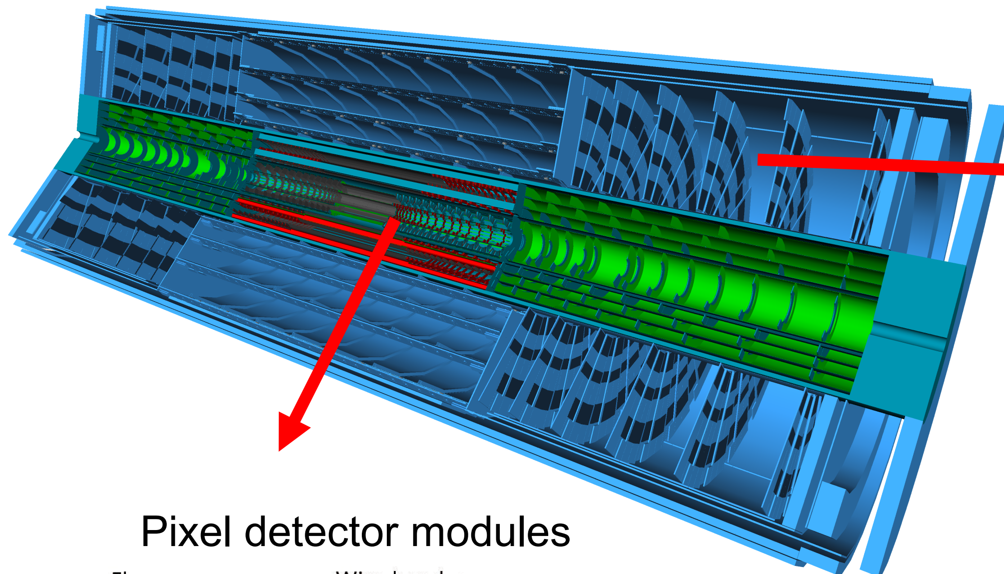
ITk track parameters resolution

- Longitudinal impact parameter resolution (pile-up rejection)
  - Improved by pixel finer segmentation in z ($50\mu m$ instead of $250\mu m$)
- Transverse impact parameter resolution (b-tagging)
  - Worse resolution at high p_T due to larger radius of inner pixel layer ($39mm$ instead of $33.5mm$; radiation and data rate prohibitive at smaller radii)
- Transverse momentum resolution
  - Improved by almost a factor 2 thanks for the higher precision of the strip detector wrt. TRT
- Lower material benefits all track parameters resolution

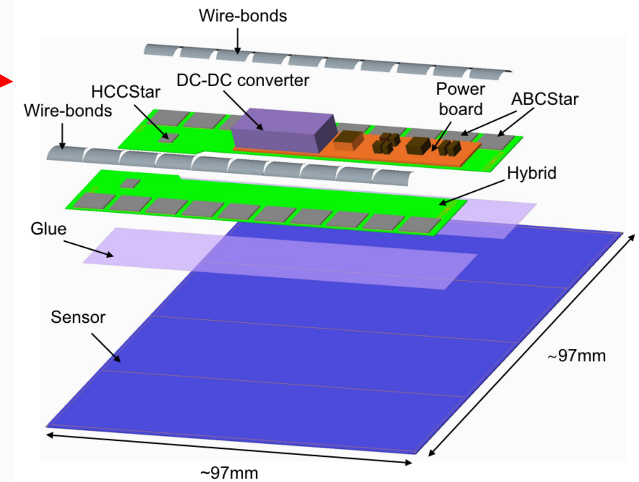


ITk detector modules

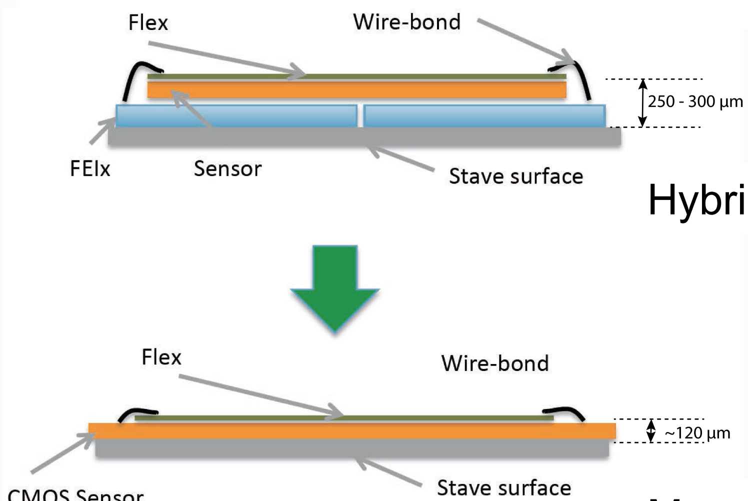
Silicon detector technologies for the ITk



Strip detector module



Pixel detector modules

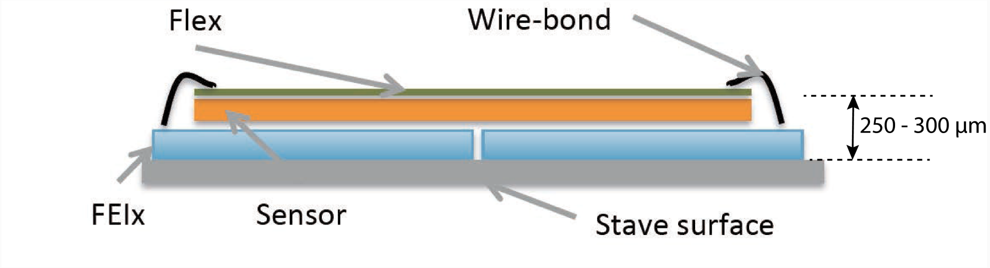


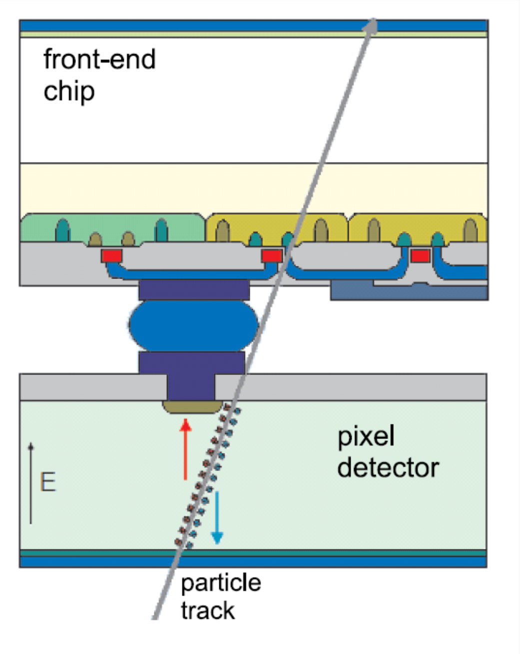
Hybrid

Monolithic

- Common elements
  - Sensor
  - Readout electronics (Front-End chip)
  - Interconnections
  - Electrical interface (power and data)

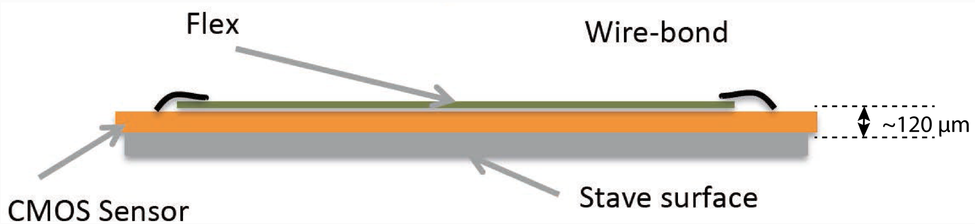
Hybrid pixel detector concept

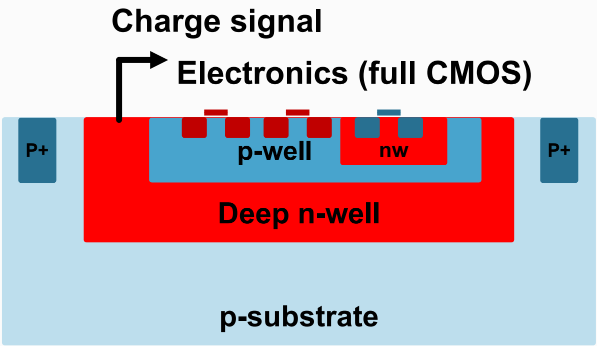


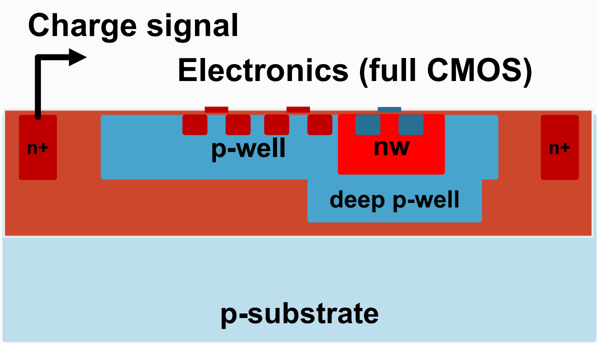


- Developed for operation at the LHC
- **Baseline** concept for ITk pixel detector
  – Optimised sensor design
  – New CMOS technology for the readout chip
- Sensor and readout electronics are separate entities connected via **fine pitch bump bonds**
  – Each pixel is connected to one readout channel in the FE chip
  – Expensive, non-commercial hybridization process
- Electrical interface, **flex,** glued on sensor backside
  – Hosts passive components and auxiliary chips (i.e. for data aggregation and transmission)
  – Wire bonds connection to sensor and FE chip

DMAPS in commercial CMOS technology



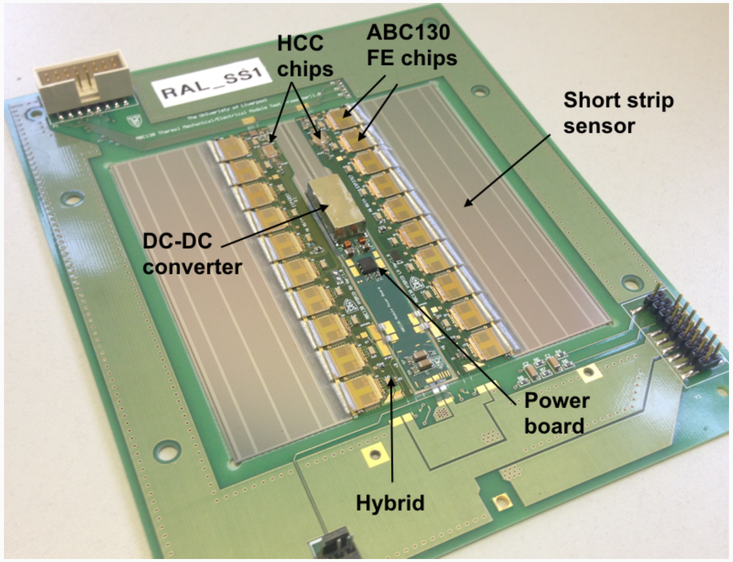


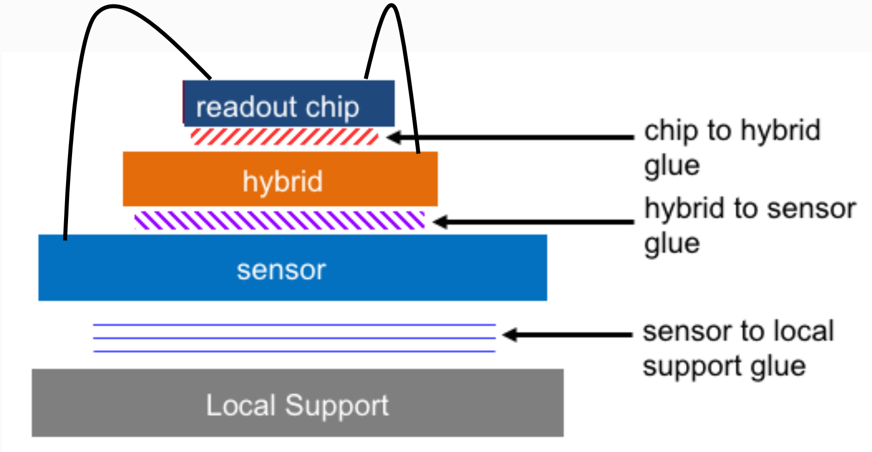


- Monolithic active pixels sensors (MAPS)
  - Sensor and readout electronics in the same substrate
  - Originally developed for low rate applications (STAR and ALICE ITS)
- Recent development with commercial CMOS technologies improve radiation-hardness and high rate capability → **Depleted MAPS**
- No hybridisation and advantages of commercial fabrication process → **low cost and ease of construction**
- Candidate technology for pixel outermost layer

Strip detector module

- Hybrid concept with separated sensor and readout electronics
- Two electrical interfaces, **hybrid flex and power board**, glued on the sensor front-side
- Readout ASICs and data aggregator chip are glued on the hybrid flex and wire bonded to the sensor
  - Each strip is connected to one readout channel in the FE chip
- Power distribution is provided via the power board

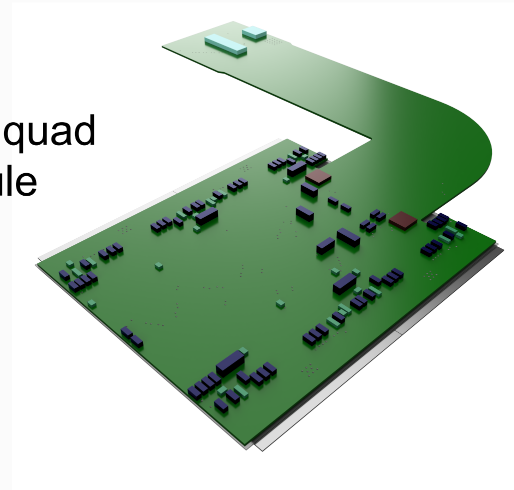




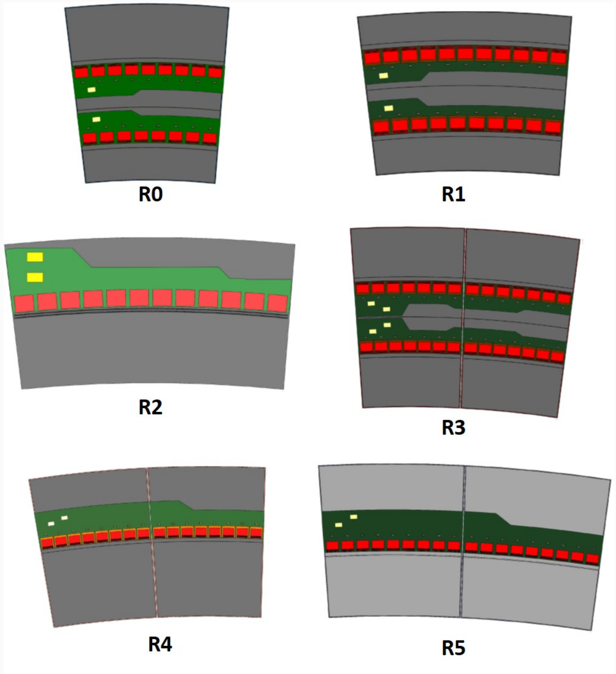
Module types in the ITk

- To provide hermetic coverage, different module configurations are need resulting in a **large number of different sensors and hybrid/flex flavours**
- Pixel modules can be single, dual, or quad depending on whether the sensor is bump bonded to one, two, or four FE chips
- Strips
  - Long-strip and short-strip barrel modules
  - R0, R1, .., R5 modules for the end-cap

Pixel quad module



Strip end-cap modules



Sensor development

Radiation tolerant silicon sensors

- High energy particles introduce **complex lattice defects** in the silicon bulk, i.e. energy levels in the silicon band gap

- Increased **leakage current**
  - Shot noise
  - Temperature increase → higher leakage current → need to cool sensors to avoid **thermal runaway**
- Change in **effective doping concentration**
  - Change in charge collection volume
- **Charge trapping**
  - Smaller sensor signal

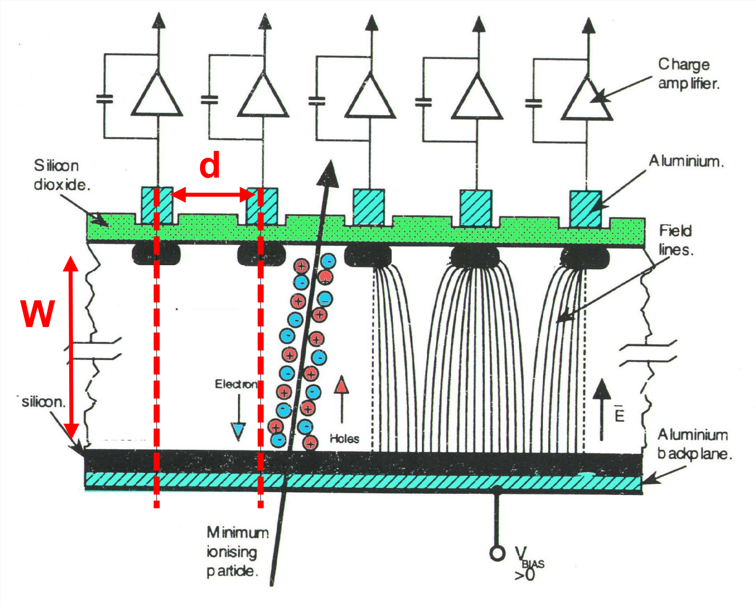
	Max fluence [1 MeV n_{eq}/cm^2]
Pixel	1.3×10^{16}
Strip	1.2×10^{15}

- To mitigate these effects **charge should be collected by drift**

Drift based silicon sensors

- Drift based silicon sensors work as a **reverse biased pn-junction**
- Low doped, i.e. **high resistivity**, silicon bulk with highly doped collection electrodes
  - The segmentation (pitch, d) of the contacts defines the **spatial resolution** (σ)
- **High (reverse) bias voltage** (V_{bias})
  - **Depletion** grows into the substrate
  - Electric field

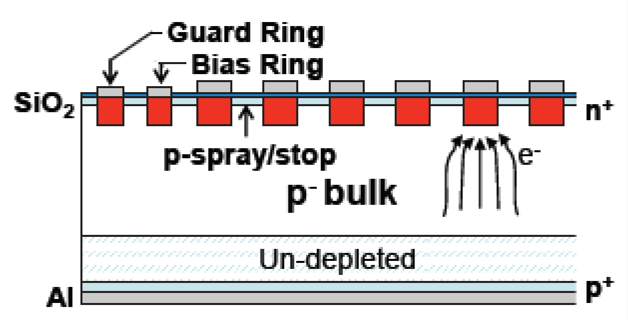
Cross section of a silicon sensor



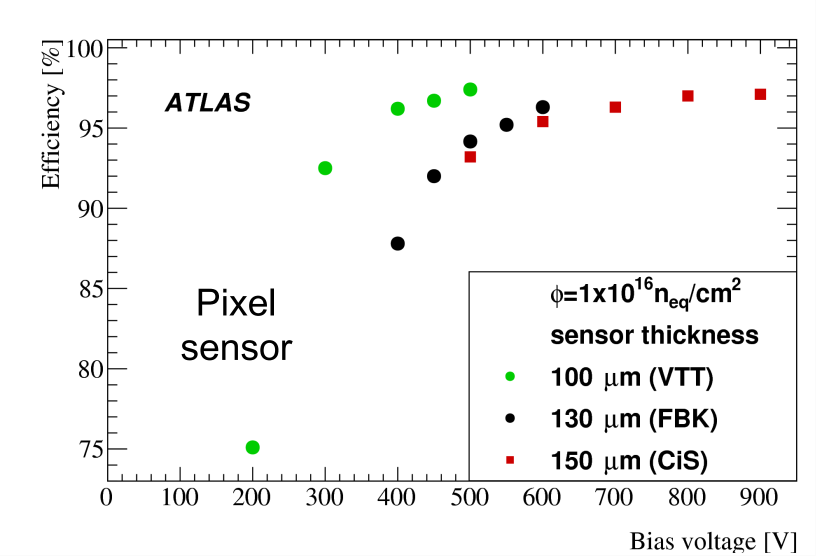
$$W \propto \sqrt{\rho V_{bias}}$$

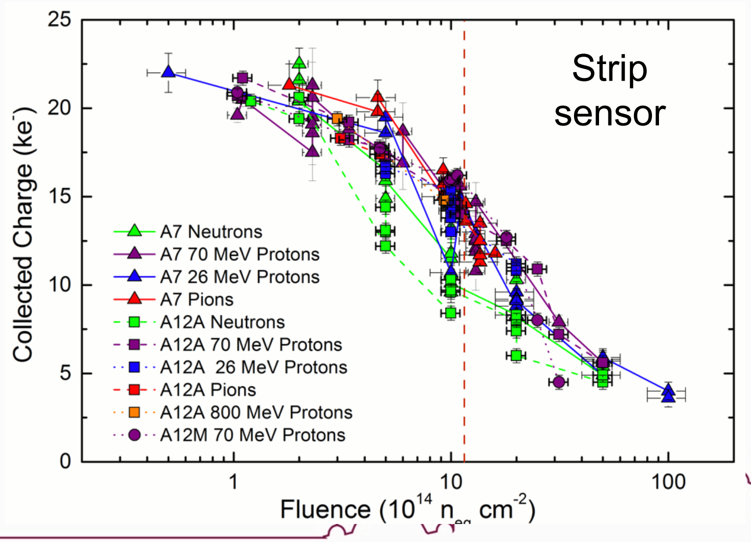
- Traversing charged particles create e-/h+ pairs
- Movement of charges (i.e. **drift** in electric field) towards the electrodes generates a signal
  - Large collected charge, fast charge collection, radiation-hard

Planar pixel and strip sensors



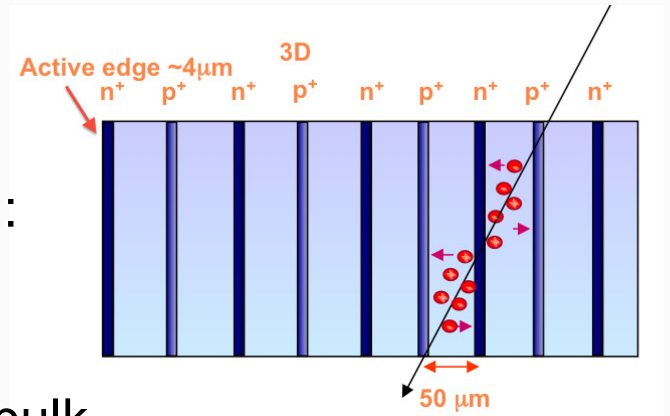
- **n-in-p** configuration for both strips and pixels
  - In the ID strips are p-in-n and pixels n-in-n
  - Signal from electrons faster than holes
  - One sided process, simpler and cheaper than n-in-n
- Optimised design of bias structure and edge region to obtain uniform electric field
- Pixel pitch 50 x 50 or 25 x 250 μm², thickness 100-150 μm
- Strip pitch 75 μm x 25-50 mm, thickness 300-320 μm



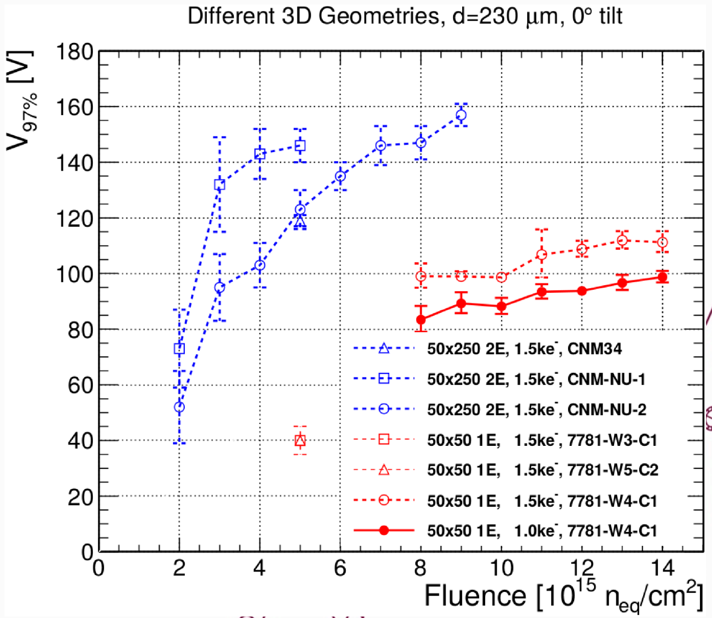


3D sensors

- Alternative geometry for pixel sensors that provides higher radiation tolerance by design: **drift path decoupled from particle path**
  - First application in the IBL detector
- Electrodes penetrate vertically in the sensor bulk
  - Shorter charge collection distance → **less charge trapping**
  - **High field with low voltage** → lower power, i.e. heat, after irradiation
- Technology of choice for pixel inner layer

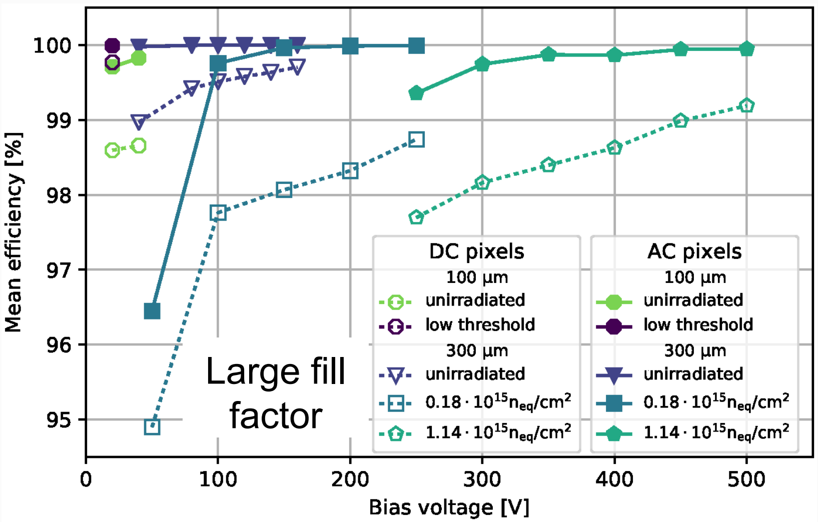


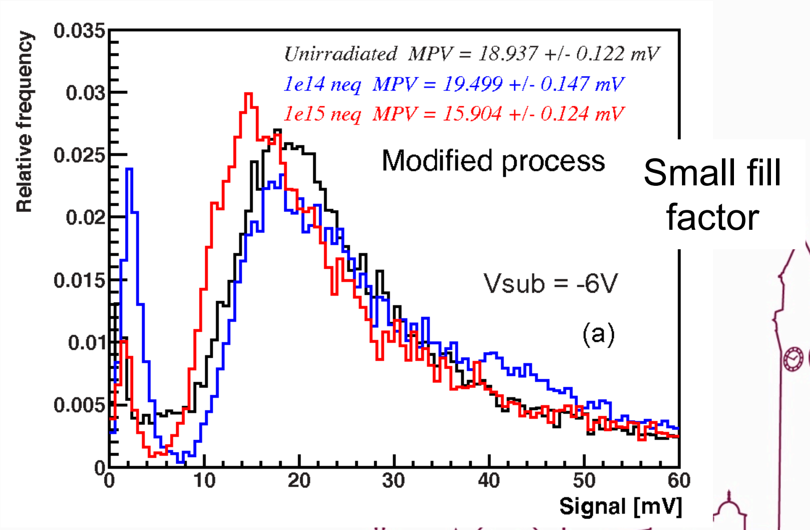
	IBL	HL-LHC	
Pixel size [µm^2]	50 x 250	50 x 50	25 x 100
Electrode config	2E	1E	2E
Electrode spacing [µm]	67	35	27
Thickness [µm]	230	230	
Rad-hard [1MeV n_{eq}/cm^2]	9 x 10^{15}	1.4 x 10^{15}	



CMOS sensors

- Recently commercial CMOS technologies have become available with **HV capability on HR substrate**
  - Imaging sensors market
- CMOS sensors investigated as a possible replacement of traditional silicon sensors for hybrid pixels or to develop DMAPS detectors for the pixel outmost layer
  - Significant advantages in terms of **cost and large area production**
  - Demonstrated **adequate radiation tolerance**





Readout electronics design

Readout electronics

- Basic functionality
  - The signal from pixel and strip sensors is **integrated, amplified and digitized** by the FE chip
  - The FE chips **stores the hit information** and sends it to the detector data acquisition system upon arrival of the **trigger signal**
  - Different **readout architectures** are developed based on the rate and radiation levels

- To cope with the high hit rate, **fast readout** with **high logic density** (i.e. memory) is needed

- Smaller feature size **CMOS technologies** are used for the ITk
  - **65 nm** CMOS for the pixel FE (130 and 250 nm in ID pixel)
  - **130 nm** CMOS for the strip FE (250 nm in ID strip)

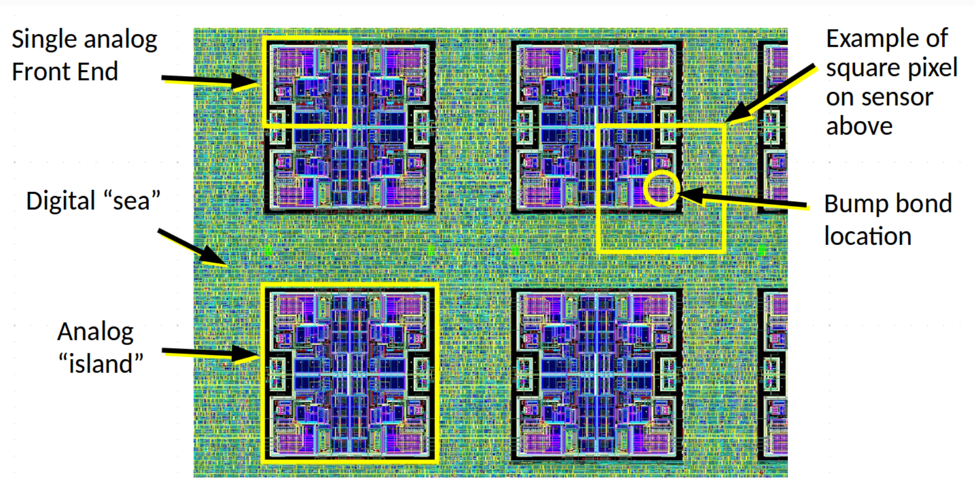
Radiation hardness of CMOS technologies

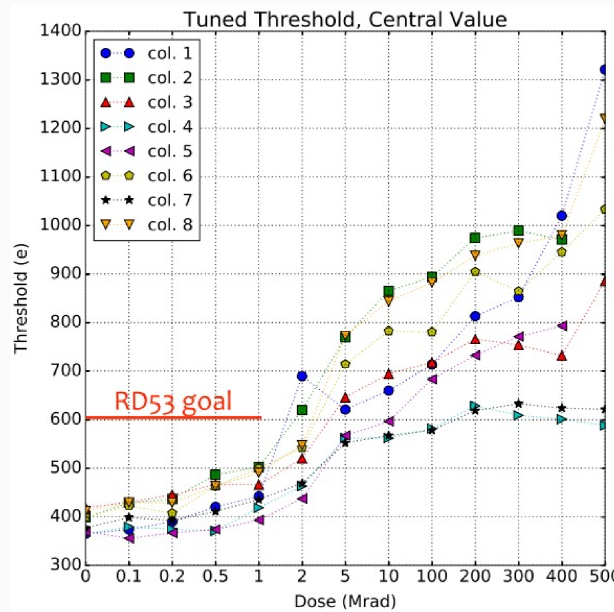
- **Total ionising dose** effects
  - Charge trapping in thick isolation oxides and at the oxide-silicon interfaces lead to degradation of the performance of MOSFETs transistors
  - Dependent on dose rate and temperature history of the FE (annealing)
- Single Event Effects, **SEE**
  - Local ionisation effects that change the status of memory cells
- Deep submicron CMOS technologies provide adequate radiation tolerance provided mitigation strategies are put in place
  - Pixel innermost layers will be **replaced after 2000 fb^{-1}**
  - Strip detector **operational T profile** devised to reduce the effects of TID
  - **Triplicated logic** and **reset schemes** to protect against SEE

	TID [Mrad]
Pixel	10^3
Strip	50

Readout for HL-LHC innermost layers

- Very innovative design based on a new readout architecture
- Analog "islands" in a digital synthesized "sea"
- Collection of large digital cores containing many regions
  - Complex functionality in the pixel matrix
  - Resources shared among many pixels
- 2 dimensional digital connectivity
- Smart clustering in the pixel matrix to send most information with least bandwidth (5.12 Gbps/chip)



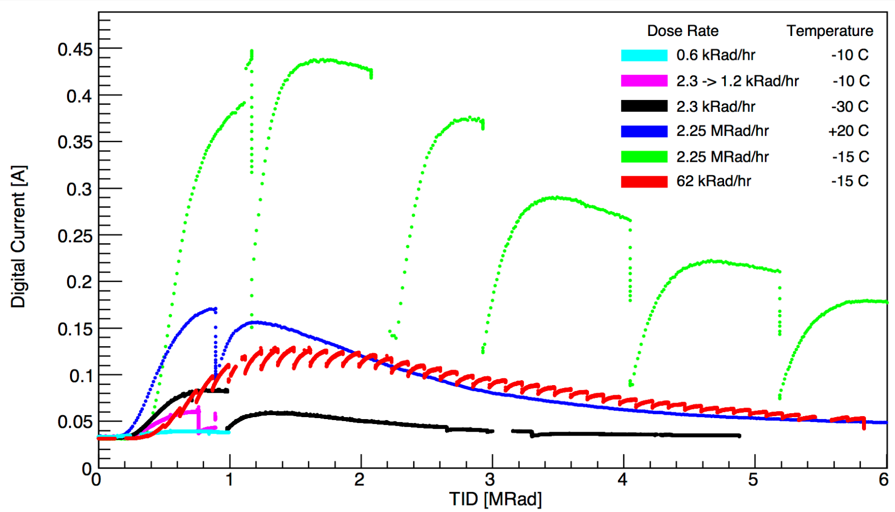


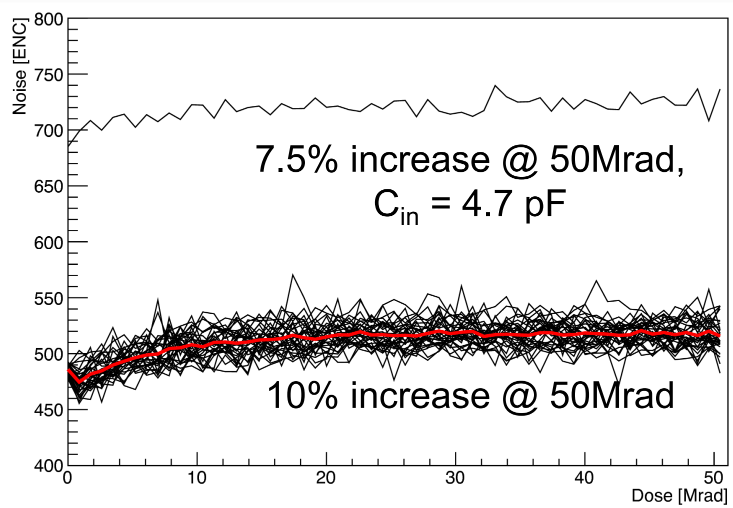
Strip FE readout chip: ABCStar

- 256 readout channels with binary readout
- Design compatible with multi-level trigger scheme (increased buffering per channel)
  - Single Level- 0 trigger (L0) at 1 MHz with a maximum latency of 10 μs
  - L0-L1 trigger: information from ITk used as input for a second level L1 trigger signal combined with calo and muon data
  - L0 readout at 1 MHz for 10% of the modules belonging to the Region of Interest (RoI) identified at L0, followed by full read-out at L1 at 400 kHz
- LCB protocol
  - L0, commands, and bunch crossing ID sent in one encoded data stream designed to allow triggering on 4 consecutive bunch crossings
- L0 tag
  - The L0ID is generated by the DAQ and attached as a tag to the L0
  - Modules receive the L0ID and send back data with this identifier
  - Errors affect only one frame (i.e. 4 triggers)
  - No need for synchronized counters in chip and DAQ

Strip FE TID characterization

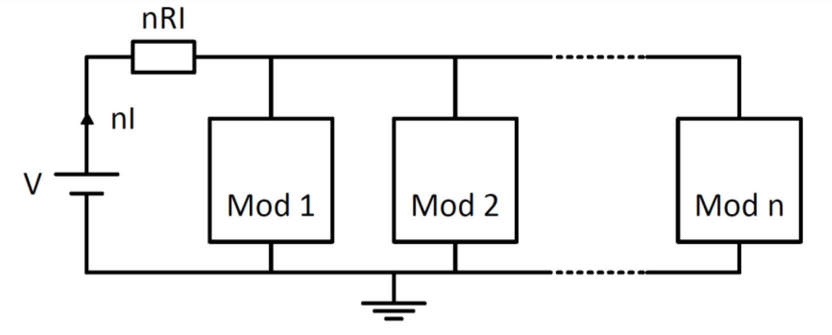
- Low temperature, low dose rate irradiations show a current evolution with TID compatible with the radiation induced narrow channel effect typical of 130 nm CMOS technology node
  - Current increase due to positive charge trapped in the later STI
  - Current decrease due to later built-up of negative interface states
  - Effect well characterised, model available to predict current peak at different T and dose rate
- FE noise increase with TID mitigated by the use of enclosed layout transistors





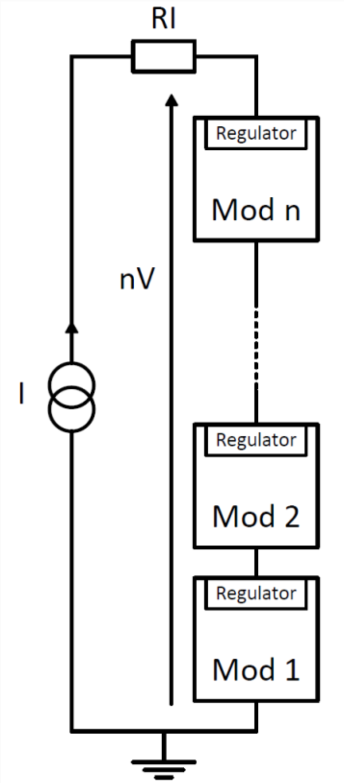
Lightweight services

Power distribution



- Tracking detectors for high rate environments are power hungry devices → **high current consumption**
- Traditional tracking detectors power distribution scheme
  - Each module is powered independently with a constant voltage
  - **High number of long cables with large cross section**
  - At the LHC cable channels are saturated, services dominate the material budget, power efficiency is below 50%
- Readout electronics design for the HL-LHC optimises power consumption against rate requirements but given the larger number of detector channels, the power consumption will be higher than then ID → New powering schemes are needed to **reduce the transmitted current**
  - **Serial powering** for the pixel detector
  - **DC-DC conversion** for the strip detector

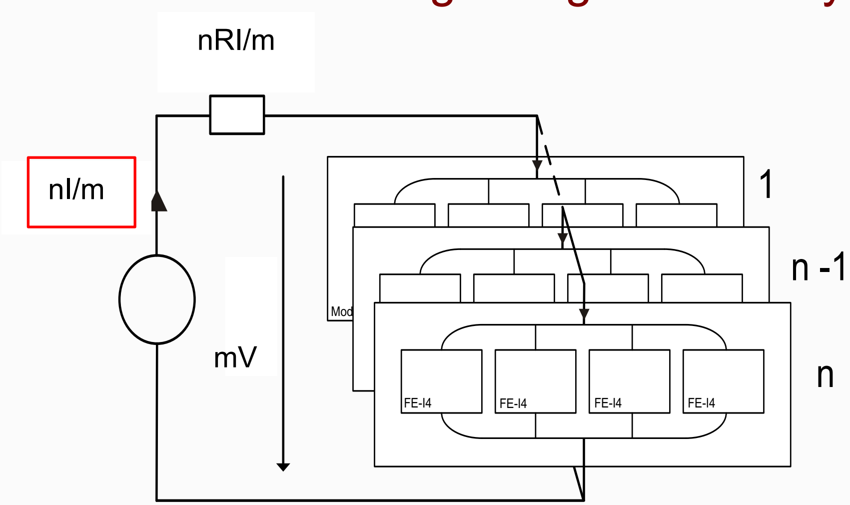
Serial powering for pixels

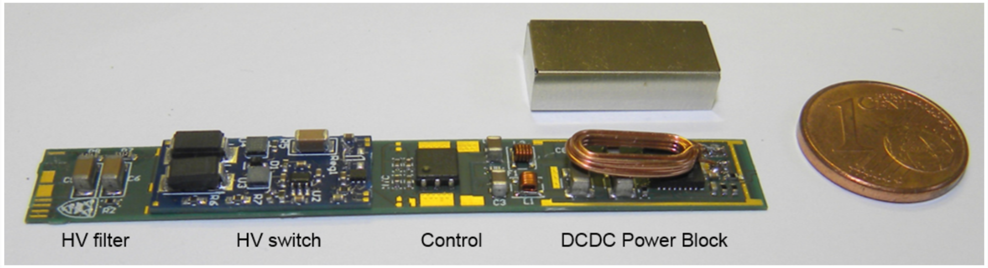


- Current based powering scheme
  - N nodules are powered in series by a **constant current = current for one module**
  - Voltages are generated by **regulators on-chip**
- Wrt. a conventional voltage based powering scheme the transmitted current scales of a factor N: **I → I/N**
  - Smaller cable cross section
  - Reduced power losses on the cables
- Number of modules in the chain is a trade-off between redundancy, quality of data transmission, and amount of cables
- Dedicated developments
  - **Integrated regulator** to convert input current to stable voltage for FE chips, Shunt-LDO
  - Bypass chip to disconnect faulty modules from the chain
  - Both need to meet the radiation requirements

DC-DC conversion

- Power transmitted at high voltage and low current to the modules
- **x2 DC-DC buck converter** on module
  - Radiation-hard tolerant converter development by CERN PH-ESE group
- Optimised integration of regulator and coil on power board to **shield module from EMI**
  - Solenoidal flat coil geometry to fit into available space
  - Shield made of a mix of aluminium and copper
  - Demonstrated electric and magnetic fields shielding whilst still maintaining a target efficiency of 75% at the nominal load of 2 A





ITk production

Production of a $200m^2$ silicon tracker

- The production of the ATLAS ITk is a challenge as much as the R&D to identify the right technologies and design for the components
- **Quality control and quality assurance**
  - Assure component reliability in extreme experimental conditions
  - Monitor rate and quality of production to detect problems that may arise and stop production
- Industrialised **production flow**
  - Common tooling development and assembly procedures
- **Database**
  - Store information from all detector elements QC and QA during production
  - Track the geographic location and utilisation of all parts during construction
  - Debugging of faulty conditions during operation

Conclusion

- To benefit from the physical potential of the HL-LHC the ATLAS experiment is preparing the replacement of its inner tracking system
- The new, all-silicon Inner Tracker (ITk) maintains and in some cases improves the tracking performance of the ATLAS detector while coping with 200 pile-up events per collision
- Radiation tolerant sensor and readout electronics prototypes have demonstrated the required functionality
- Production is due to start in 2020 for the strip detector and in 2021 for the pixel detector. The 200m^2 ITk detector will be produced in three years.