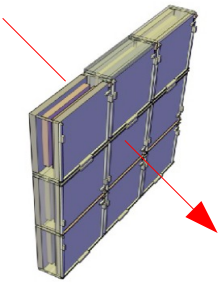


ASAP

Array of Silicon Avalanche Pixels

Development of a vertically integrated CMOS position-sensitive detector for charged particles

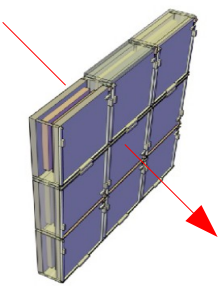
The ASAP Collaboration

P.S.Marrocchesi[1] (Coordinatore Nazionale INFN)
P.Brogi[1], C.Checchia[2], G.Collazuol[2], G.F.Dalla Betta[3],
A.Ficorella[3], F.Morsani[1], M.Musacci[4], L.Pancheri[3], L.Ratti[4],
A.Savoy-Navarro[5], L.Silvestrin[2]…

1) University of Siena & INFN Pisa
2) University of Padova & INFN Padova
3) University of Trento & TIFPA
4) University of Pavia & INFN Pavia
5) University Paris-Diderot/CNRS Paris

Overview

- **latest results** (APIX → ASAP)
  focussing on local group achievements
- **perspectives 2019**
  - 2nd chip characterizatoin + beta probe
  - 3rd chip → timing



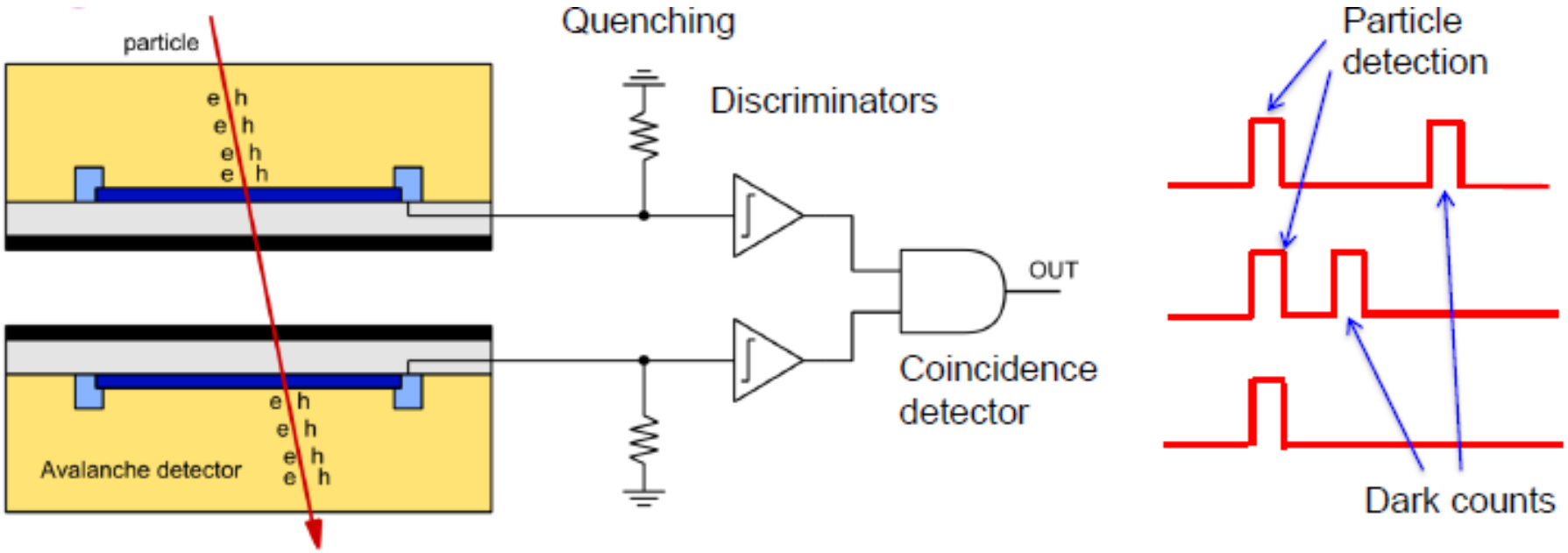
APIX/ASAP particle detector concept

Innovative Silicon tracker

1) thin sensitive volumes (pixels)

2) large signals (enhanced S/N)

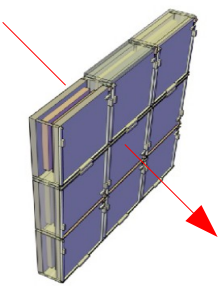
- reduced material budget
- reduced power consumption
- "simple" electronics → digital readout
- high rate capability
- high timing resolution



- Two Geiger-mode avalanche detectors in **coincidence**:

  $DCR = DCR_1 \times DCR_2 \times 2\Delta T$

- In-pixel coincidence: integrated electronics is needed:
  CMOS avalanche detectors



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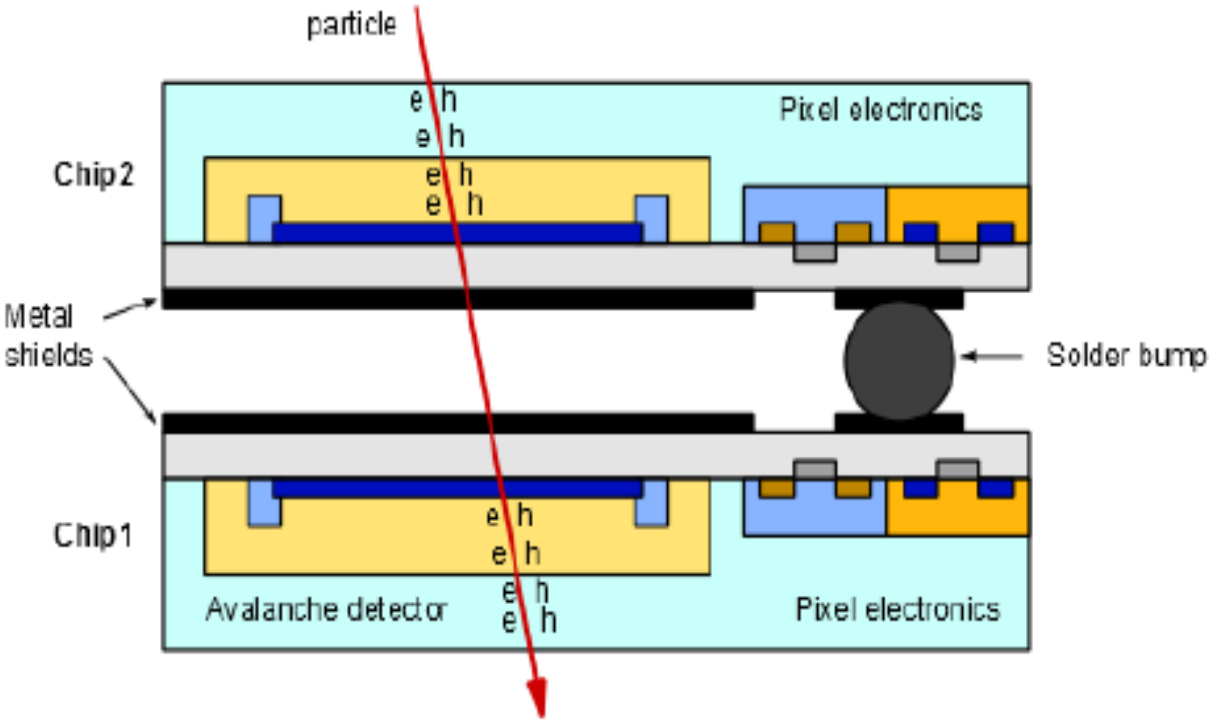
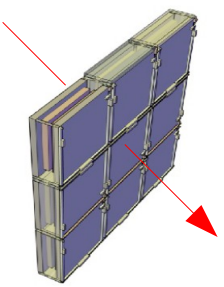


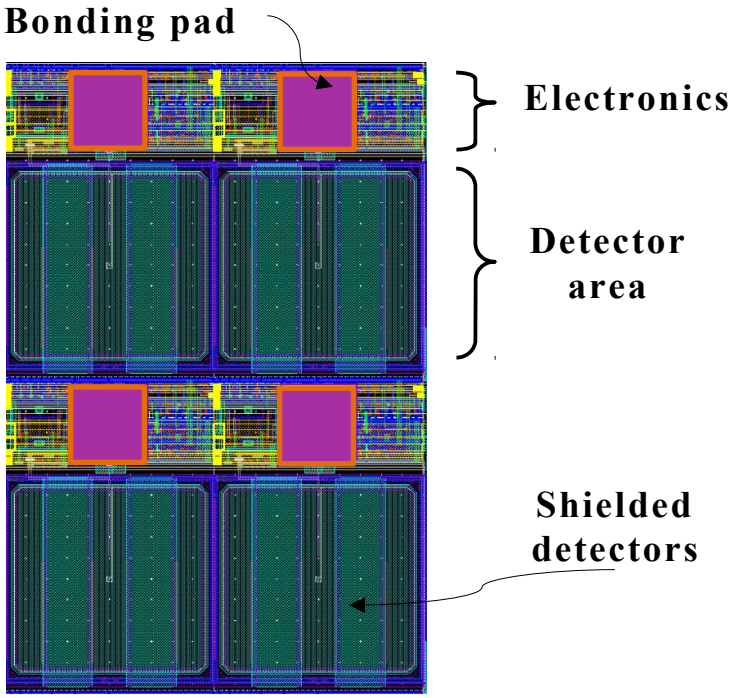
2-layer pixel cross section:

- Electronic readout on both layers
- **Metal shielding** from optical cross-talk
- Vertical interconnection by **bump bonding**

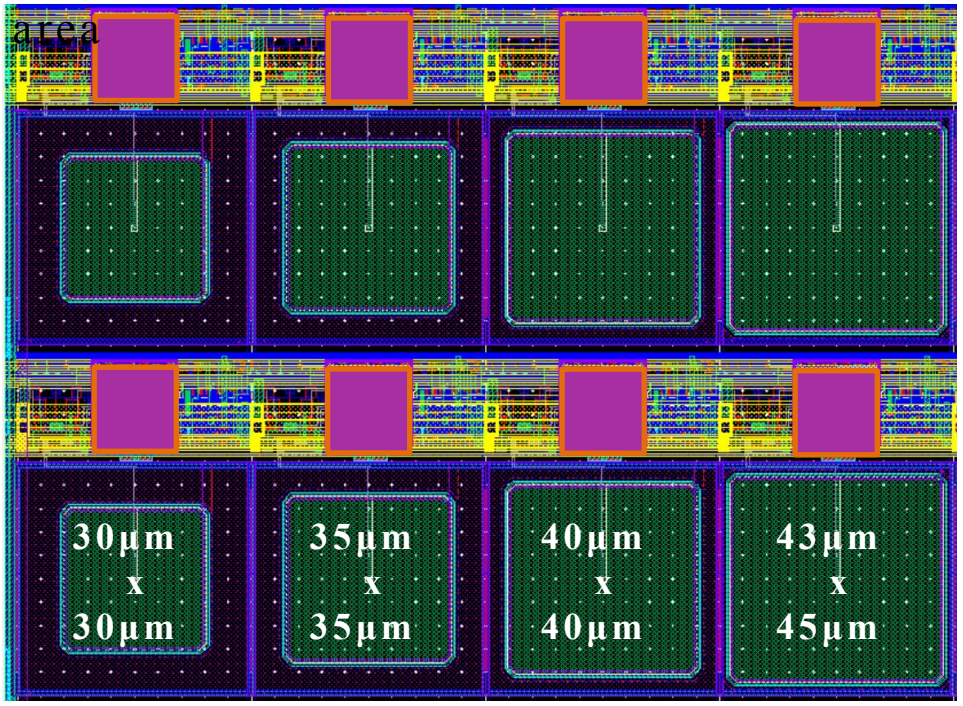


APIX pixel array (1st prototype chip)

- Sensor array of 16 rows x 48 SPADs
- Pixel size: 50 µm x 75 µm
- Total sensor dimensions: 1.2 x 2.4 mm^2

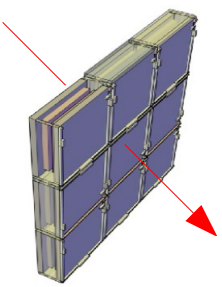


Unshielded pixels with different active area



Array partitioning:

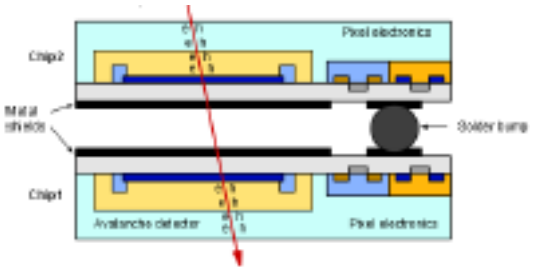
- Two SPAD types: p+/nwell and p-well/n-iso
- Different SPAD active areas: 30 – 35 – 40 – 45 micron side
- Some unshielded structures for testing with light
- Coincidence between SPAD with the same size and with different sizes

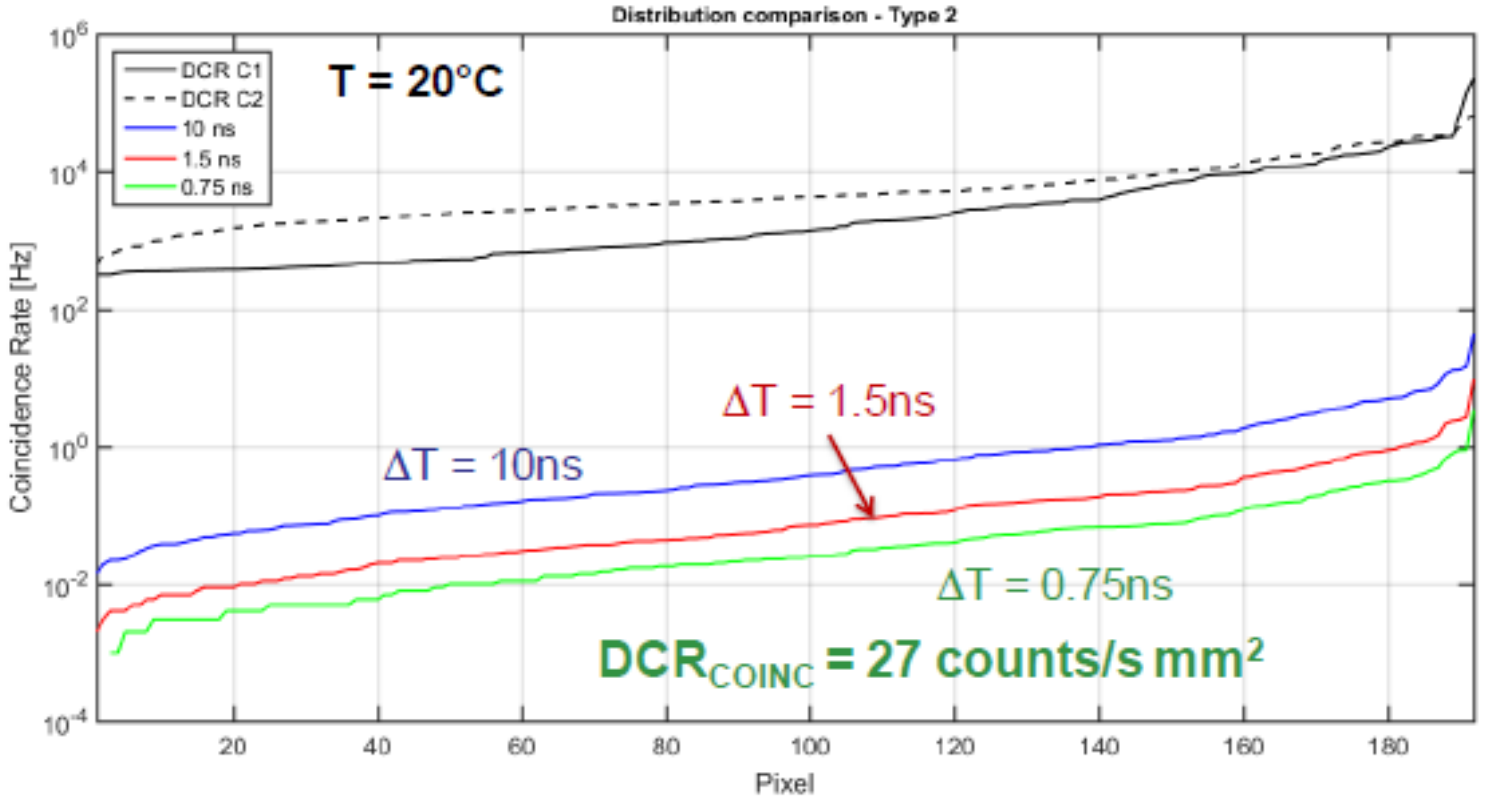


DCR – vertically integrated assembly

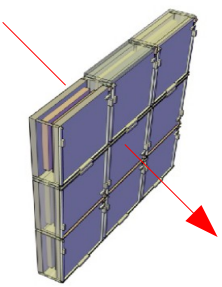
Dark Count Rate vs. coincidence time ΔT

$$DCR_{COINC} = DCR_1 \times DCR_2 \times 2\Delta T$$

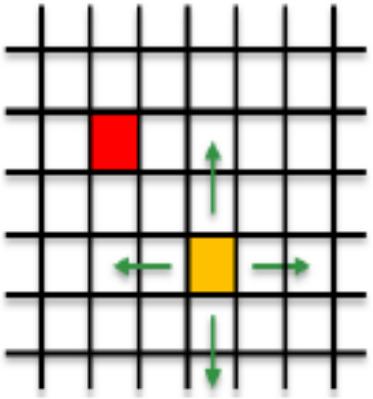




Dark count rate lower than expected



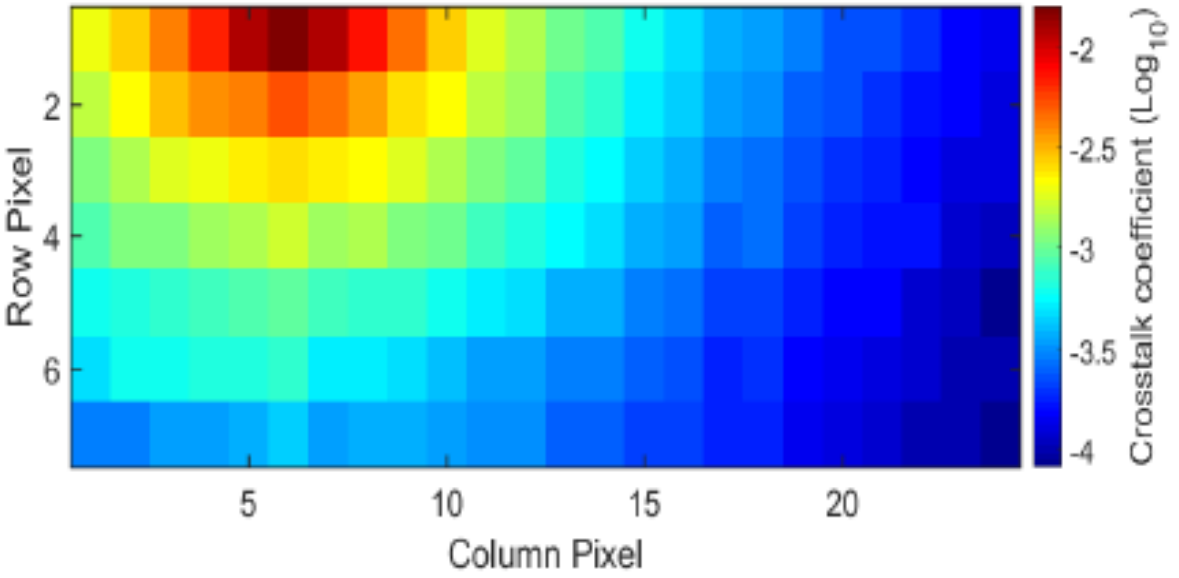
Optical cross-talk



- Crosstalk coefficient

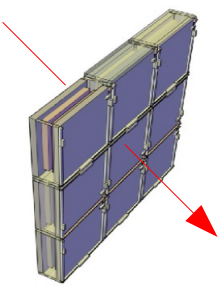
$$CR_m = DCR_e \cdot DCR_d \cdot 2\Delta T + \mathbf{K} \cdot (DCR_e + DCR_d)$$

- **Emitter** (fixed)
- **Detector** (scan)



Crosstalk map – Type 1, 25µm thickness

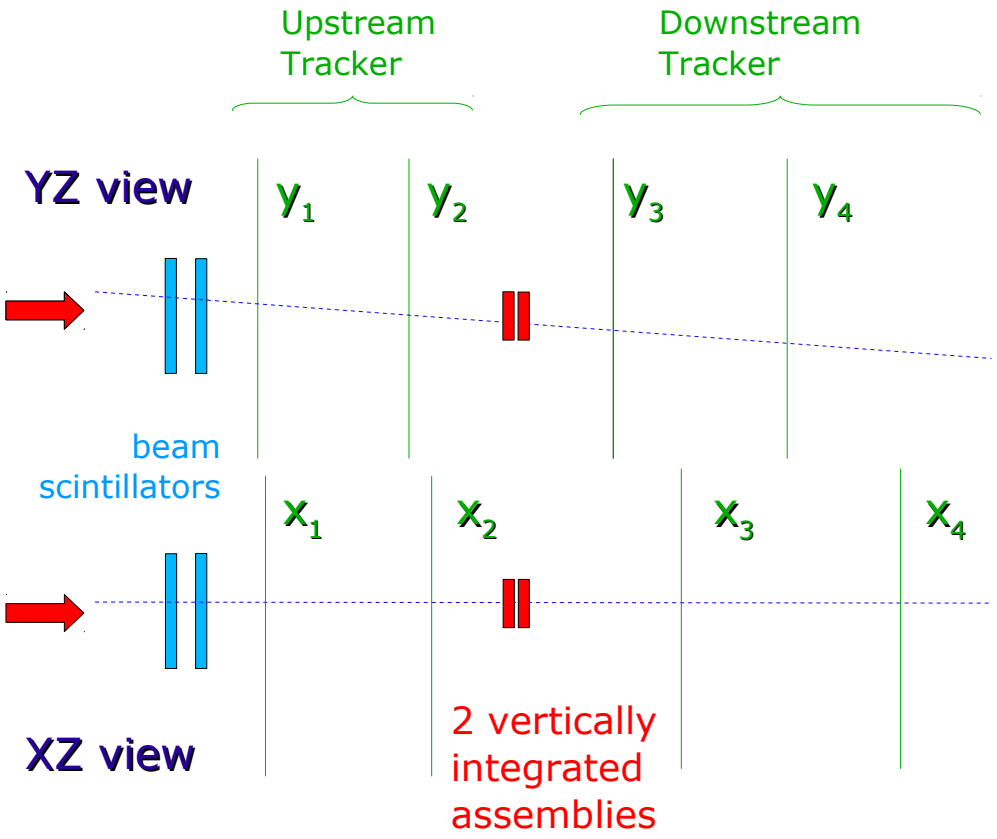
Optical cross-talk as expected → O(%)

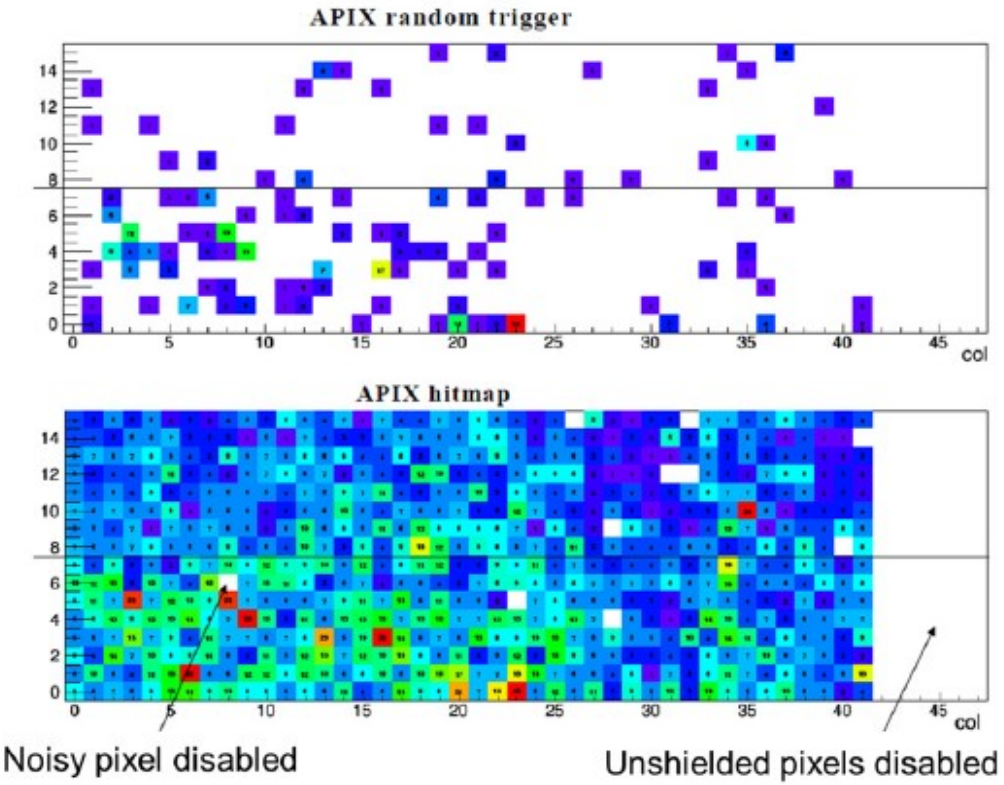


Pixel efficiency - high energy protons

Test Beam @ CERN – Sept 2016

→ two vertically integrated assemblies exposed to 400GeV protons

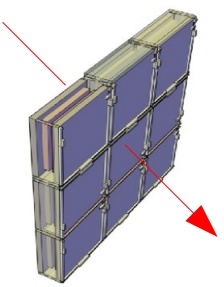




Top: DCR (coincidence) map
Bottom: Beam rate map

- top/bottom chip alignment at level better than 3μm
- pixel efficiency ≥ geom Fill Factor → charge "diffusion"

→ New Test Beam with hi-res tracker (2018 Sept.)

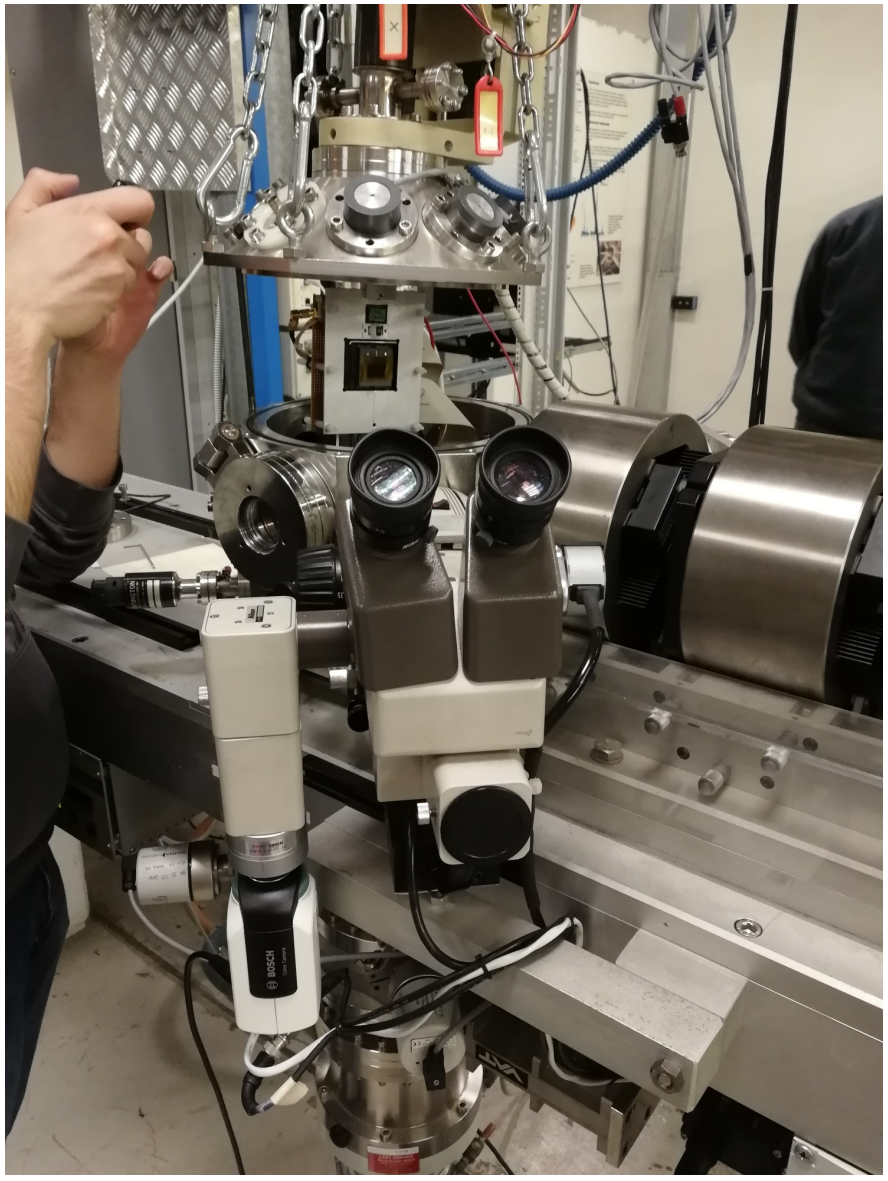


Pixel efficiency & Rad hardn. - 2MeV p

Test Beam @ AN microbeam (LNL) – Jan 2018

→ single bottom chip exposed to 2MeV protons

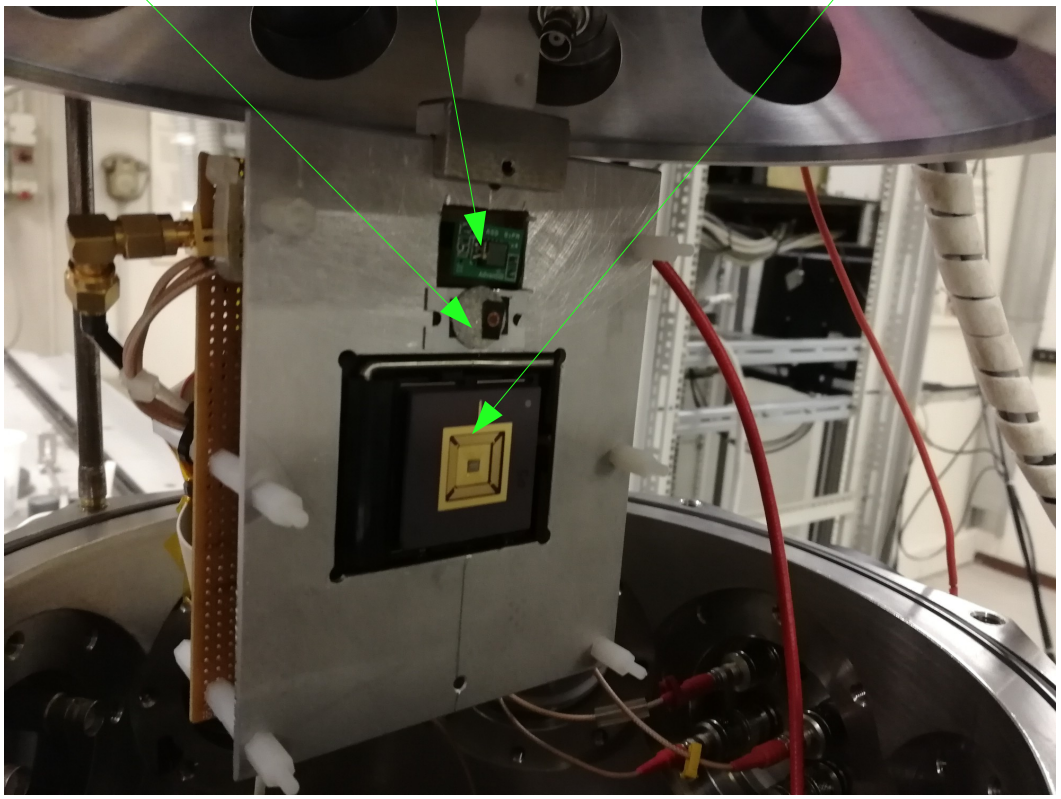
collaboration and sinergy w/ ASIDI project

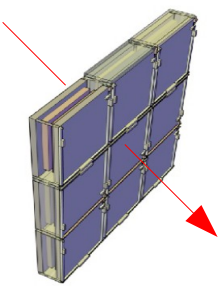


SiPM with p-terphenil scintillator layer deposited (200μg/cm²)
→ single proton count
→ beam intensity tuning

Alumina & Cu grid
→ coarse alignment

APIX (bottom) chip sample





Pixel efficiency & Rad hardn. - 2MeV p

Test Beam @ AN microbeam (LNL) – Jan 2018

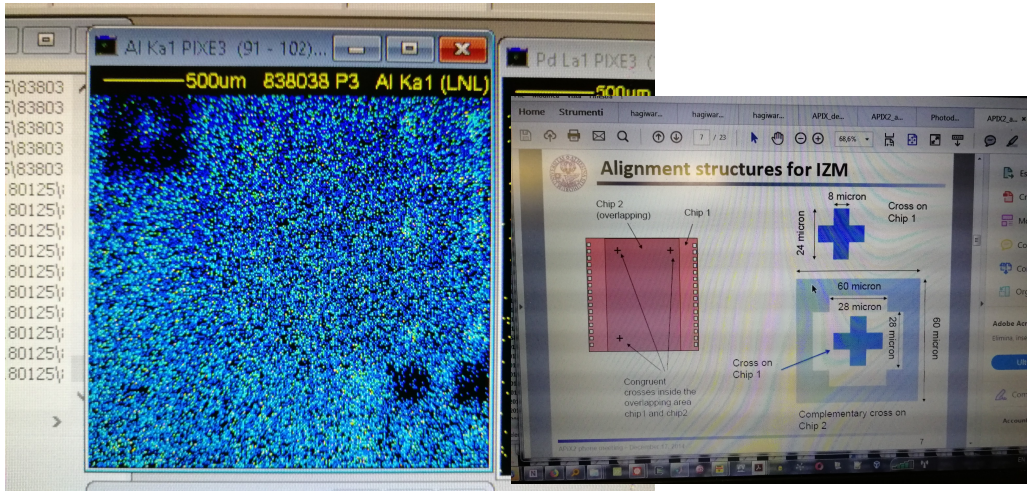
→ single bottom chip exposed to 2MeV protons

1) Optical alignment (microscope)

2) beam geometry tuning
w/ copper grid + PIXE tecnique

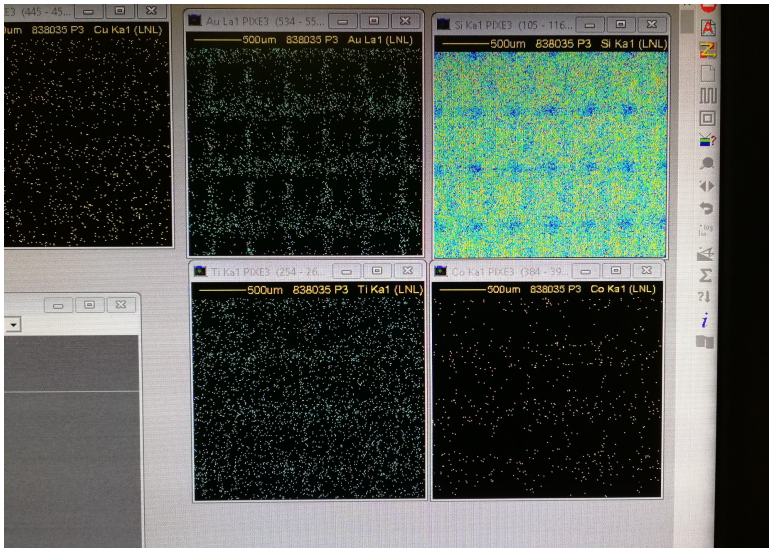
→ measured beam size < 3μm

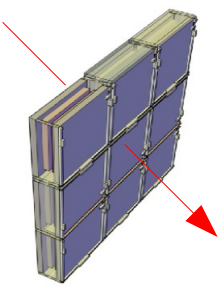
3) fine alignment w/ markers
on the sample chip (PIXE)



Note: PIXE needs relatively high intensity beam...

NOTE: PIXE → chip structures

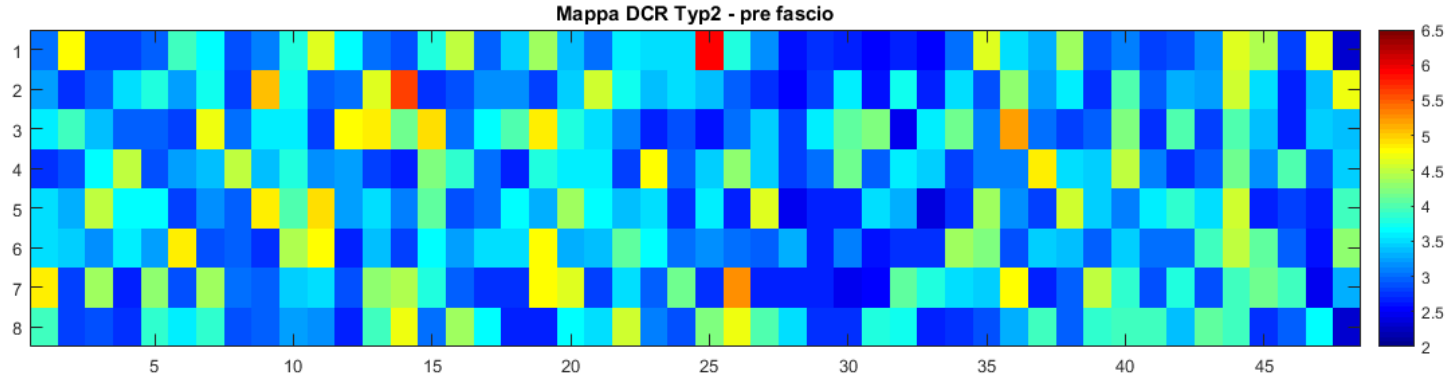


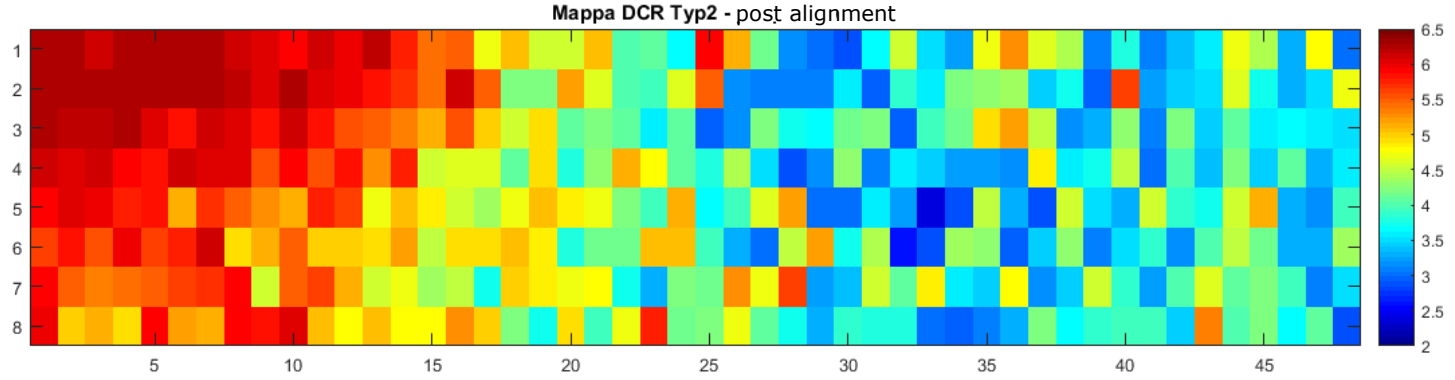


Pixel efficiency & Rad. hardness - 2MeV p

Test Beam @ AN (LNL) – Jan 2018

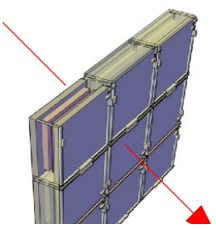
→ single bottom chip exposed to 2MeV protons





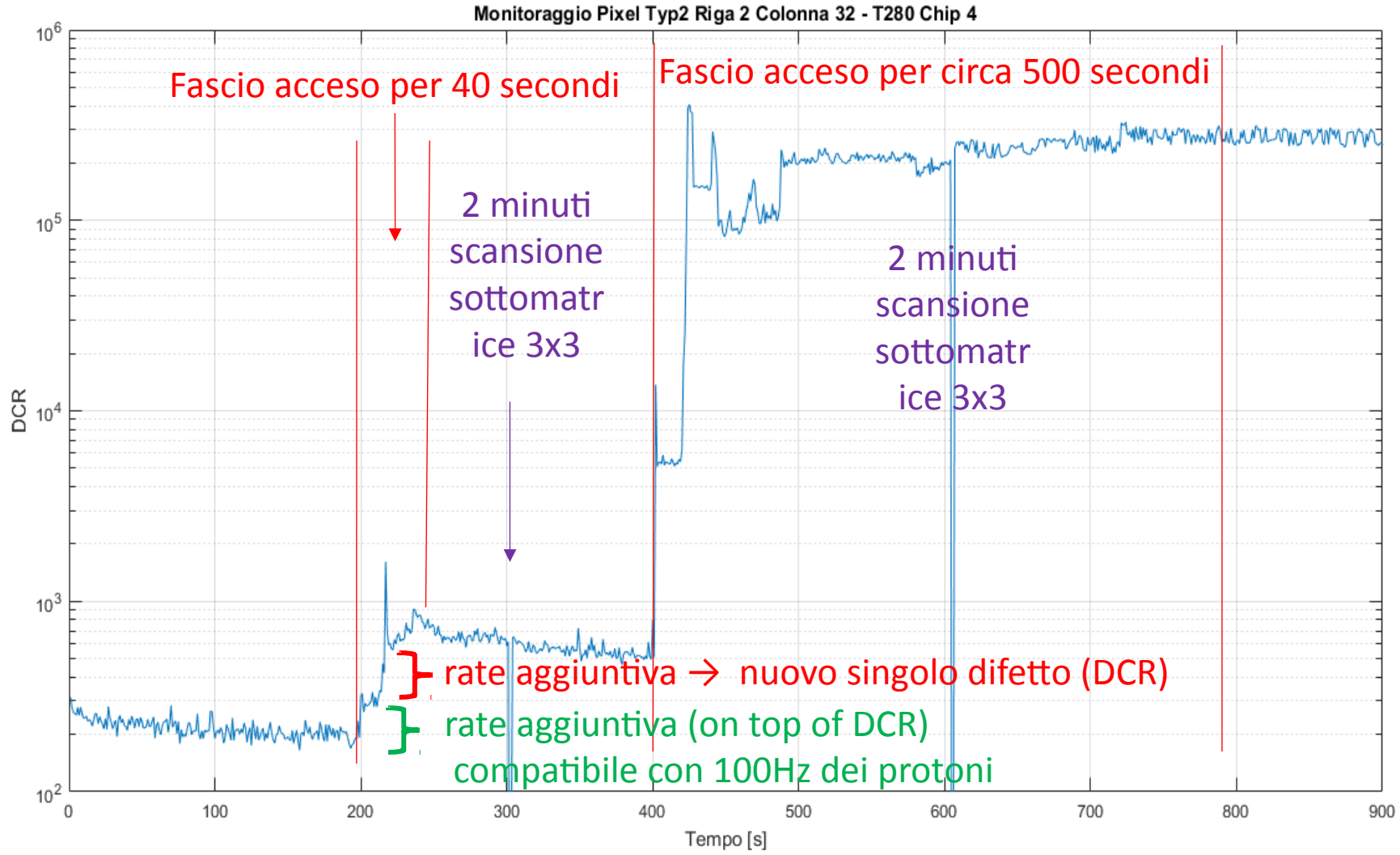
- PIXE needs relatively high intensity beam...

→ unfortunately chips are damaged during 3rd aligment phase even at large (1mm) distance from marker !!!

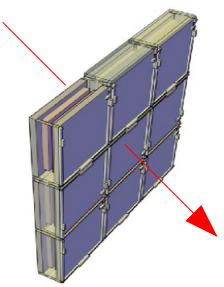


Pixel efficiency & Rad. hardness - 2MeV p

Test Beam @ AN (LNL) – Jan 2018



- APIX beam rate (on top of DCR) → OK
- new single defect setup after 10^3 protons per pixel clearly seen
  → efficiency difficult to measure (rate tradoff rad damage vs DCR)

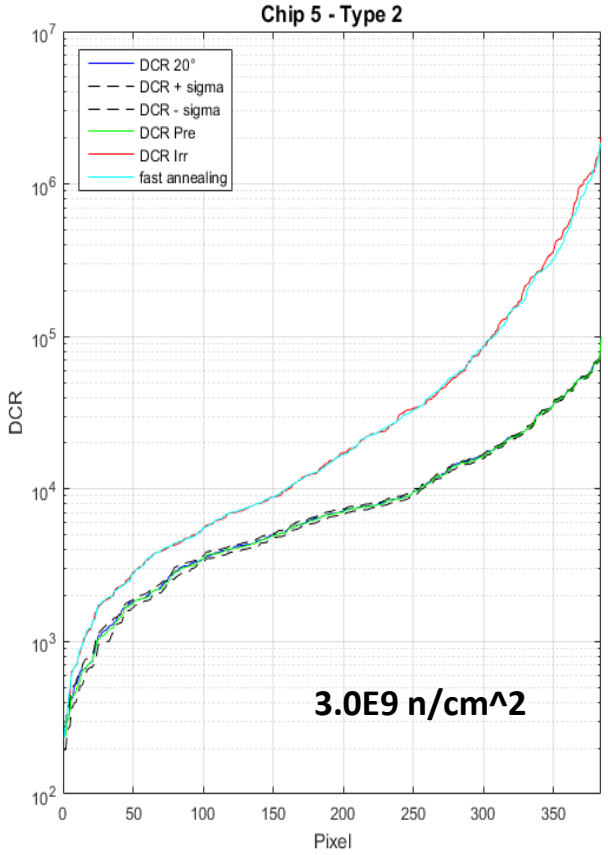


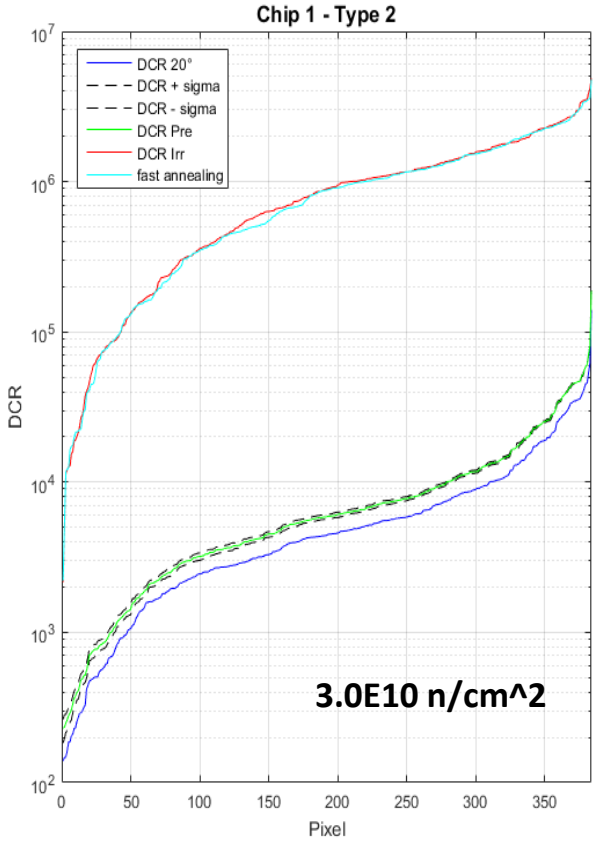
Pixel efficiency & Rad. hardness - 2MeV p

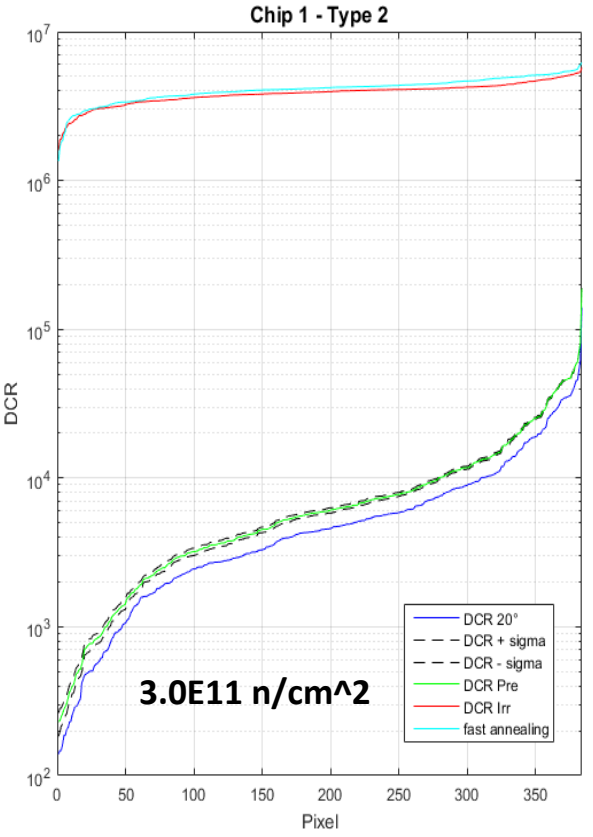
Test Beam @ CN (LNL) – Jun 2017

Protoni con energia 5 MeV: neutroni da Be target (spettro tra 0.5 e 3 MeV)
fluenza max raggiunta: 3 x 10^{11} n_{eq}/cm^2

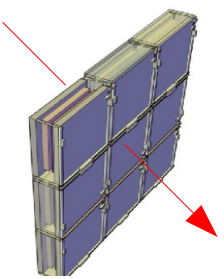
Distribuzione DCR pre-irraggiamento e post-irraggiamento a diverse fluenze
Per alti DCR c'è una saturazione a qualche MHz dovuta al tempo morto dei detector (> 100ns)





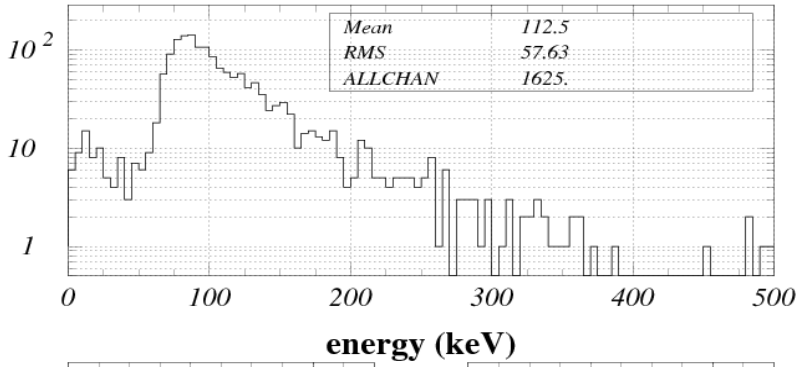


- … Silicon devices with internal multiplication suffer enhanced radiation damage … to be investigated further

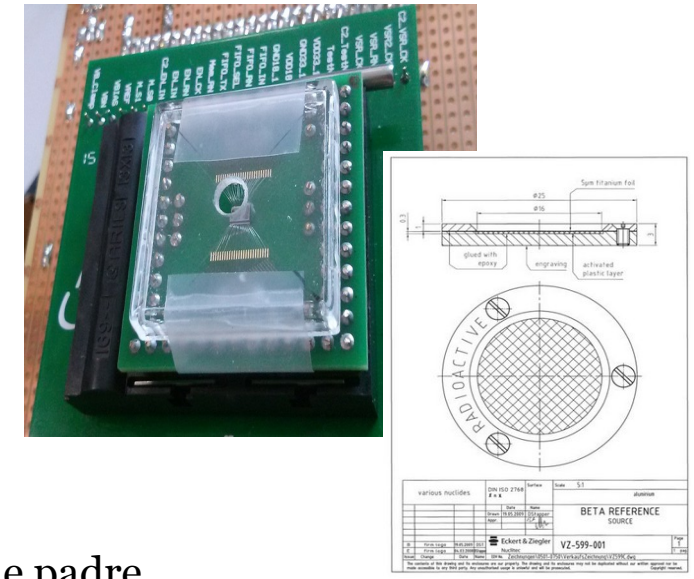


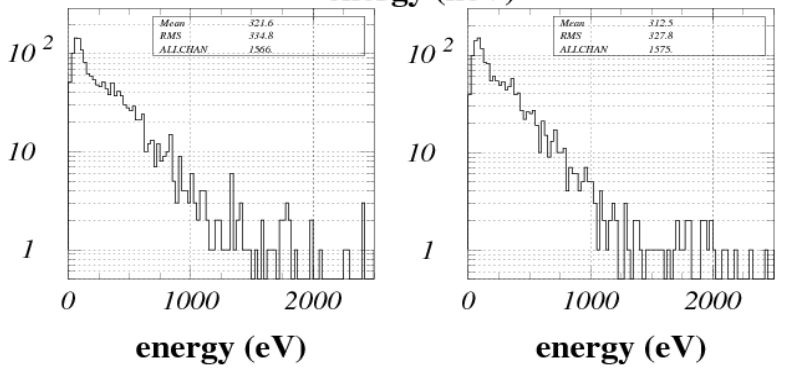
Measurements with beta-source on a vertically integrated assembly

Depositi di Energia per particelle che danno coinc. Padre*Figlio

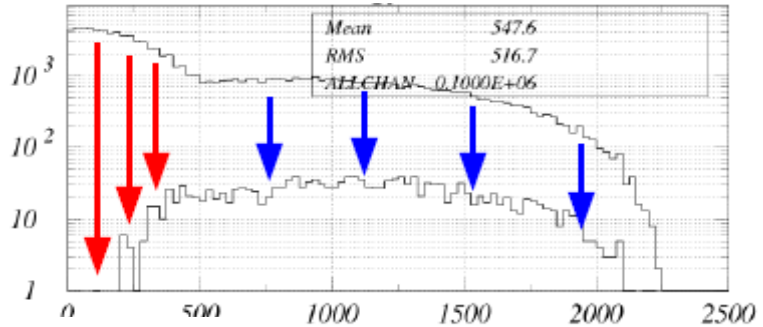


a) in bulk figlio
<dE> ~ 115keV
RMS_E~50keV





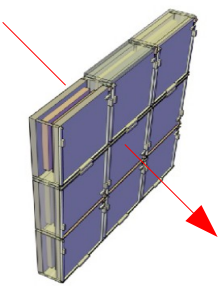
b) in zona attiva di figlio e padre
<dE> ~ 320 eV
RMS_E ~ 320 eV



Perdite per
- accettanza
- assorbimento in bulk figlio

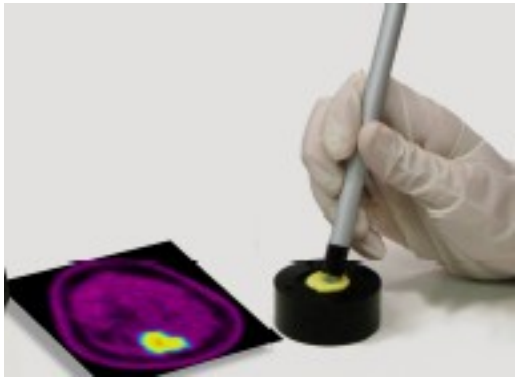
Risultati: rate misurato ~ 7Hz in agreement @ 10% con rate simulazione

Note:
- bkg sottratto
- source 39kBq

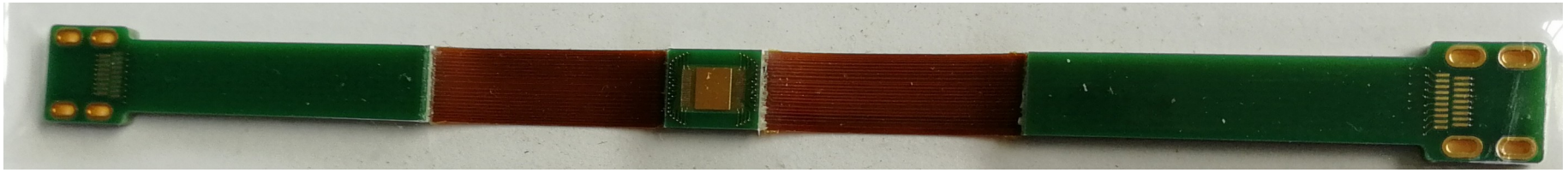


ASAP application low energy/small surface

→ Intraoperative imaging beta probe for radio guided surgery

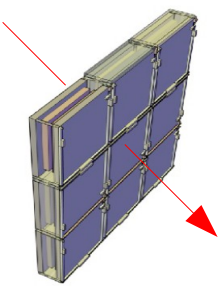


- high density rigid-flex pcb designed at INFN Pd (thanks to F.Fabris and M.Nicoletto)



- chip to be bonded (INFN PD) and PCB connected to readout electronics (INFN-PD → G.Rampazzo, M.Bettini and G.Viola)

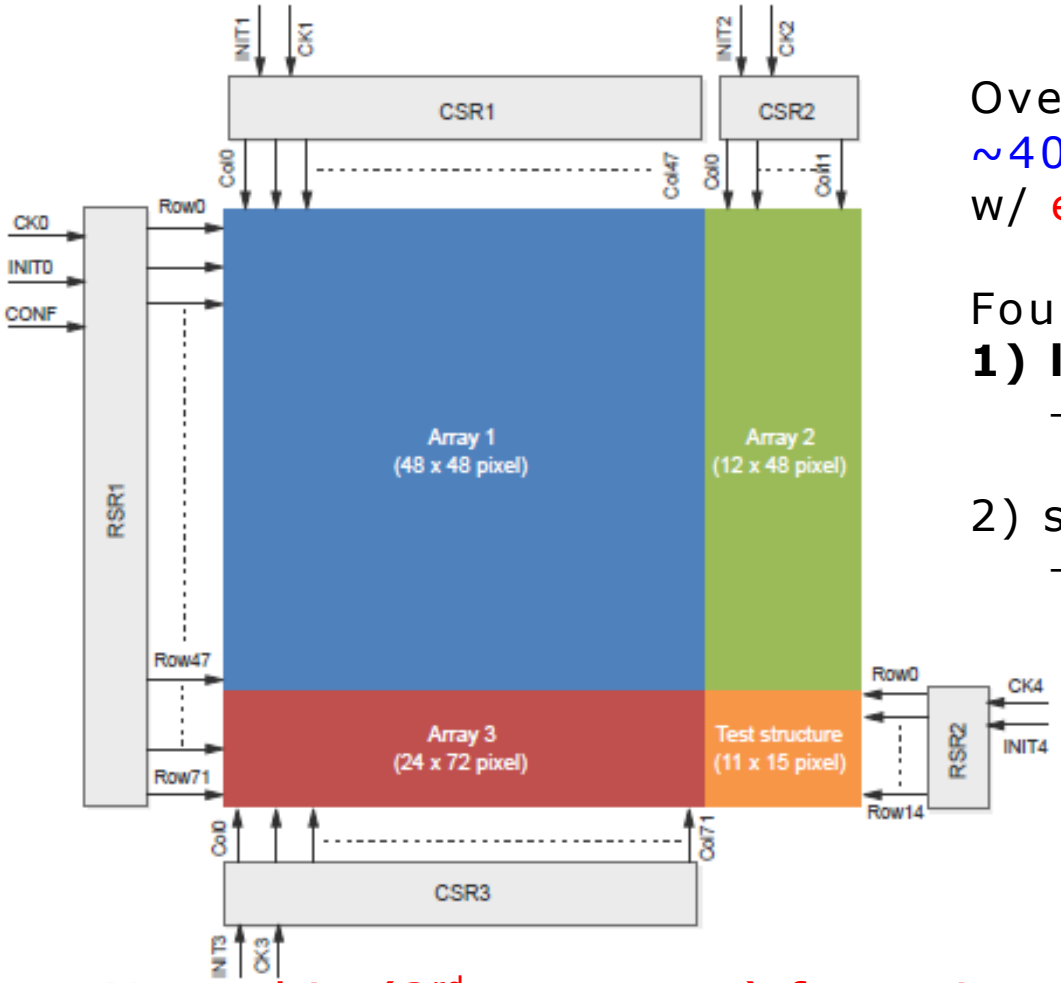
Aiming at characterization in Fall 2018



ASAP new "large" chip (2nd prototype)

Da esperienza 1st chip APIX → nuovi chip (top/bottom) ~ 5x5mm²
- disegnati da gruppi ASAP di TN e PV
- prodotti @Lfoundry in standard 150nm CMOS technology

Chips just arrived (in PV) → thinning (15 μm)
→ characterization within 1 year



Overall sensor dimensions: 6 x 5 mm²
~4000pixels (75x75 μm² or 50x50 μm²)
w/ enhanced Fill Factor (up to 80%)

Four sensors in arrays of SPAD:

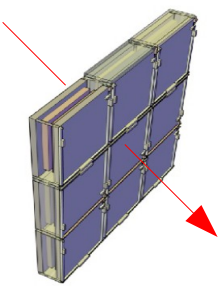
1) large sensor
→ high rate imaging applications

2) sensor with **integrated counters**
→ radio-probe applications

3) **reduced pitch** sensor
→ higher resolution imaging

4) **test structures**
→ active quenching
→ fast timing
→ radiation resistant pixels

Next chip (3rd prototype) focussing on
→ ultra-fast (ps) timing for imaging charged particles



ASAP - Padova

FTE

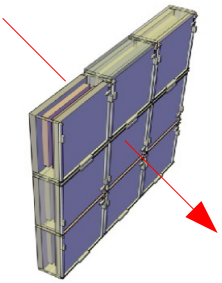
- G.Collazuol 15%
- C.Checchia 50% (Assegno J)
- L.Silvestrin 0% (al momento non associato)

Richieste PD preventivi 2019

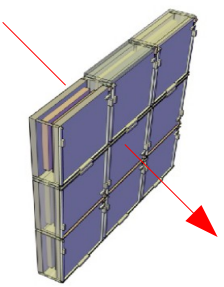
- Missioni estere 2k€
  → test beams 2019
- Consumo 7k€
  → beta probe upgrade → 2nd chip (5.5kE)
  → (completion) new high resolution silicon tracker (1.5kE)

Richieste PD servizi locali

- Serv. Elettronica: **1 m.p.** per disegno e realizzazione nuova interfaccia e beta probe
- Uff. Tecnico e Off. Meccanica: **0.5+0.5 m.p.** per disegno e realizzazione sistema per high resolution silicon tracker



Additional material



Summary APIX2

Strengths:

- Can be thinned to a **few microns**: low material budget
- **Timing resolution**
- Low **power consumption**

Weaknesses:

- Radiation tolerance
- Geometric efficiency: surface device guard ring and electronics

Opportunities:

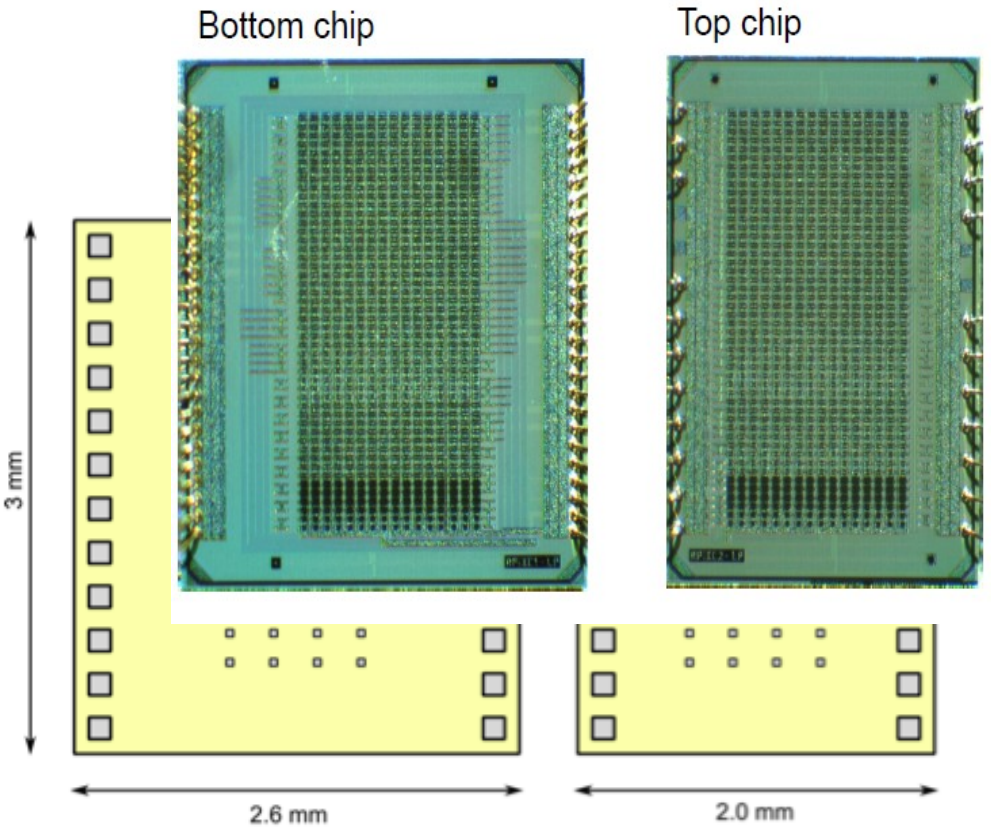
- Progress in SPAD production and **3D integration technologies**: many major foundries active

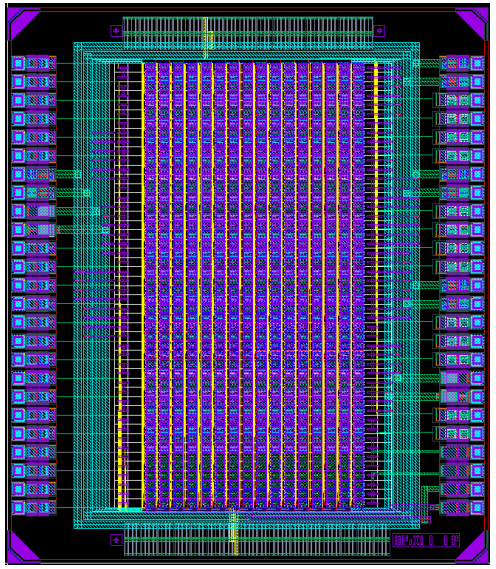
Threats:

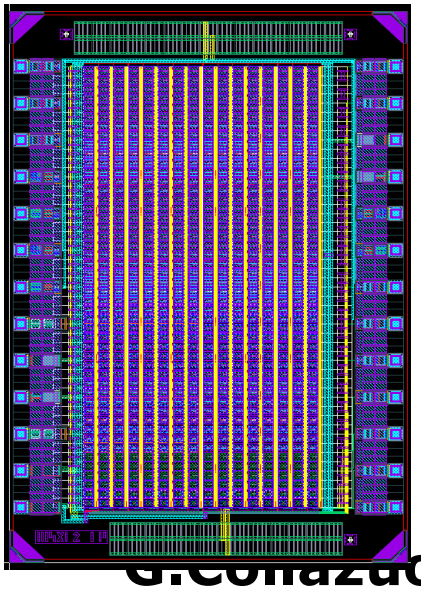
- Cost and accessibility of 3D integration processes

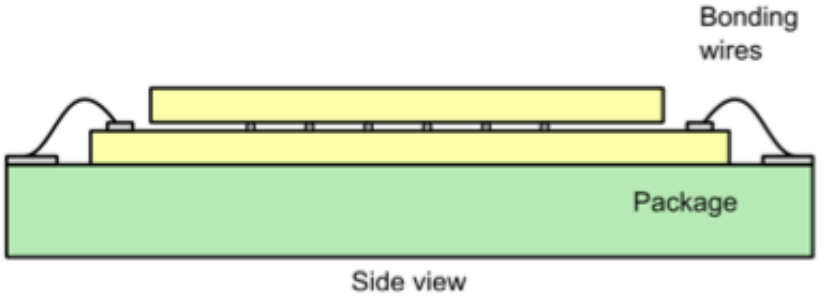
APIX array prototype

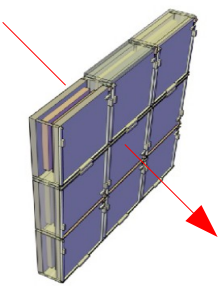
- Process: LFOUNDRY 150nm CMOS
- 2 different chips: APIXC1 ($8mm^2$) and APIXC2 ($6mm^2$)
- Vertical interconnect: **per-pixel coincidence detection**
- Chip-to-chip stacking (**micro bump bonding @ IZM**)





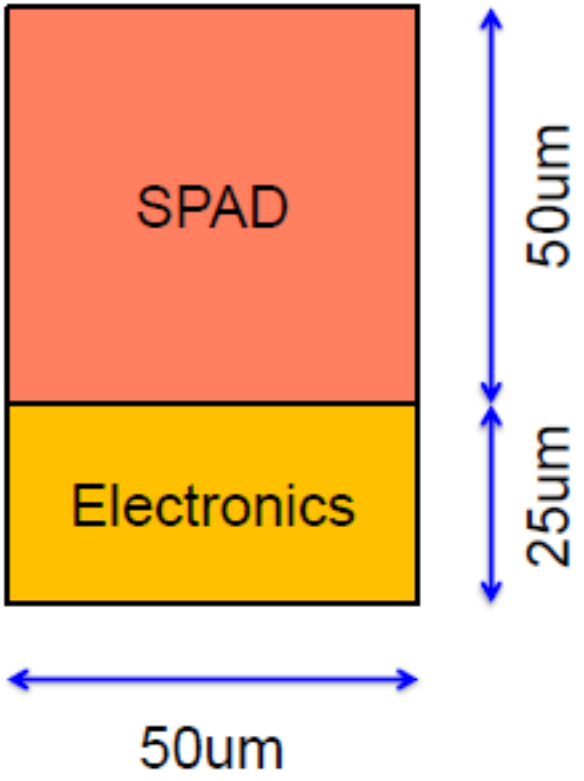




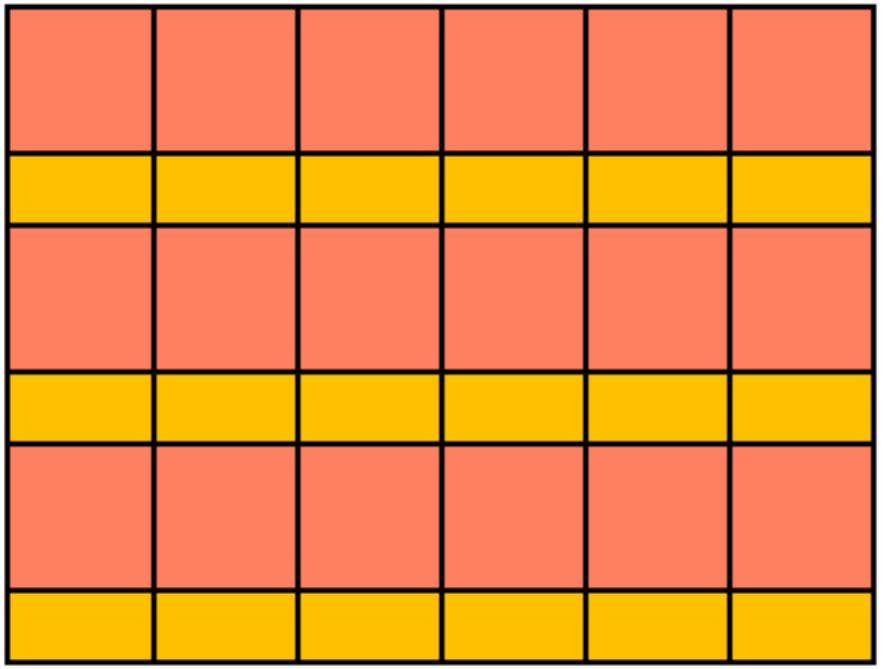


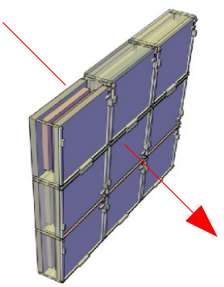
Pixel layout

Single pixel



Array arrangement

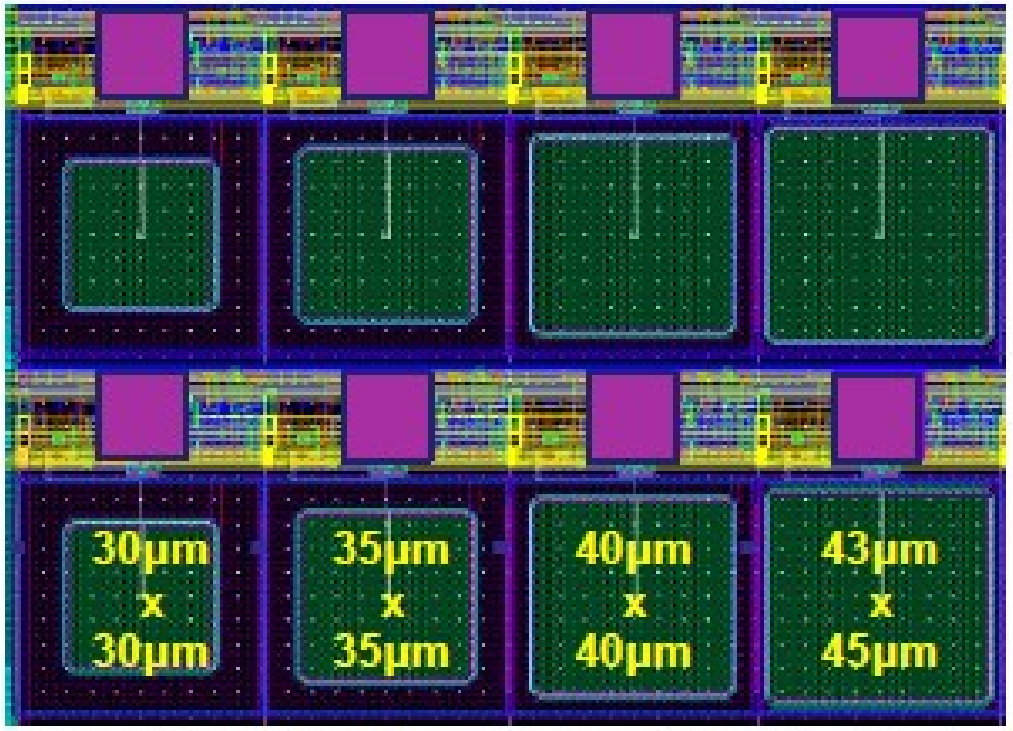




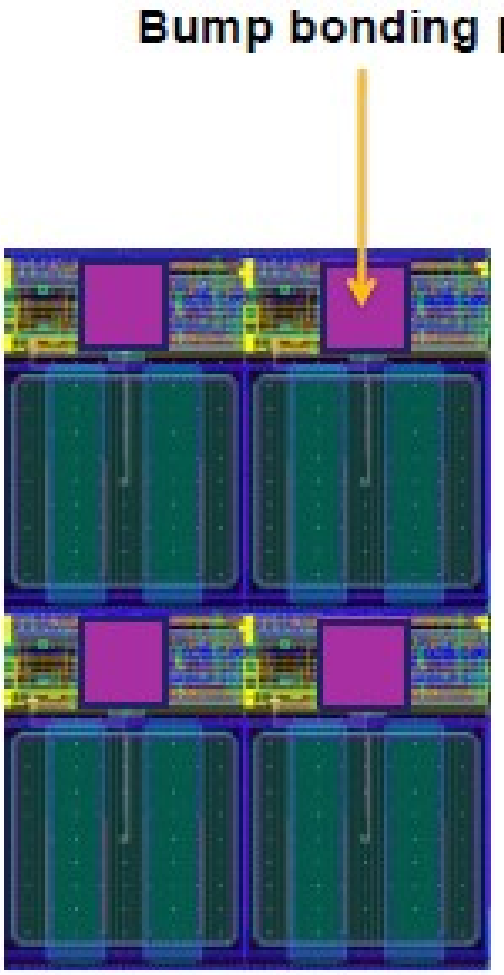
Pixel array prototype

- 16 rows: total width 16x75um = 1.2mm
- 48 SPADs per row: total length 48x50 = 2.4mm

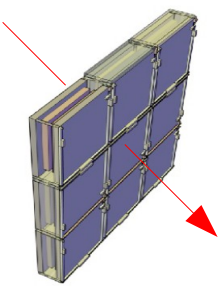
- 16 x 48 pixel array
- Pixel size: 50µm x 75µm
- Splittings in detector type and area



Pixels with different detector area (unshielded)



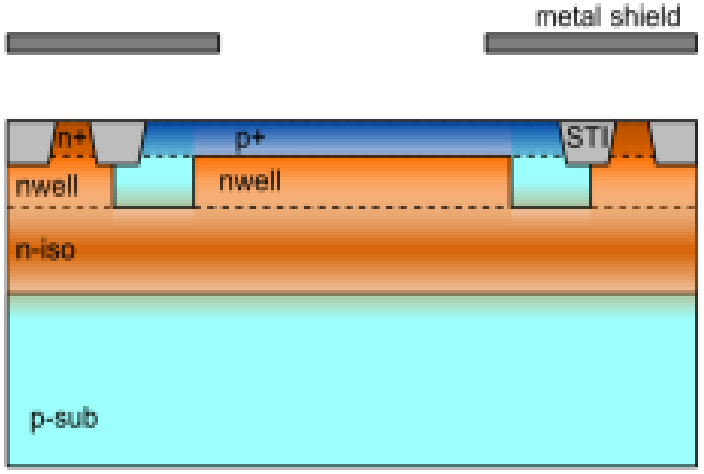
Pixels with shielded detectors



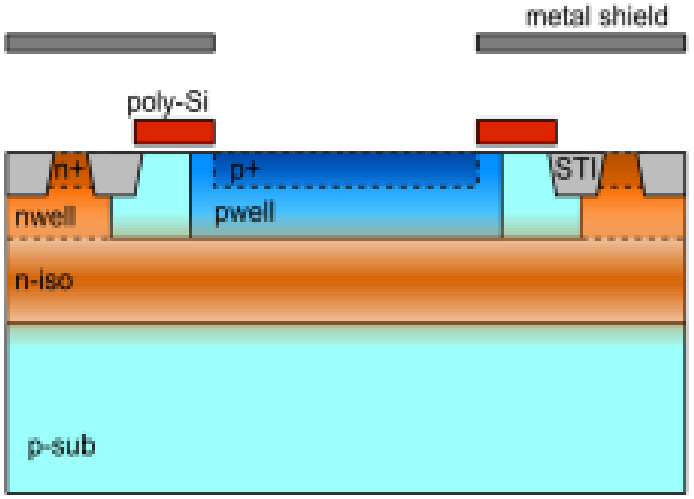
SPADs in 150nm CMOS process

- **Standard CMOS** process – no modifications
- Avalanche diodes in deep nwell: **isolated from substrate**

p+/nwell



pwell/niso

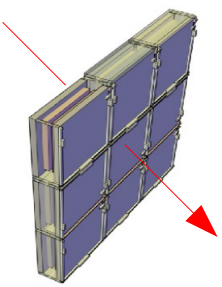


Type 1:

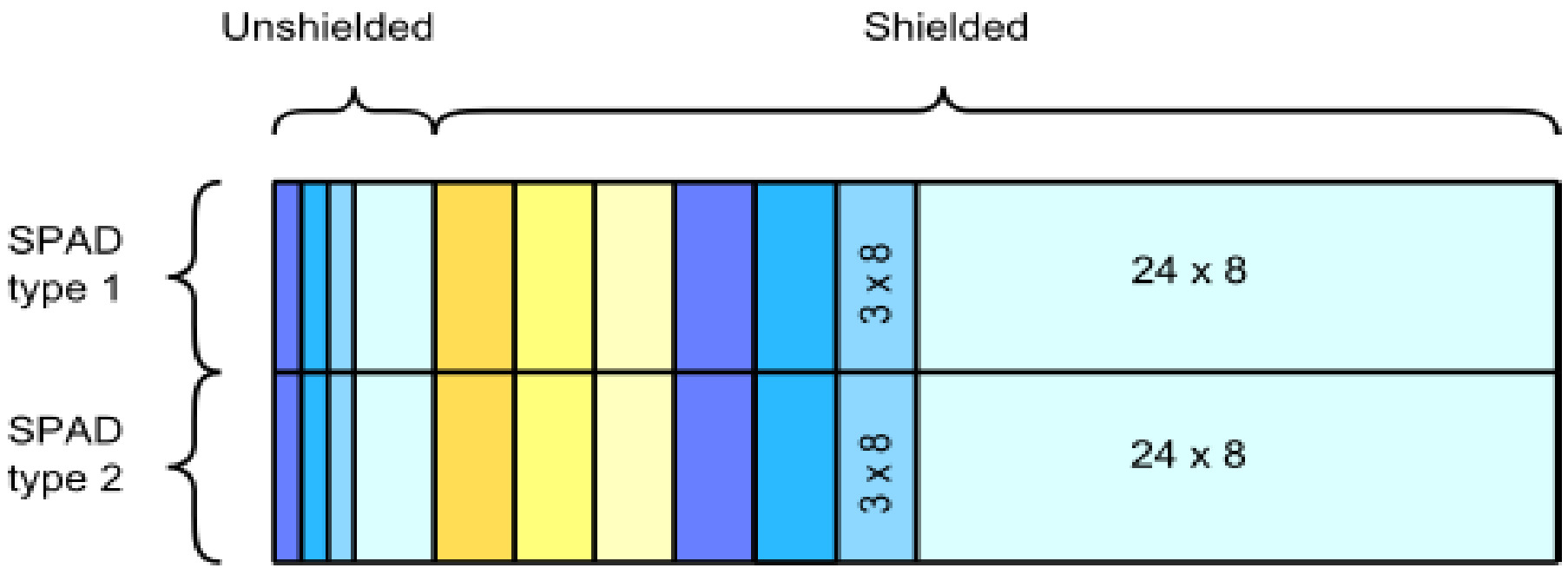
- Shallow step junction
- Active thickness ~ 1µm

Type2:

- Deep graded junction
- Active thickness ~ 1.5µm



Array partitioning



Array size: 48 x 16

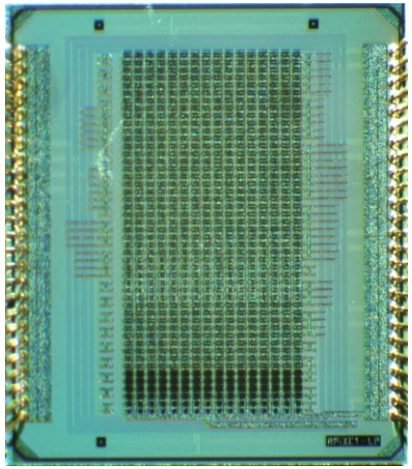
SPAD active area sizes:
- A: 45um
- B: 40um
- C: 35um
- D: 30um

SPAD pairs size combinations (Chip1 - Chip2)

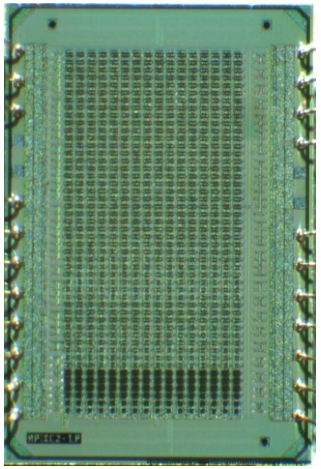
- A - A
- B - B
- C - C
- D - D
- A - B
- A - C
- A - D

Sensor layout

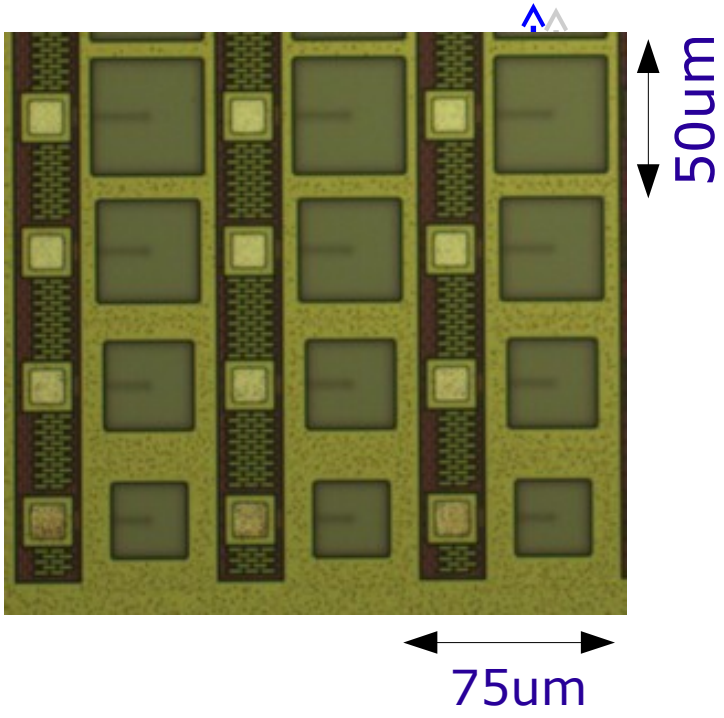
Chip 1



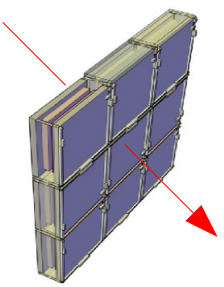
Chip 2



Layout detail: pixels with different SPAD areas



- Array size: 48 x 16 pixels
- Array partitioning:
  - **Two SPAD types**: p+/nwell and p-well/n-iso
  - **Different SPAD active areas**: 30 – 35 – 40 – 45 micron side
  - Some **unshielded structures** for testing with light
  - **Coincidence** between SPAD with **same size** and with **different sizes**



Status of the project APIX2

- APIX2 funded by CNS5 for 3 years → end in 2017

- First submission: end 2014 to LFoundry (150nm)
  SPAD chip ("son") + SPAD and logic chip ("father")
  → received in end April 2015
  → very good single chips performances
  → thinning (20μm !!!) and vertical integration (μ-bump bonding) by IZM
  → received end March → successful !!!
  → extensive characterization of bonded chips → very good bonded chip perf.
  → test beam at CERN sept. 2016 → efficiency with MIPS

- Second submission: May 2015 to XFAB 180nm CMOS HV (40V)
  → good chips performances

we are

---

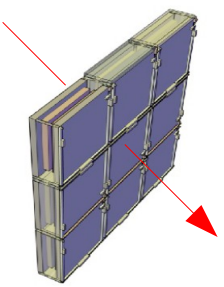
here

- development of a new vertically integrated detector prototype of "large area"
- size 5x5mm^2 with different regions:
- uniform area (3.6x3.6mm^2) → "large" detector prototype
- smaller structures → for testing:
- active vs passive quenching, timing optimized spads, memories and counters

→ design completed → submission JULY 2017

- study of radiation tolerance of the device
(from the standpoint of both ionization and bulk damage)
→ first irradiation tests (neutrons) → JUNE 28-30 2017 @ CN (LNL)

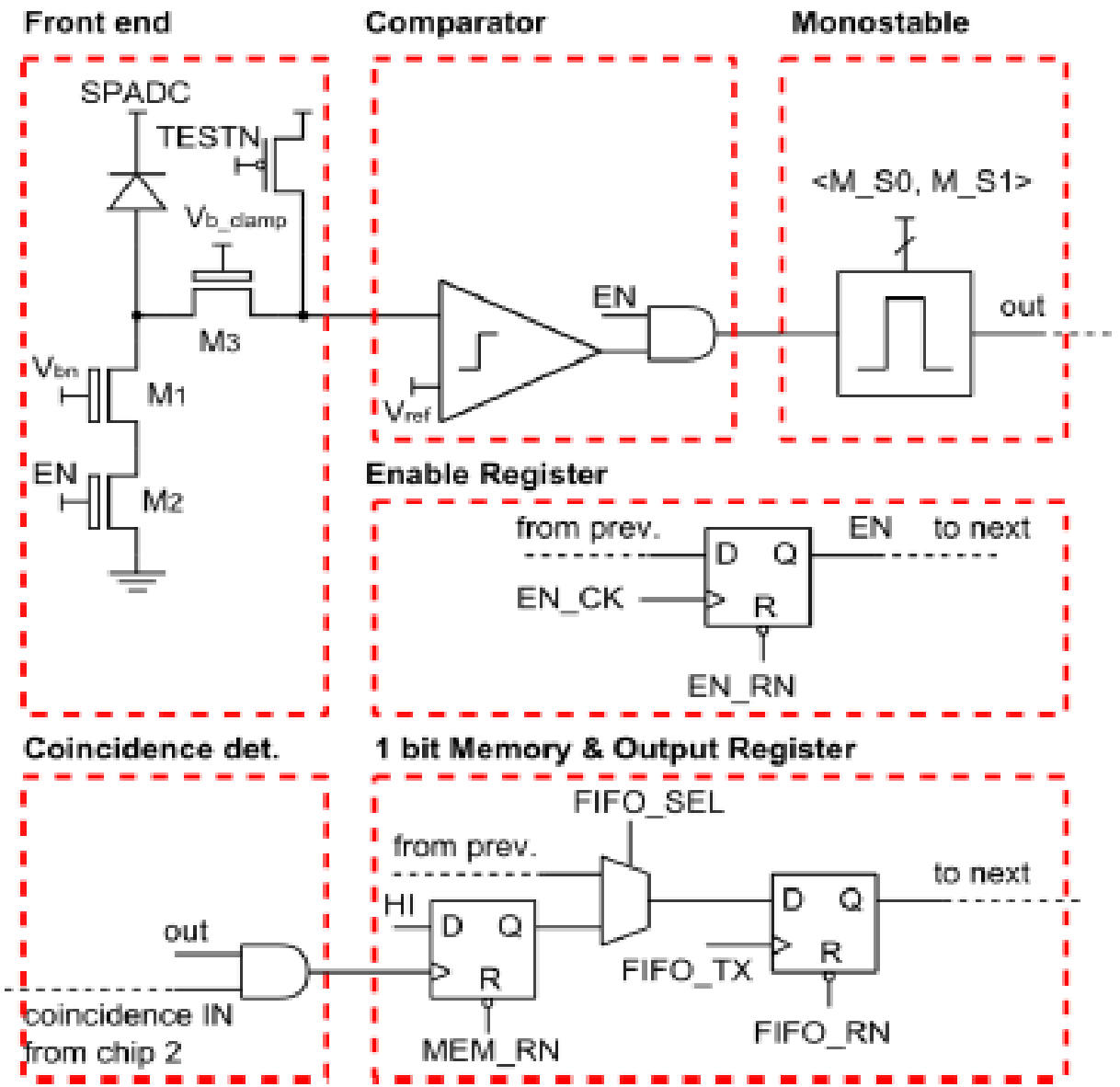
… main milestones reached with success

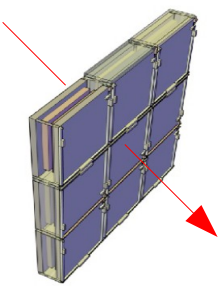


Pixel Electronics

Common to Chip 1 and 2

Only in chip 1





Characterization @ SNRI 2016 – PD/LNL

1. pixels Dark Rate measurement → breakdown voltage
   - Oscilloscope / scalers

2. Cross-talk measurement
   both horizontal (bottom chip) and vertical (Top-Bottom)
   - Coincidence circuits (on-chip/external)

3. Timing resolution
   - pulsed laser (30ps, 375nm)
   - TAC (5ps) / Waveform digitizer (5GSs)

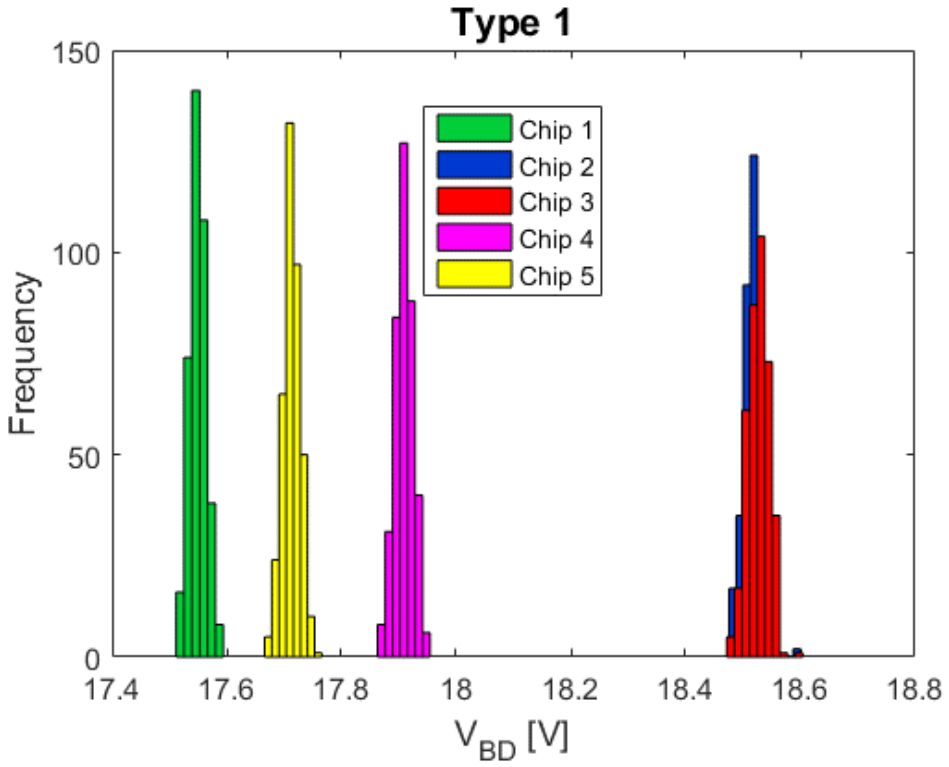
4. Afterpulsing
   - Waveform digitizer / TDC

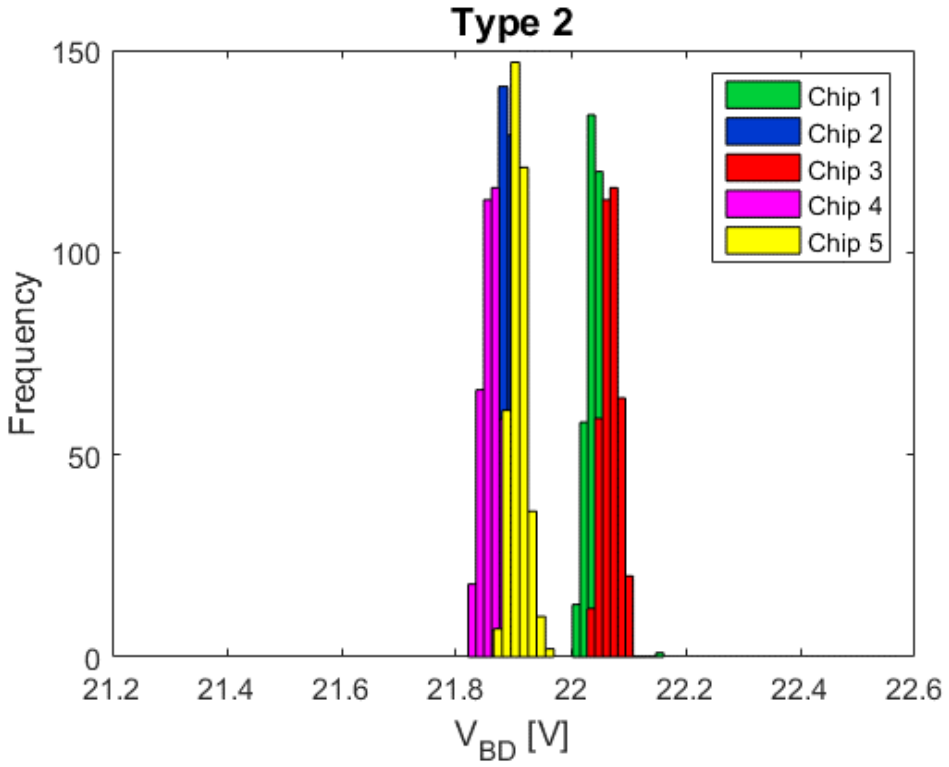
5. absolute Photo-Detection Efficiency (unshielded cells)
   - pulsed laser (30ps, 375nm) / pulsed diodes
   - calibrated photo-diode
   - $1/r^2$ method

   (5'. Optional) relative PDE
   - halogen lamp
   - monochromator

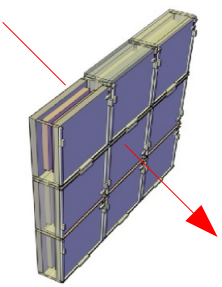
6. Sensitivity to a and β sources
   - scalers

Breakdown voltage uniformity

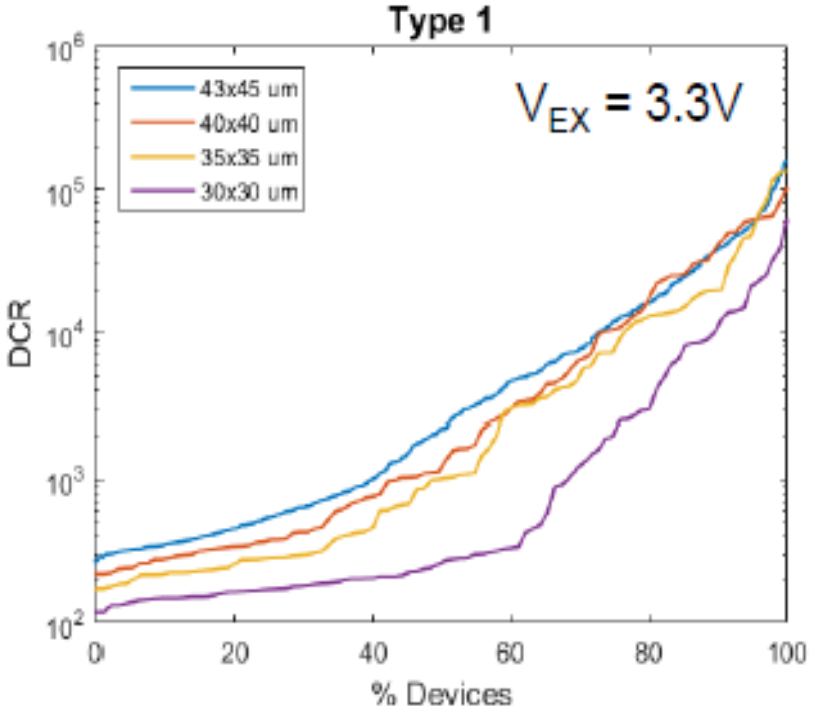


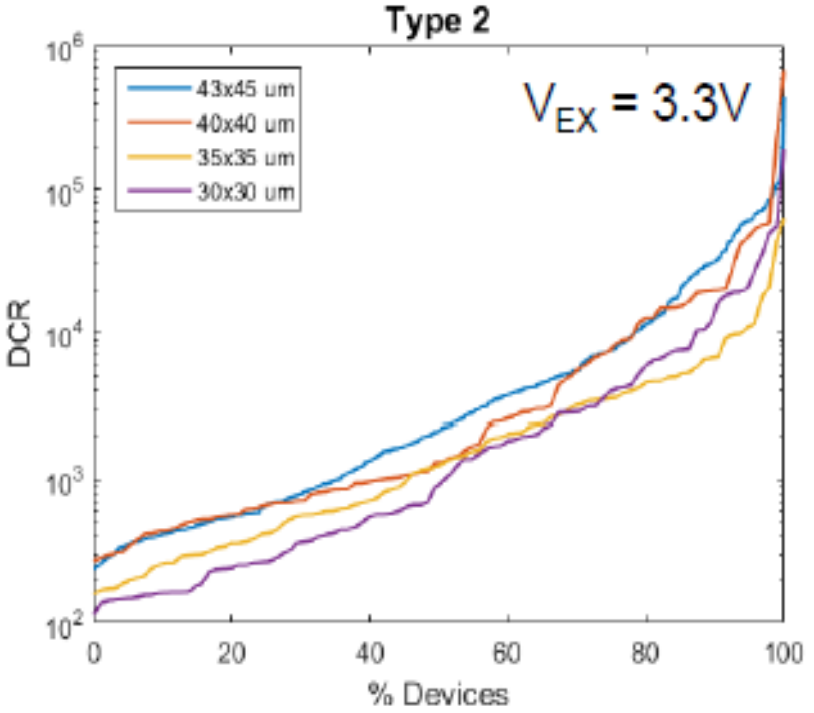


- Measurements on:
  5 sample chips x 2 types x 196 devices per chip
- Very good uniformity on-chip (σ < 20mV)
- Large difference (1V) between different chips for type 1



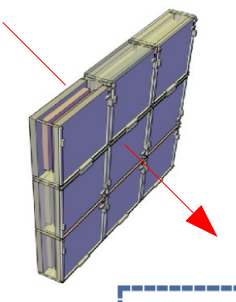
Dark count rate



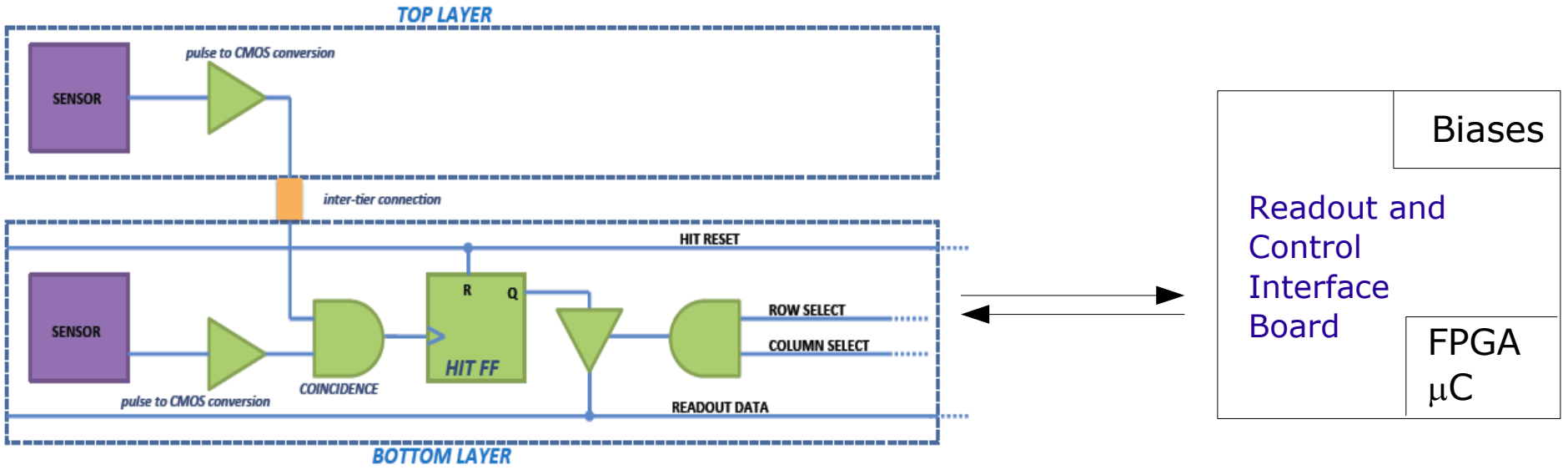


- Cumulative distribution, combined measurements on 3 chips
- 600 devices for largest size, 72 for smaller ones
- Median DCR = 2.2kHz for largest cell size of both types

Dark count rate lower than expected



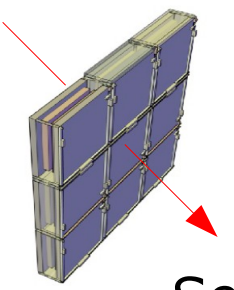
APIX Padova: interface electronics and contribution to all the meas.



APIX-Padova took care of interface electronics used in all the measurements and characterizations

1. chip carrier board (2 versions)
2. basic chip test pcb
3. Interface and Control Board → μ-controller
4. additional interface board → FPGA
5. compact and programmable bias voltage power supplies

Designed and built by
→ **M.Bettini / G.Rampazzo / P.Zatti (servizio elettronica INFN)**



APIX3 project: follow-up of APIX2

Several improvements to be tested exploiting
very good cooperation with LFoundry + first application

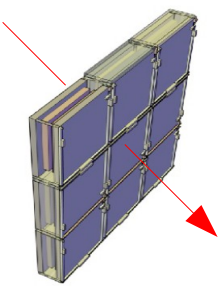
1) improvement in SPAD design (E field engineering)
   → lower DCR
   → active/passive quenching
   → radiation hardness

2) thinning (10μm !) and bonding inside LFoundry
   → lower costs & higher yield

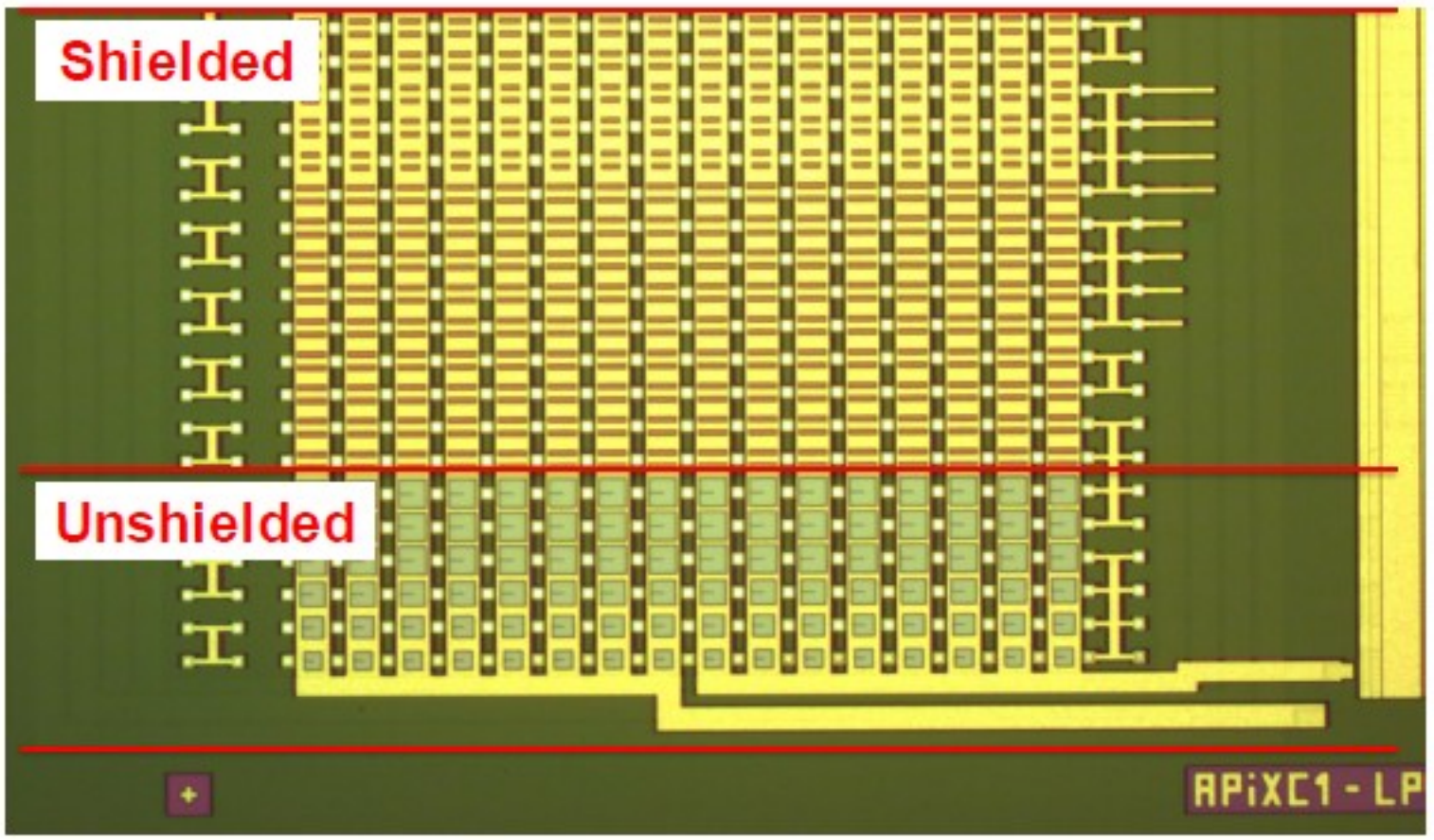
3) Through Silicon Vias
   → peripheral (easy) → sandwich at wafer level !
   → local (might be w/ thinning 10μm) → multi-layers !!!

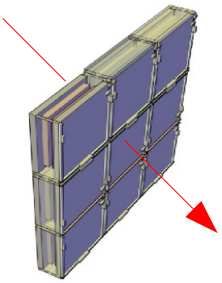
4) Electronics from 150nm to 110nm → higher fill factor

5) Response studies and Radiation Hardness with micro-beams
6) First application → beta probe for radio-guided surgery

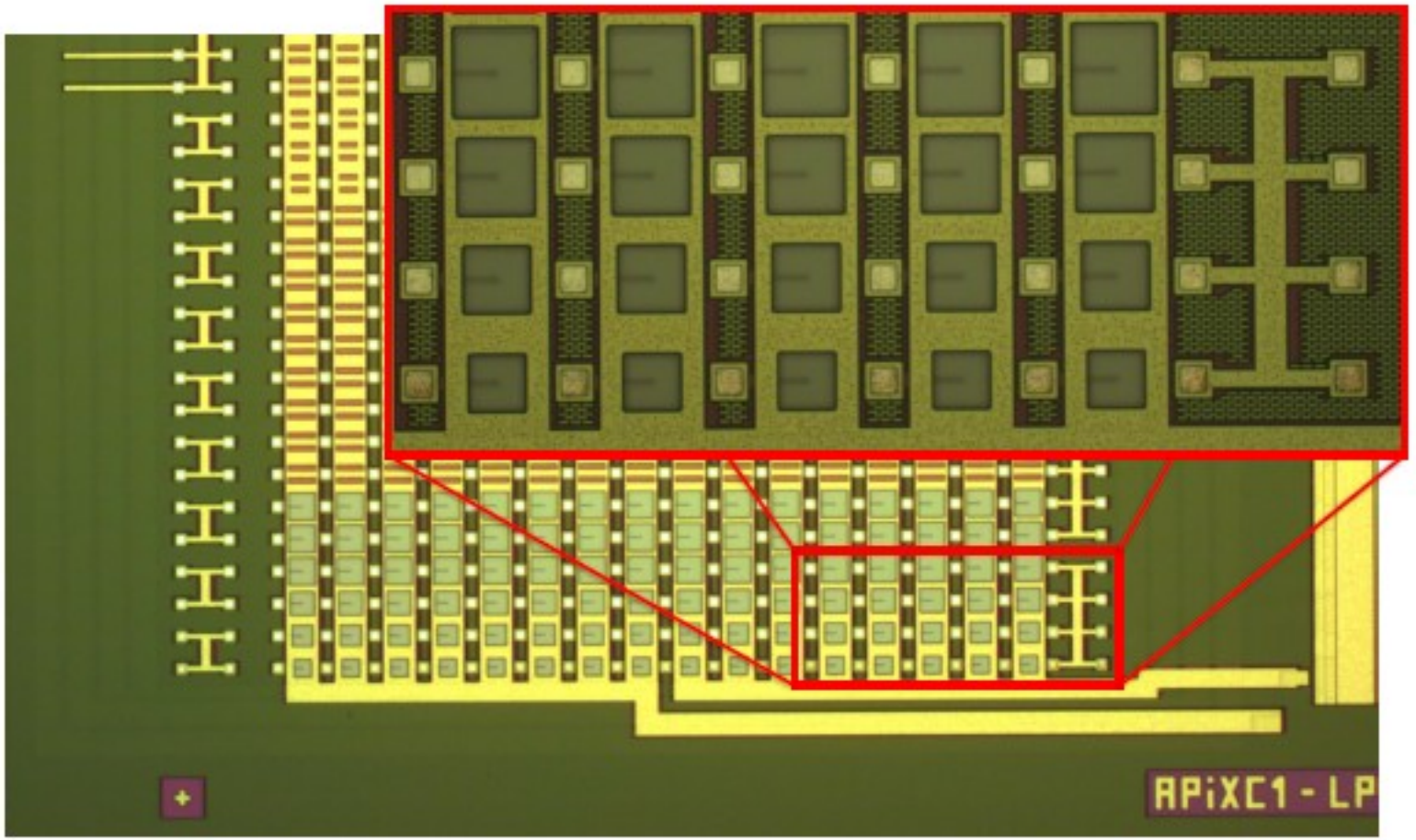


Bottom chip - Micrographs

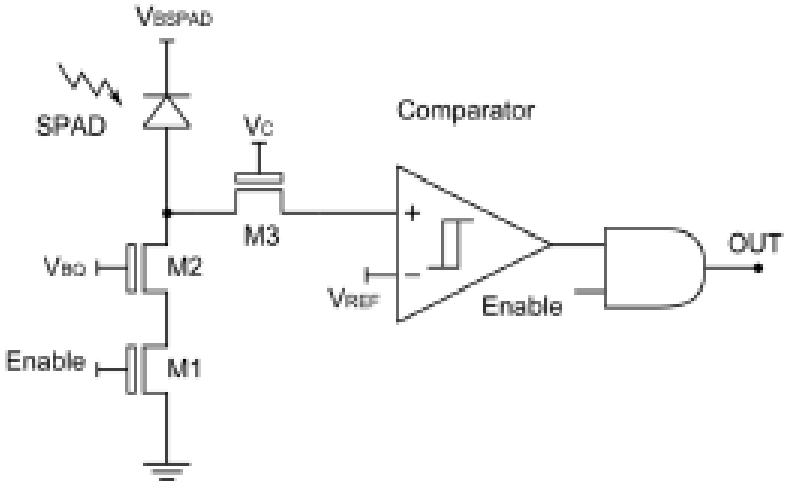




Bottom chip - Micrographs



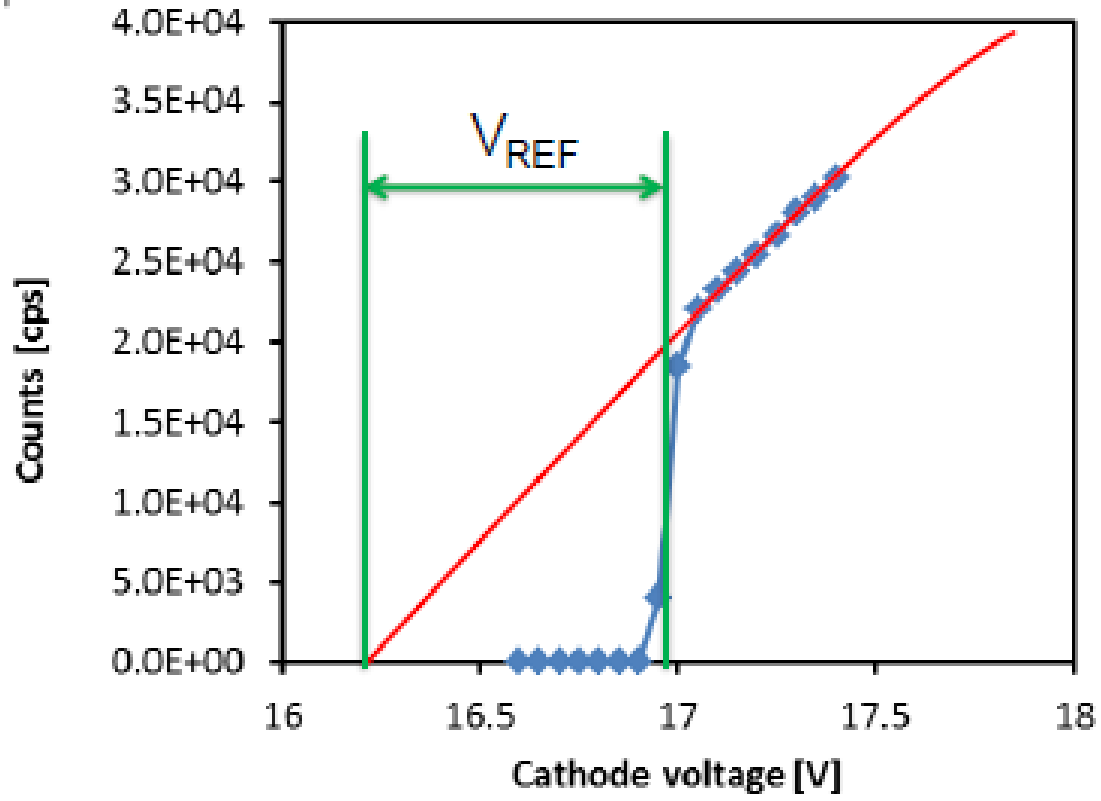
Reference – Vbd extraction method



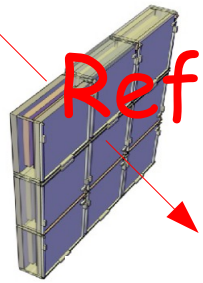
L. Pancheri et al., Proc. IEEE ICMTS, 2014

V_{BD} extraction from I-V curves: not possible

V_{BD} extracted from the dark count rate vs. voltage curve

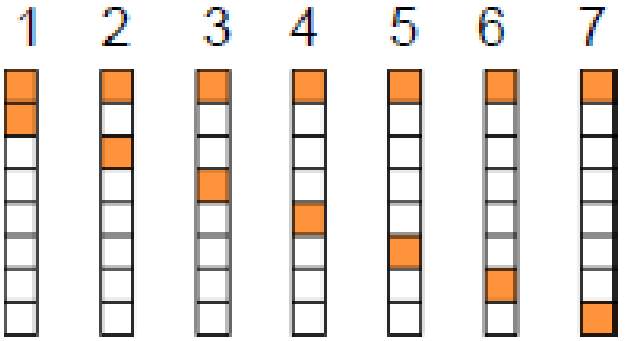


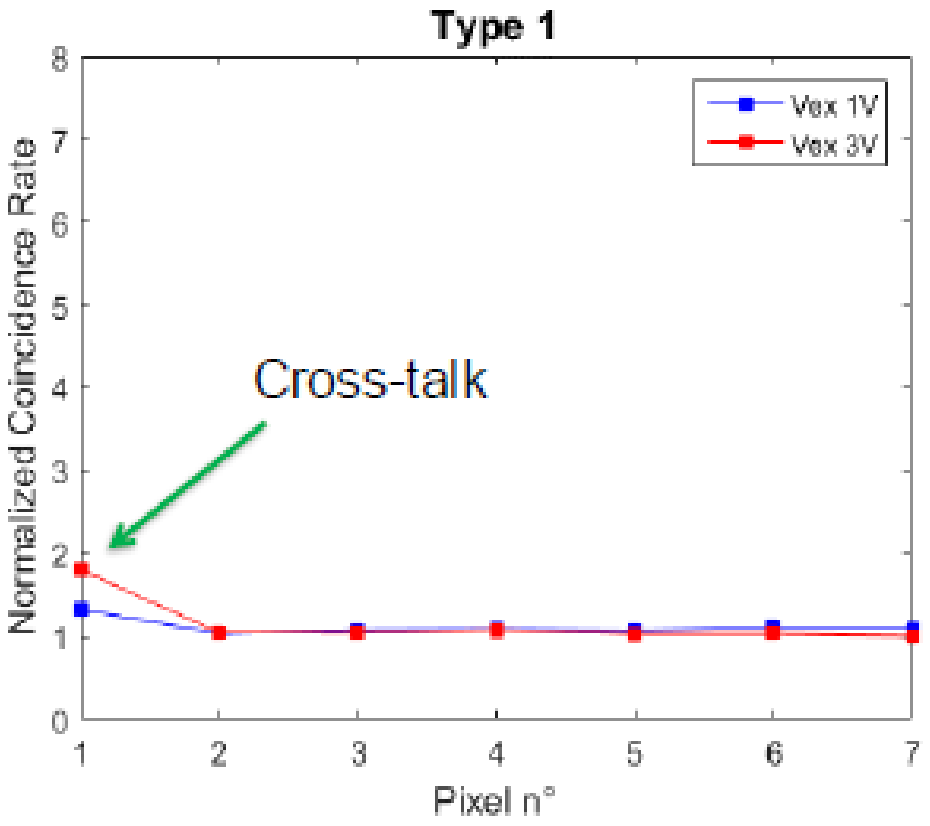
Reference – Horizontal cross-talk

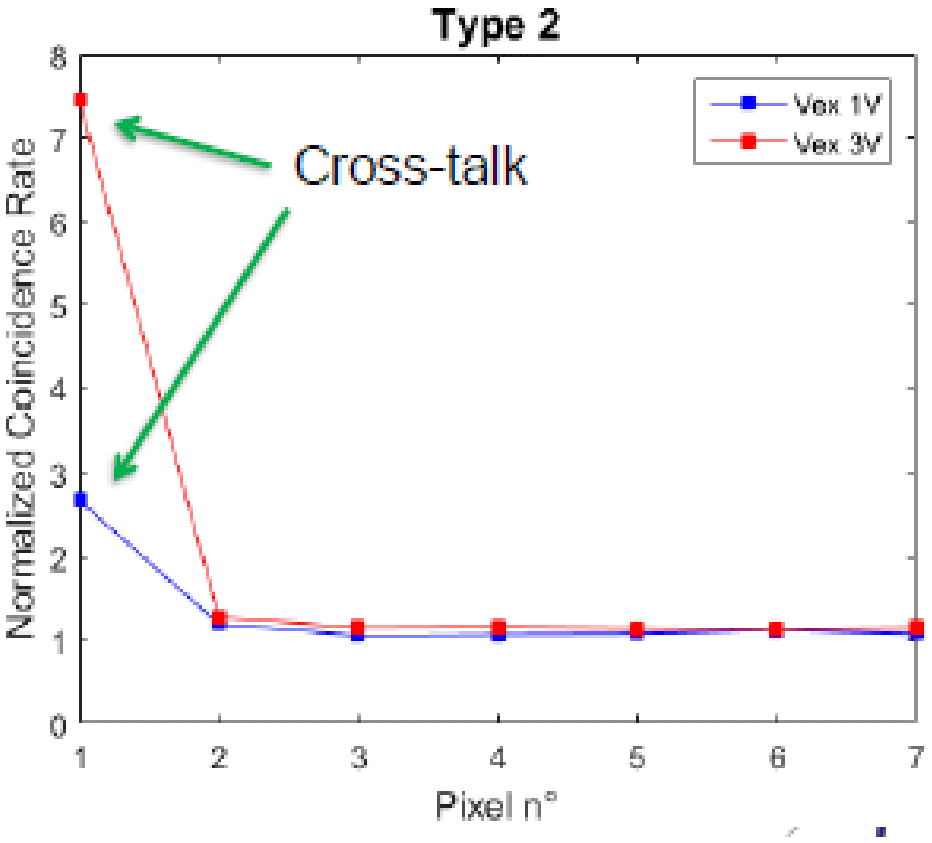


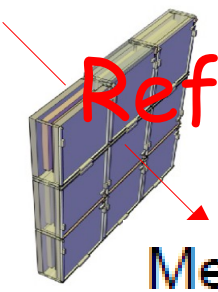
Count rate in coincidence between two pixels in the same column

Normalized rate: $$\frac{CR_{Meas}}{2 \cdot CR_1 \cdot CR_2 \cdot \Delta T}$$





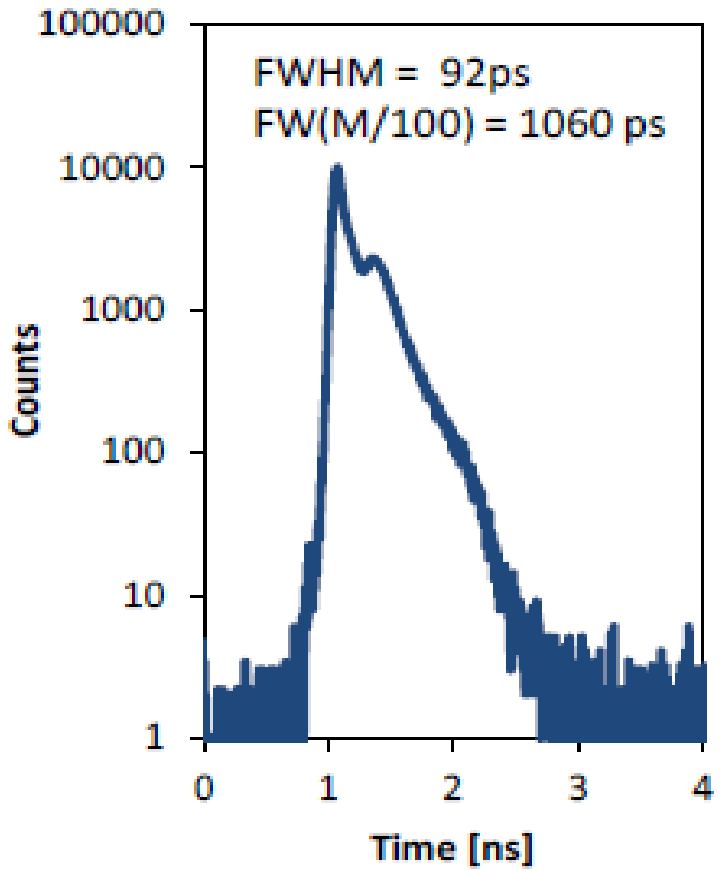




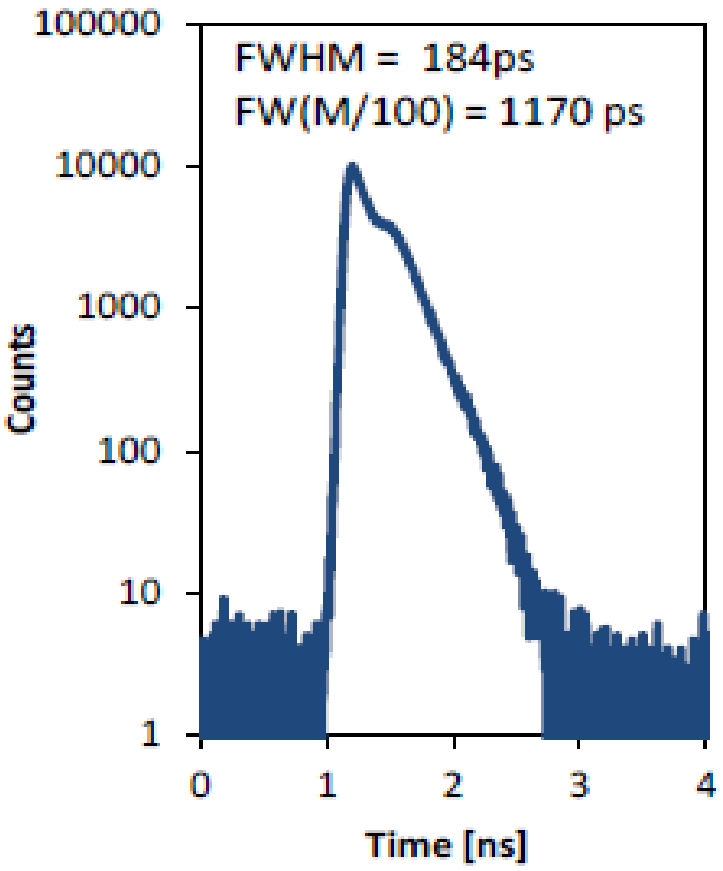
Reference - SPAD timing

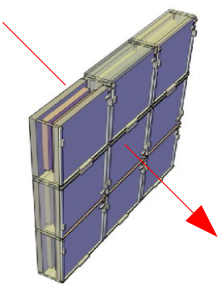
Measured on 10-µm devices, with blue laser (470nm), 70ps FWHM

Type 1: **60ps FWHM**

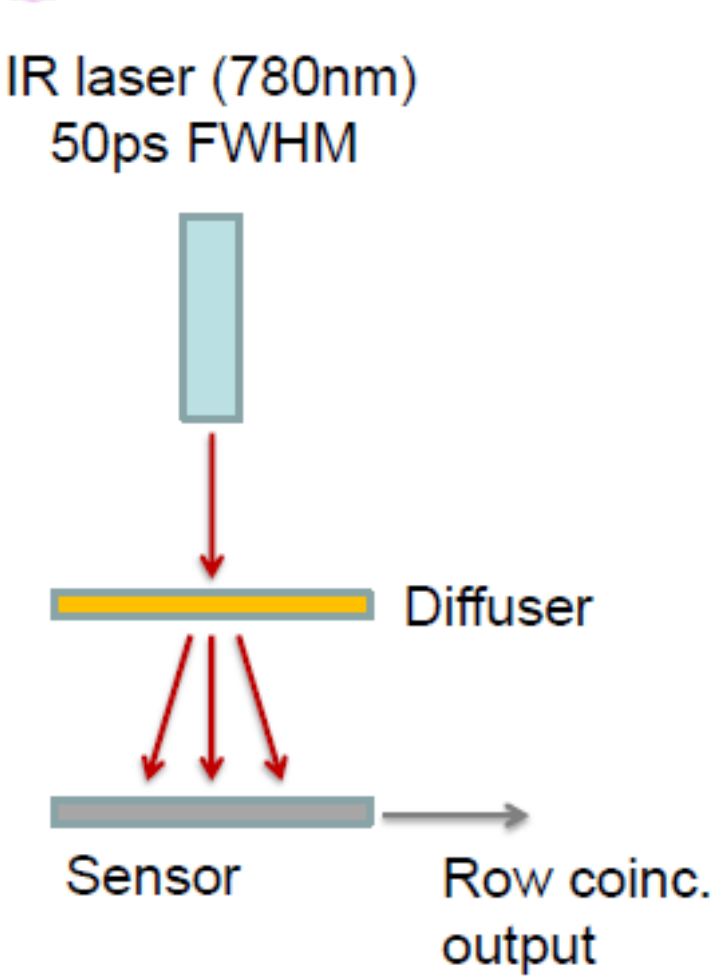


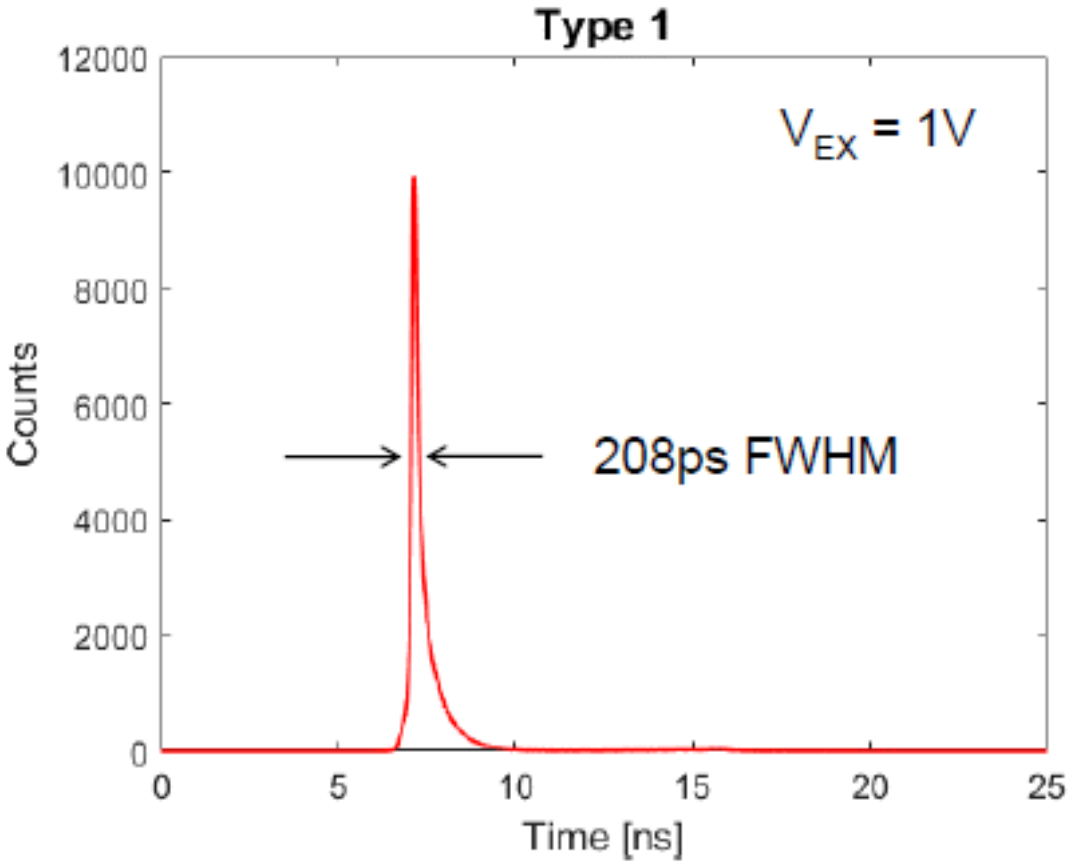
Type 2: **170ps FWHM**





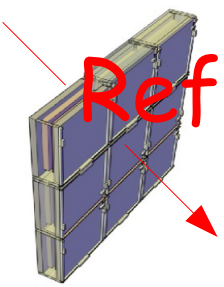
Chip characterization





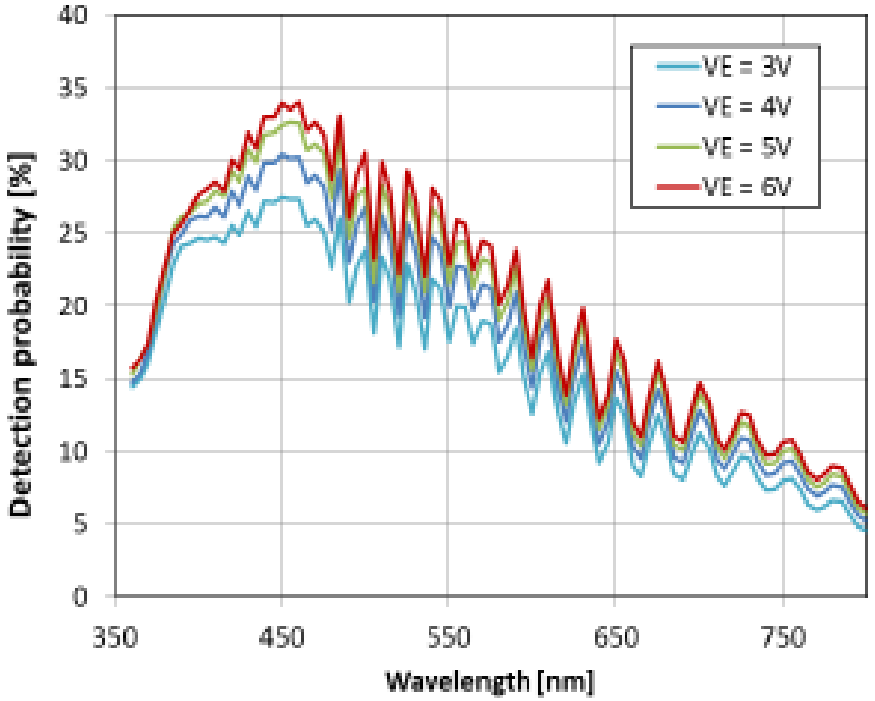
Timing histogram between laser trigger and sensor coincidence output

N.B. Design not optimized for timing

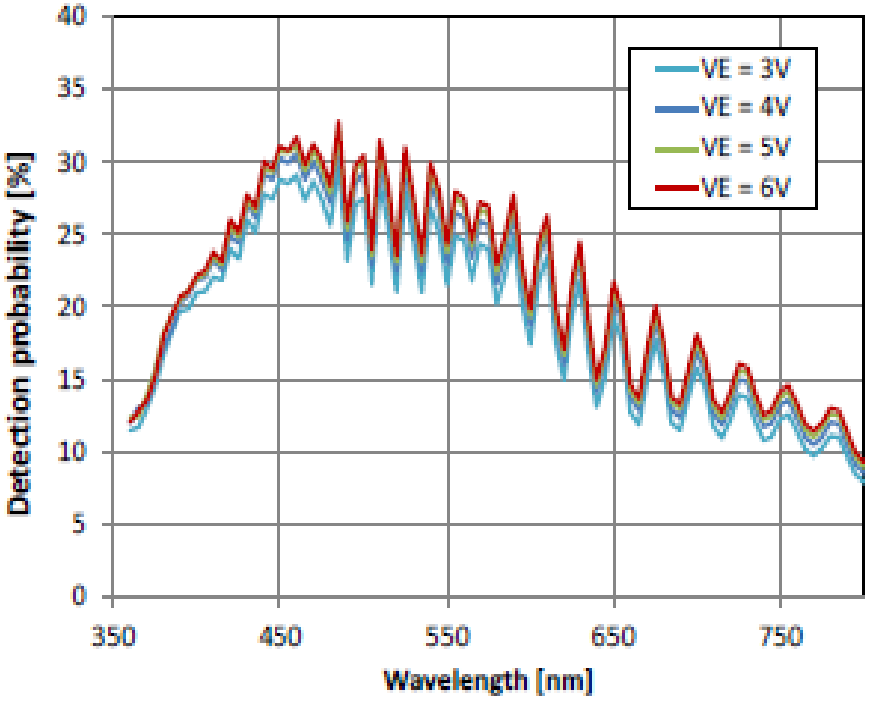


Reference – SPAD PDE

Type 1: p+/nwell



Type 2: pwell/niso



Shallower junction:
better NUV – Blue efficiency

Wider depletion region:
Better red-IR efficiency

L. Pancheri et al., J. Selected Topics in Quantum Electron, 2015