LHCb RICH electronics development in Kraków

Piotr Dorosz on behalf of RICH group in Kraków

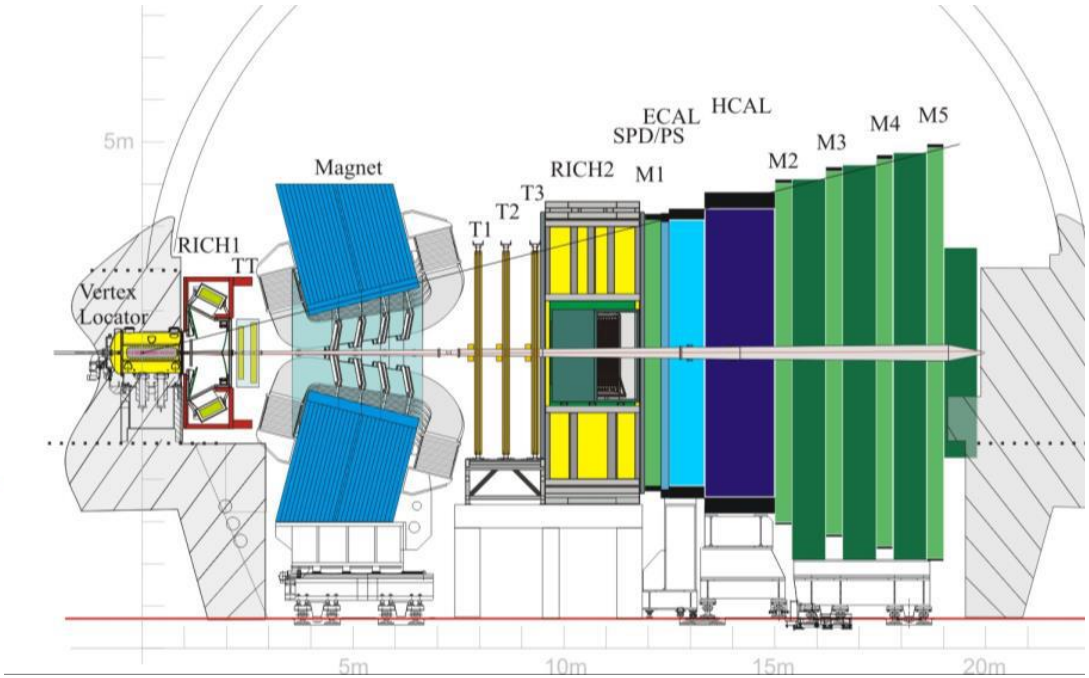
The RICH subdetectors provide k-π separation in the range 2-100 GeV/c.

RICH1:

- Upstream of the magnet
- Angular acceptance 25-300 mrad
- Aerogel range 2-10 GeV/c
- C_4F_{10} range 10-40 GeV/c

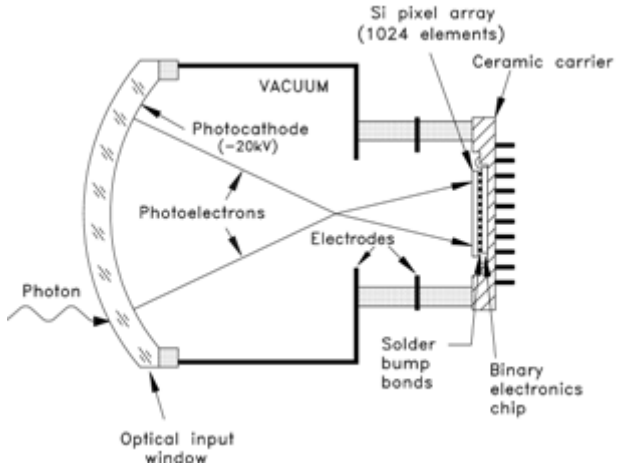
RICH2:

- Downstream of the magnet
- Angular acceptance 15-120 mrad
- CF_4 range 15-100 GeV/c

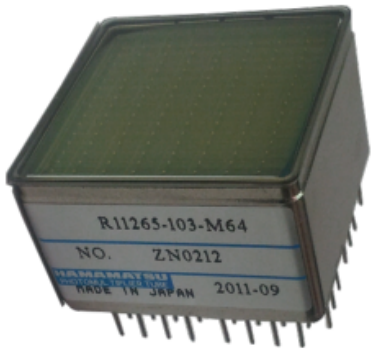


Currently readout by hybrid photon detectors (HPD)

- Embedded readout chip
- Max trigger rate 1 MHz



Multi-anode photomultiplier tube (MaPMT)



R11265
8x8 pixels

Geometrical dimensions	26.2×26.2 mm^2
Window material / thickness	UV glass / 0.8 mm
Photocathode minimum effective area	23×23 mm^2 ($> 80\%$)
Photocathode material	Super Bialkali
Spectral response range	$185 - 650$ nm
Number of pixels / dimensions	64 / 2.9×2.9 mm^2
Number of dynodes	12
Maximum supply voltage	-1.1 kV
Typical gain at -1 kV	$> 1 \times 10^6$
Uniformity between pixels	$1 \div 3$
Dark current (average per pixel)	0.4 nA
Rise / transit time	0.6 ns / 5.1 ns

H12700
8x8 larger pixels
Allows to reduce costs in the peripheral regions

R11265 → 2688 RICH−1 + 1120 RICH−2 = 3808
H12700 → 448 (RICH−2)

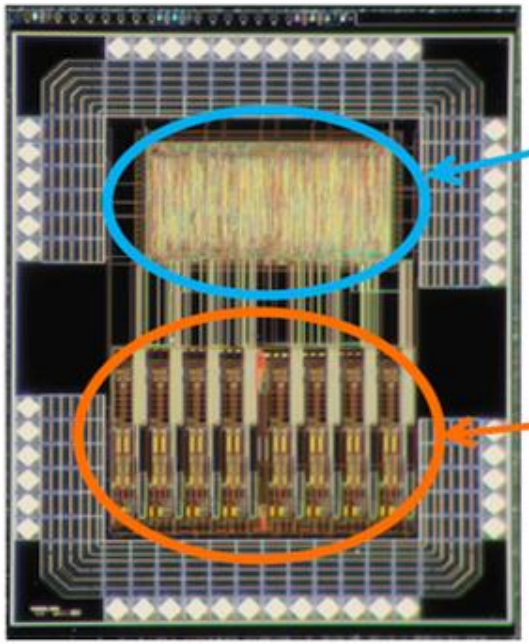
CLARO8 chip

Requirements for the front-end electronics for Ma-PMTs:

- **Dead time < 25 ns**
- **Low power ≈ 1 mW/channel**
- **Radiation tolerance: up to 10 KGy (1 Mrad), hadrons up to 10^{13} cm^{-2}**

The CLARO was designed by Milano Bicocca, Ferrara and Krakow to satisfy these requirements.

Since the end of 2013 the CLARO8 is the baseline choice for the RICH upgrade.

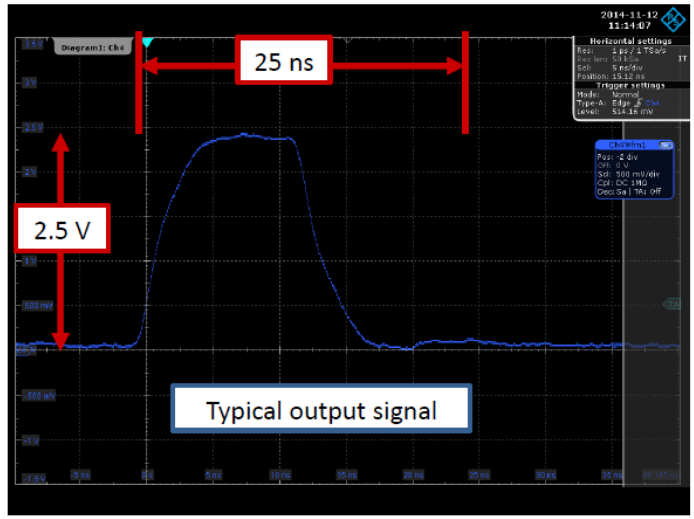


Digital configuration register (Ferrara/Krakow):

- 128 configuration bits protected with TMR
- SEU counting
- ...

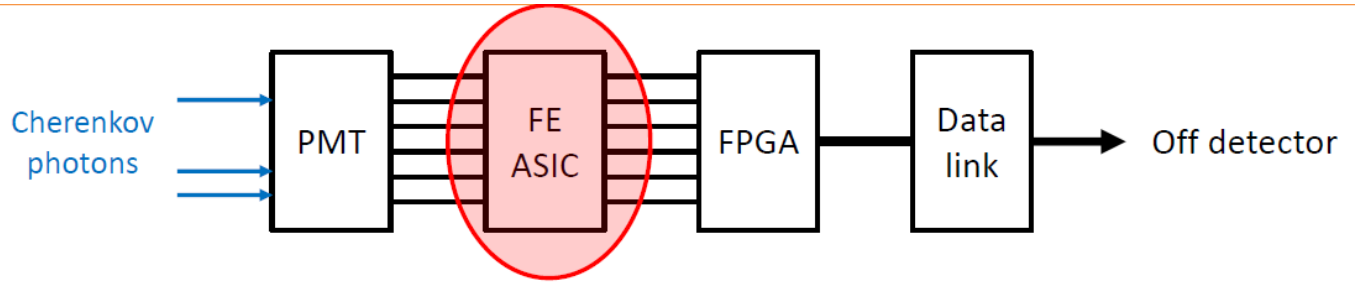
8 readout channels (Milano Bicocca):

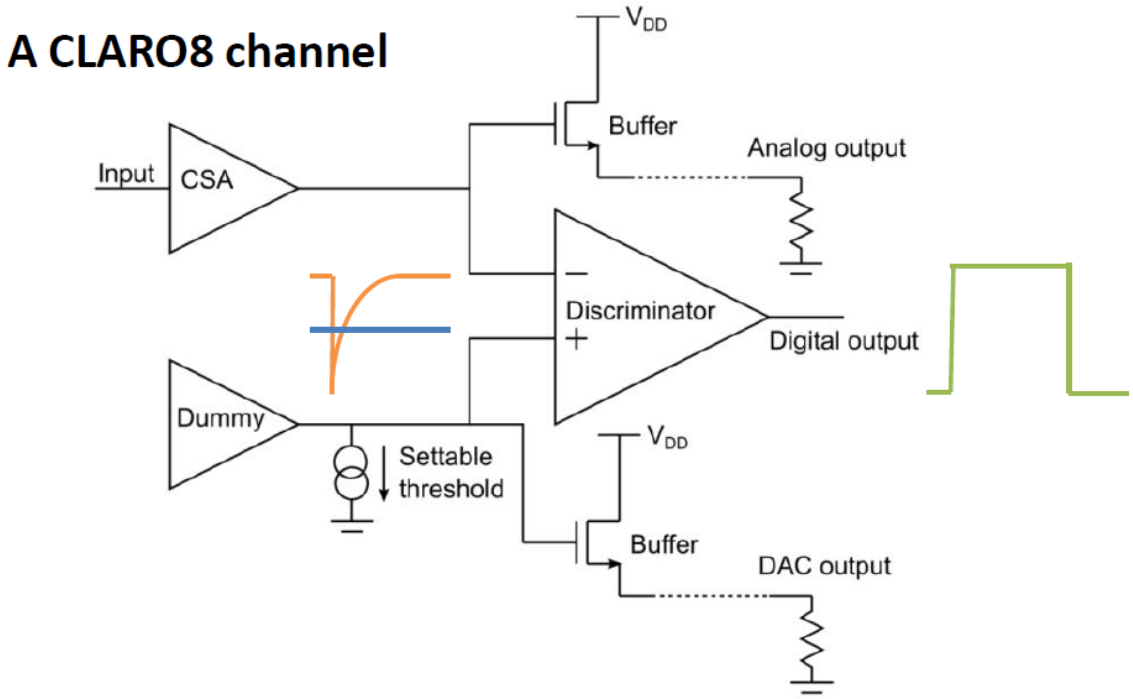
- Amplifier with low input impedance
- Discriminator with settable threshold
- Test pulse injection circuit
- ...



Claudio Gotti – The CLARO chip

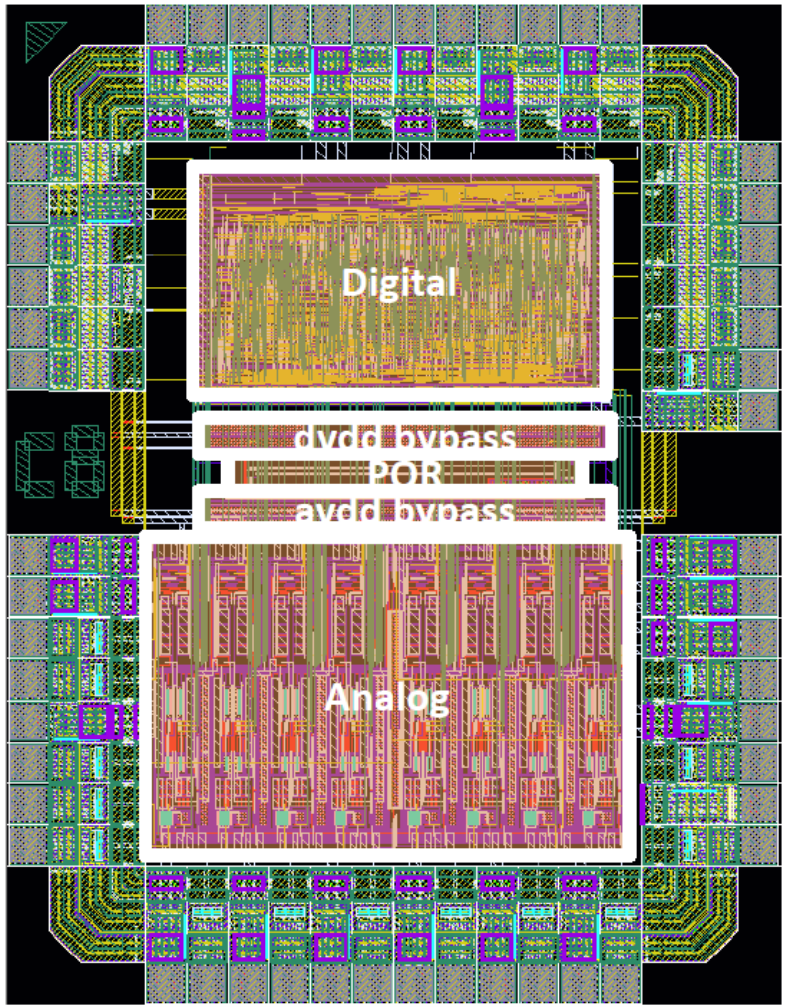
A single channel of the CLARO8 chip





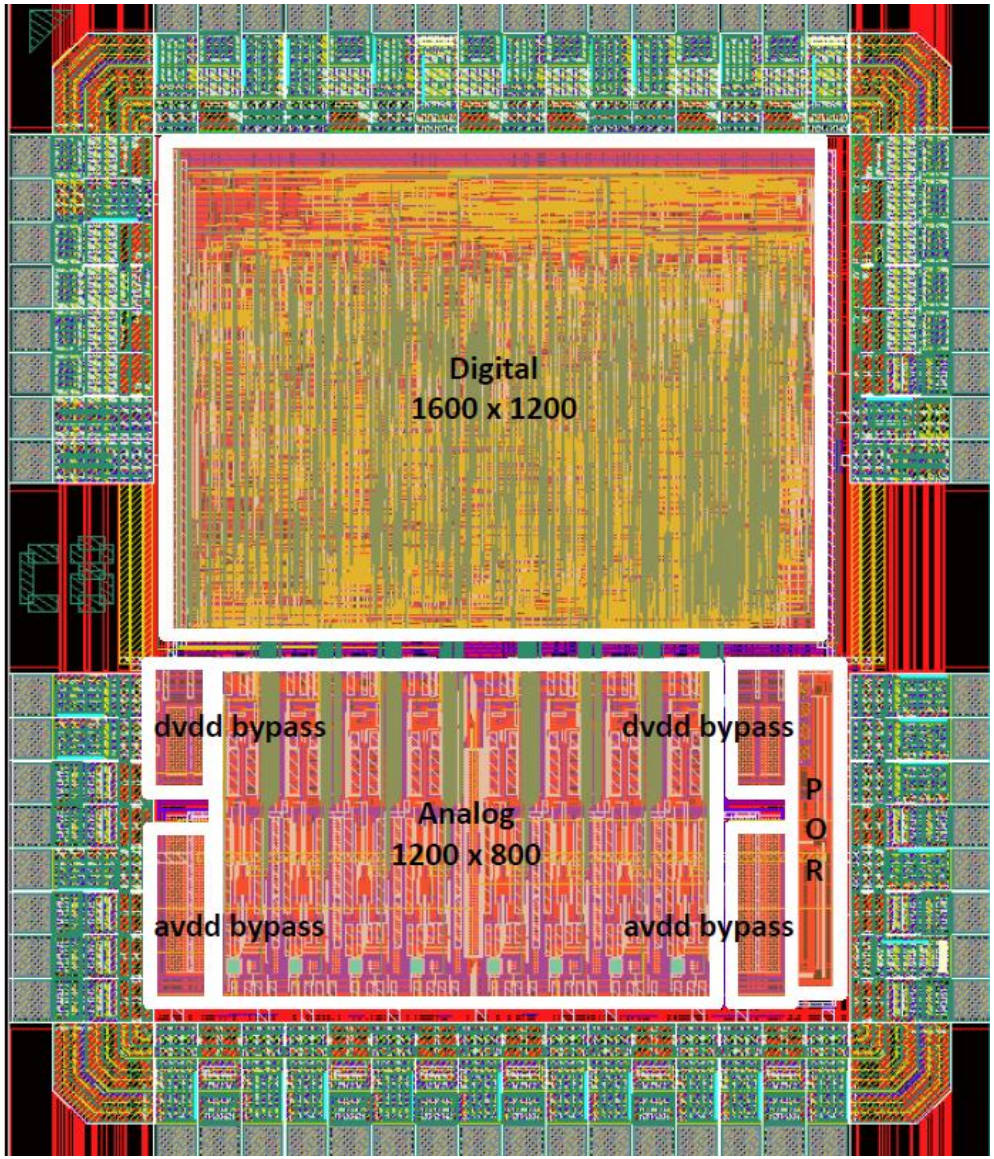
CLARO8v2 (2015):

- Total area: 5 mm^2 (2000 x 2500 um^2)
- Analog block: 1200 x 800 um^2
- POR block: 900 x 100 um^2
- Digital block: 1050 x 600 um^2
- Free space near the POR block filled with bypass capacitors (3x 13 pF on both avdd and dvdd)

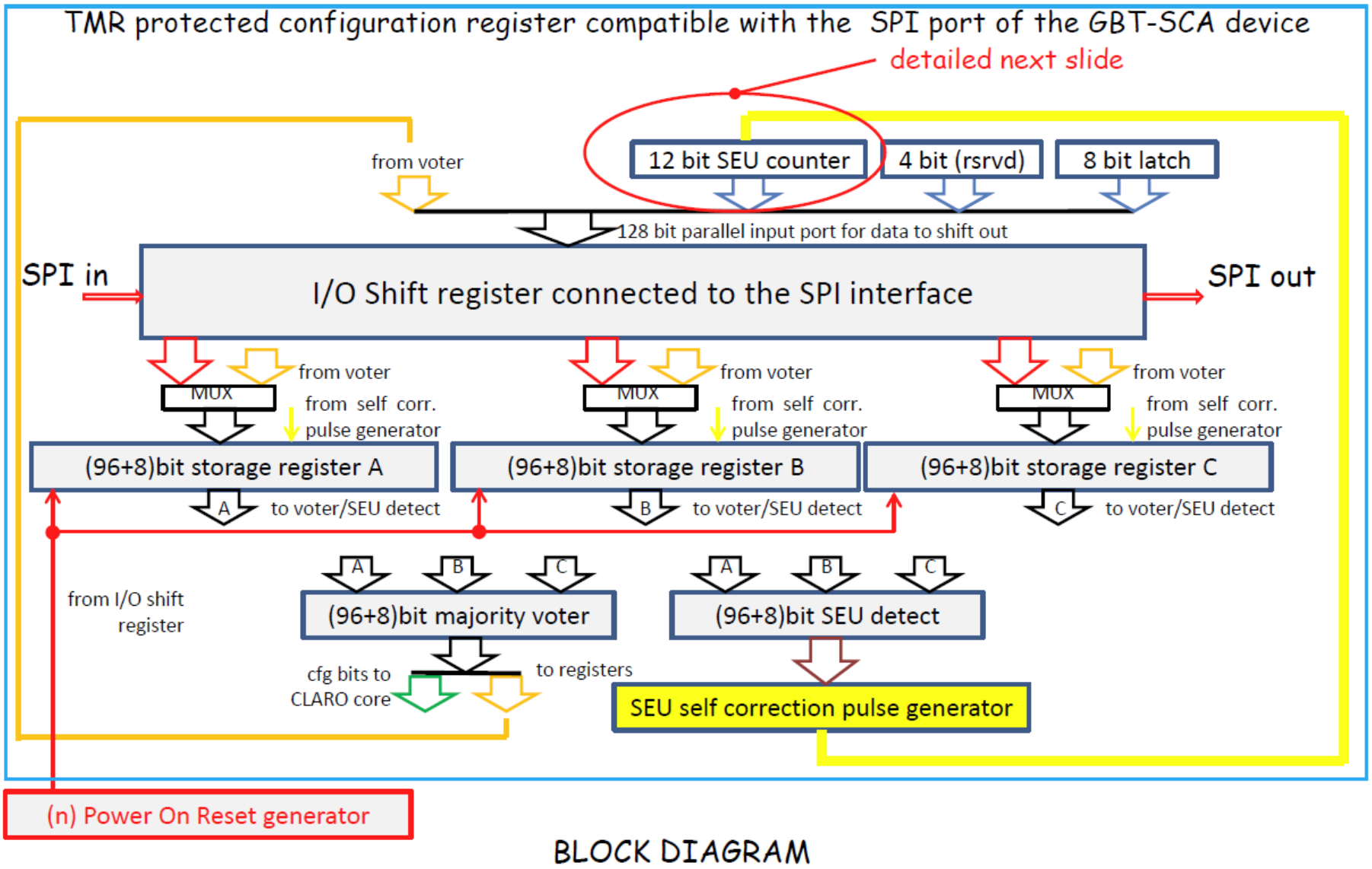


CLARO8v3 (2016):

- Total area: 6.6 mm^2 (2350 x 2800 um^2) (30% larger than CLARO8v2)
- Analog block: 1200 x 800 um^2
- POR block: 800 x 100 um^2
- Digital block: 1600 x 1200 um^2 (3x larger than CLARO8v2)
- Free space near the analog block filled with bypass capacitors (2x 40 pF on avdd, 2x 17 pF on dvdd)
- agnd pads added for direct downbond to QFN thermal pad

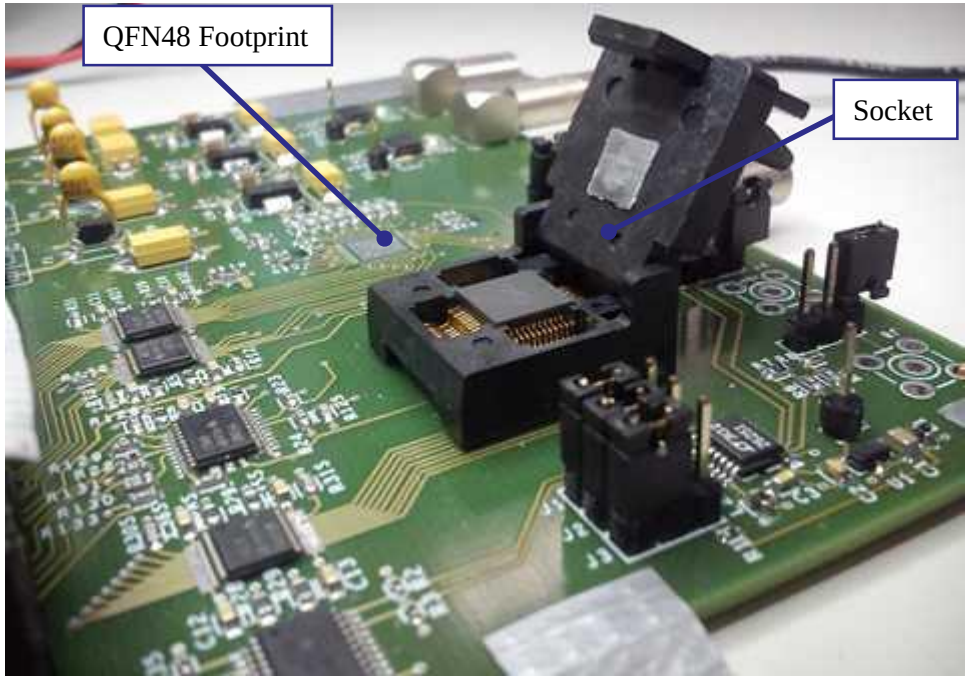


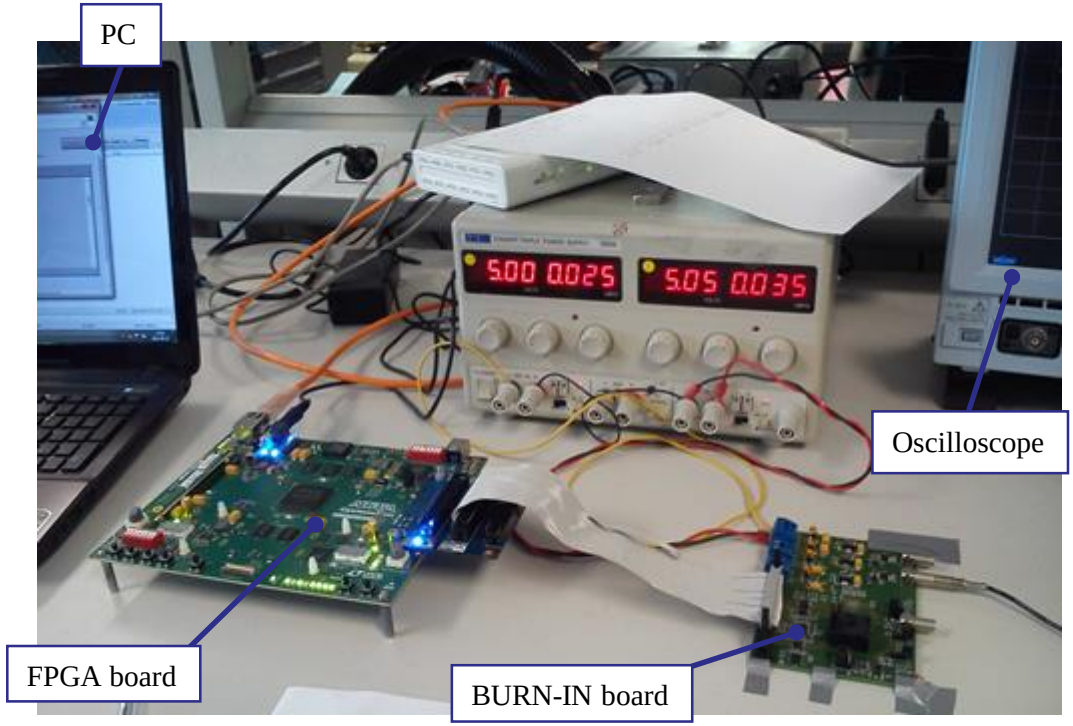
Overview: CLARO8v3 digital core details



BLOCK DIAGRAM

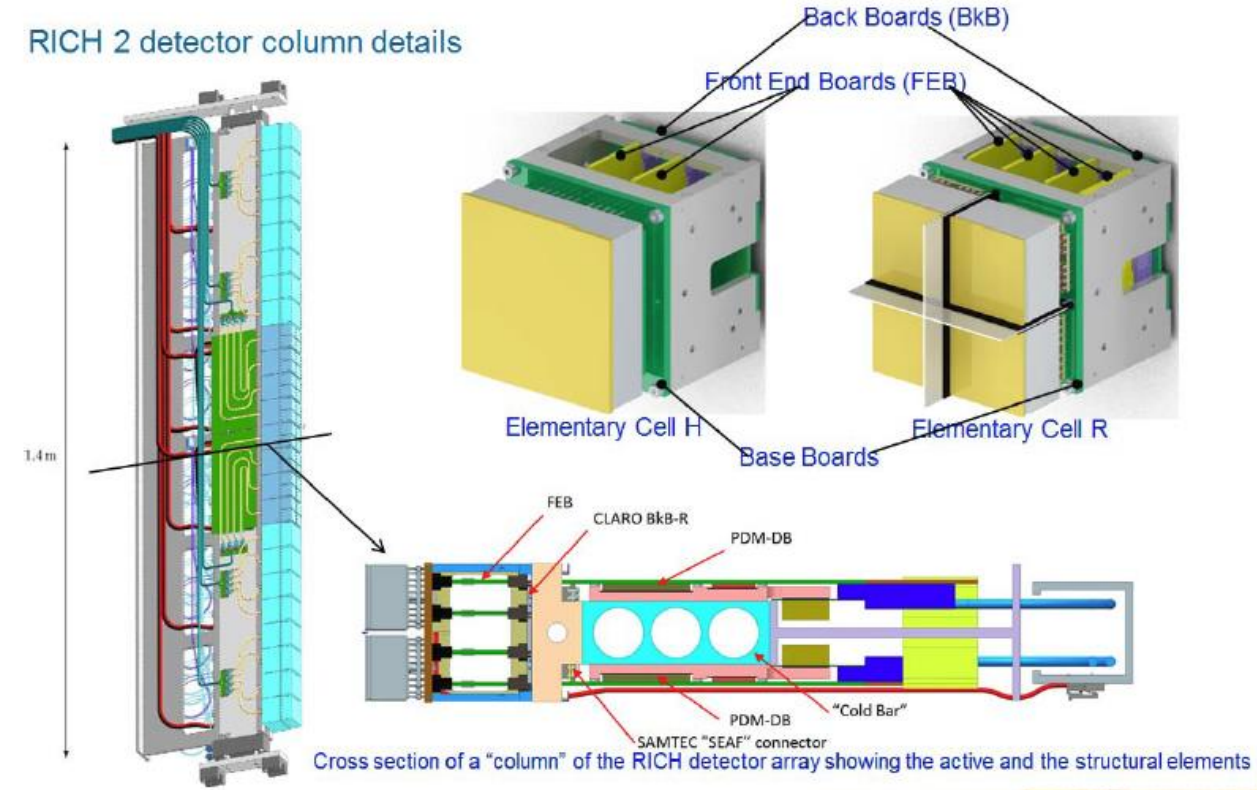
CLARO8 tests in Kraków and Ferrara

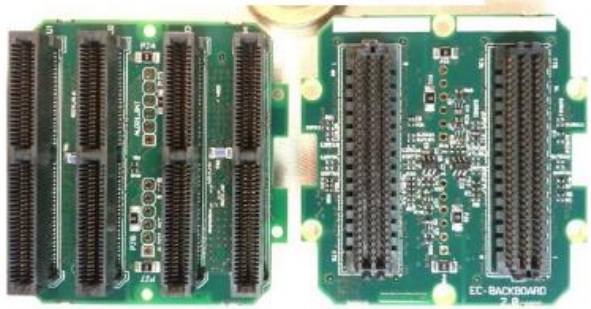


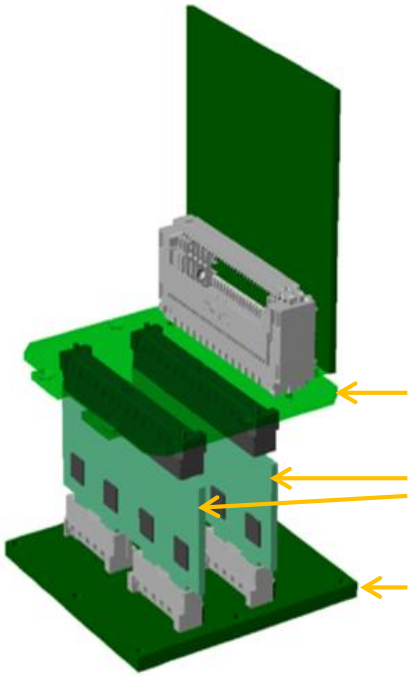


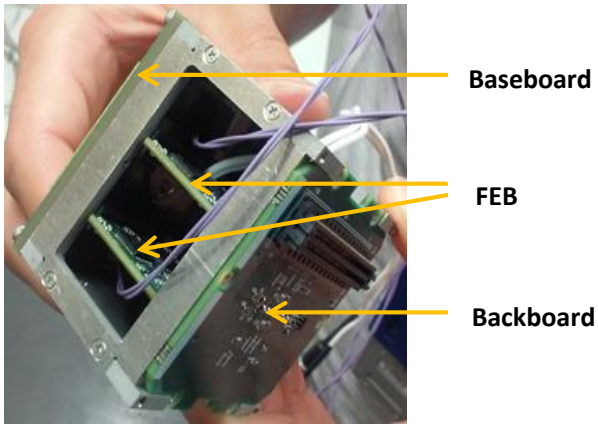
Piotr Dorosz, Mateusz Baszczyk

Elementary cells (EC): EC-R and EC-H

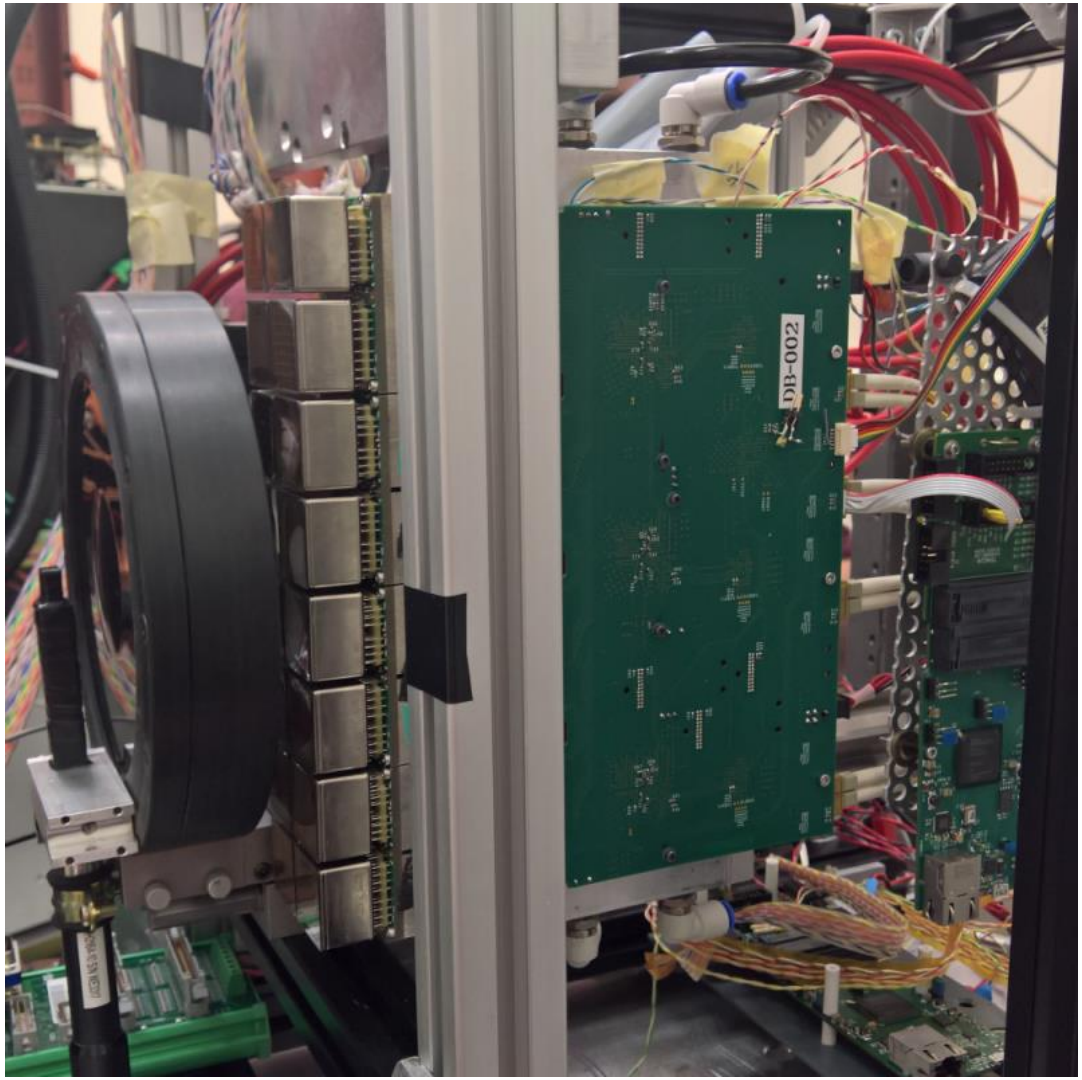




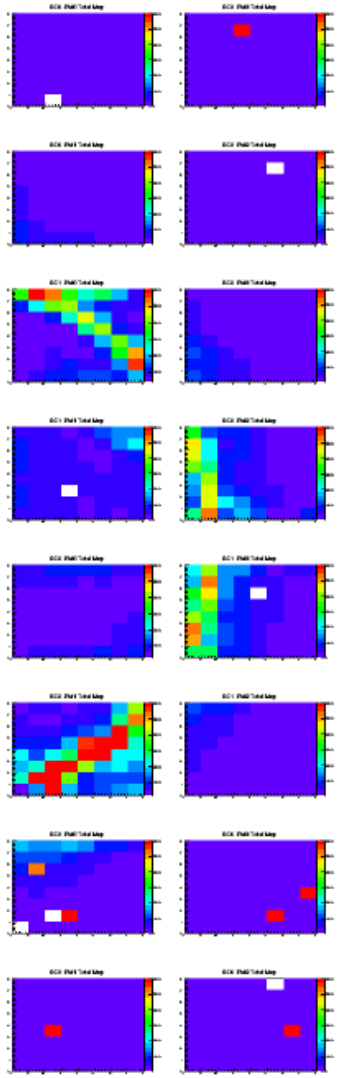




Piotr Dorosz – RICH EC-H



Roberta Cardinale – Test beam status



CLARO8 production and schedule

Name	Begin date	End date
CLARO8v3 final production	06/12/16	31/07/18
MPW for 400 CLARO8v3 for EC production startup and 2017 beam testing	06/12/16	03/04/17
CLARO8v3 dice production at AMS	06/12/16	20/02/17
packaging at ASE; delivery at MiB	21/02/17	03/04/17
Engineering run for 9 wafers (3 guaranteed, should yield min. 11.000 dice)	16/02/17	03/10/17
Effective Date of Contract to Manufacturer	16/02/17	16/02/17
CLARO8v3 dice production at AMS	16/02/17	10/07/17
packaging at ASE; delivery at CERN	11/07/17	03/10/17
Production run for 25 wafers	04/10/17	31/07/18
Validation of engineering run	04/10/17	15/11/17
CLARO8v3 dice production at AMS (after validation of engineering run)	16/11/17	27/03/18
packaging at ASE; delivery at CERN	28/03/18	31/07/18
PRODUCTION OF THE CLARO8 ASIC AUTOMATED TEST BENCH	01/02/16	04/05/17
PRODUCTION OF A SECOND UNIT OF CLARO8 ASIC AUTOMATED TEST BENCH	01/02/17	20/10/17
PROTOTYPE OF AUTOMATED TESTER FOR THE FEB+BACKBOARD (and EC)	07/03/16	11/05/17
PRODUCTION OF AUTOMATED TESTER FOR THE FEB+BACKBOARD (and EC) (6 units at least)	05/05/17	28/07/17
PROCUREMENT of FEB, Backboard-R, Backboard-H	16/02/17	26/03/19
Effective Date of Contract to Manufacturer	16/02/17	29/03/17
pre-production: manufacturer launches PCB production/component procurement	04/04/17	04/04/17
Test of ASICs (INFN-FE) for pre-production	04/04/17	24/04/17
pre-production of FEBs (30), BkB-R(5), BkB-H(5) (tests performed at INFN-Fe to qualify QC system)	26/04/17	25/05/17
MILESTONE: availability of FEBs for QC system commissioning / beam testing	26/05/17	26/05/17
pre-production: manufacturer develops BackBoard connectivity test system (for production lots)	04/04/17	29/06/17
Test of ASICs (4240) for Lot 1	04/10/17	02/11/17
Lot 1 (including test at factory)	03/11/17	31/01/18
Test of ASICs (4800) for Lot 2	03/11/17	15/12/17
Lot 2 (including test at factory)	01/02/18	26/04/18
Test of ASICs (8000) for Lot 3 - IF 6/9 WAFER GOOD FROM ENG. RUN	18/12/17	19/02/18
Lot 3 (including test at factory)	27/04/18	20/07/18
Test of ASICs (8000) for Lot 4 - ASSUME TO WAIT FOR ASIC FROM FULL PRODUCTION	01/08/18	03/10/18
Lot 4 (including test at factory)	04/10/18	31/12/18
Test of ASICs (8000) for Lot 5 - NEED TO WAIT FOR ASIC FROM FULL PRODUCTION	04/10/18	15/11/18
Lot 5 (including test at factory)	02/01/19	26/03/19
TEST of EC (no Mag.Shielding)	01/03/17	16/05/19

The FEB/BackBoard team:
M. Baszczyk, P. Dorosz, W. Kucewicz – AGH-UST Krakow
M. Fiorini, R. Malaguti, A. Cotta Ramusino – INFN Ferrara
P. Carniti, L. Cassina, C. Gotti, G. Pessina – INFN Milano Bicocca