Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

ARCADIA

Programma di attività e preventivo di spesa

Sezione di Pavia

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Resp. Loc.: Gianluca Traversi

INFN Pavia, CDS, 10 luglio 2018

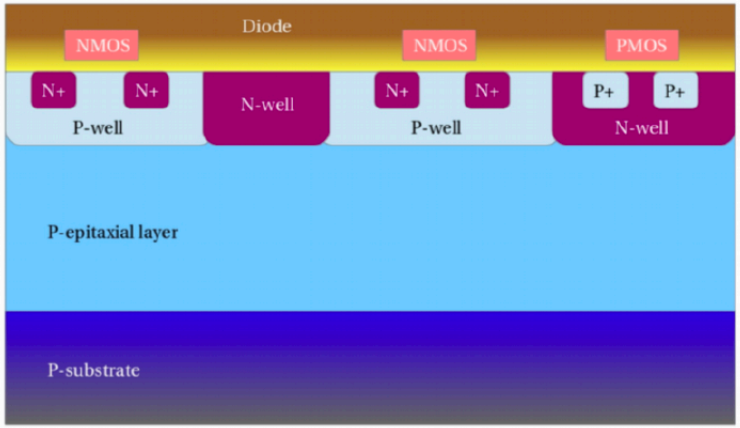
ARCADIA

- Goal of the project: develop a novel platform based on a fully depleted CMOS sensor (monolithic structure, low capacitance, fast charge collection) with possible applications in a range of fields, including charged particle tracking in HEP, medical and space applications and X-ray imaging

- Duration: 3 years

- Participating INFN groups:
  - INFN Bologna
  - INFN Milano
  - INFN Padova
  - INFN Pavia
  - INFN Perugia
  - INFN Torino
  - TIFPA Trento

Monolithic sensors



Monolithic technology

- Sensor and readout electronics are built in the same silicon wafer
- Low material budget
- Low cost because only one fabrication process is needed

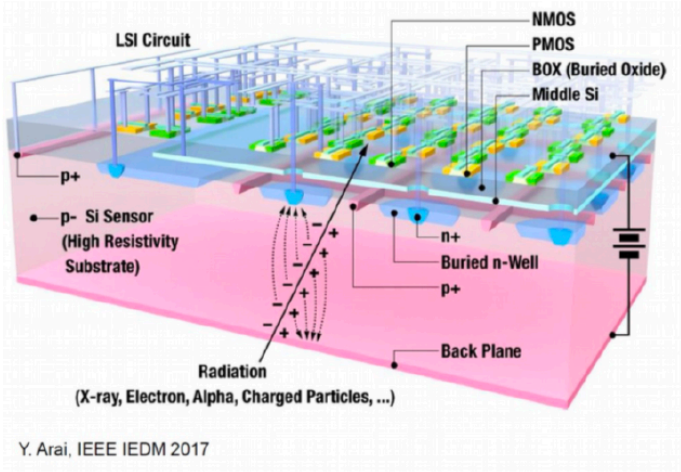
Partially depleted

- The sensing region extends for few tens of um
- The charge collection is performed mainly by **diffusion**
- Collection time > 10 ns
- Competitive charge collection → **low efficiency**
- Maximum radiation tolerance ~10^{13} neq/cm^2
- Low SNR

Fully depleted

- The charge collection is performed mainly by **drift**
- **Fast charge collection** (<10 ns)
- CMOS circuitry can be implemented
- **Competitive charge collection is avoided → good efficiency**
- High radiation tolerance
- Good SNR

Possible implementations



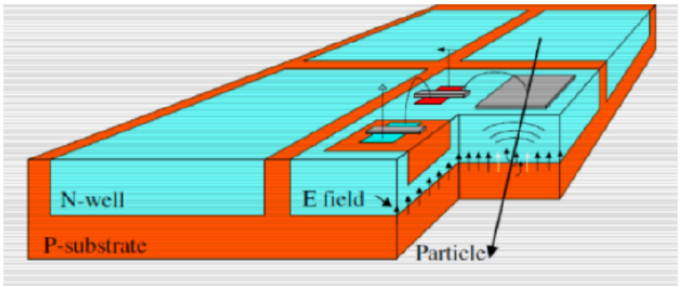
Y. Arai, IEEE IEDM 2017

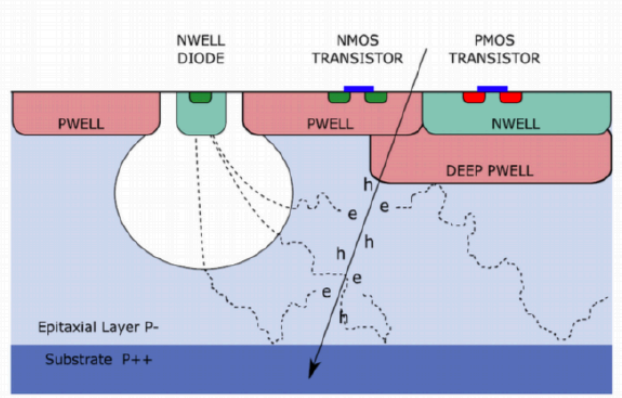
FD SOI

- Buried oxide used to separate the sensor from the electronics
- High resistivity substrate
- Buried oxide →gate effect →2 buried oxide layers used
- Radiation tolerance up to 10Mrad

HV-CMOS

- High resistivity p-substrate (>2kΩ cm)
- The collector node is a deep nwell
- High voltages can be applied
- Fast charge collection
- High efficiency
- CMOS electronics built in the sensing node → high sensor capacitance → high noise



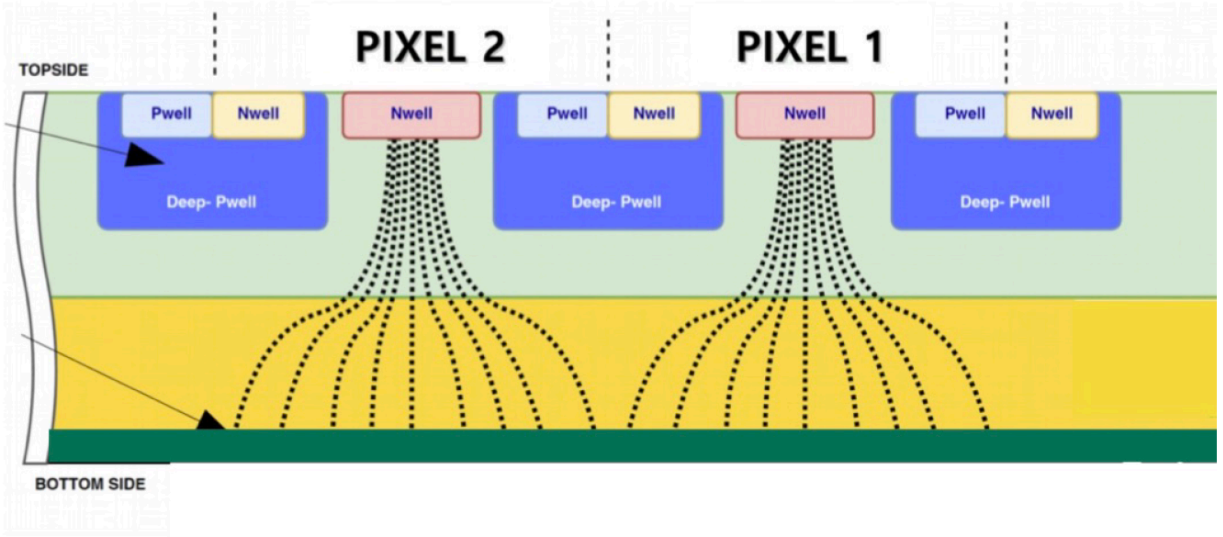


J.P. Crooks, et al., IEEE TNS 2007

ALPIDE

- High resistivity p-substrate (> 1kΩ cm) + epitaxial layer
- Partial depletion
- Sensing node shielded by a deep pwell
- Small sensor capacitance
- Radiation tolerance (TID) up to 700 krad

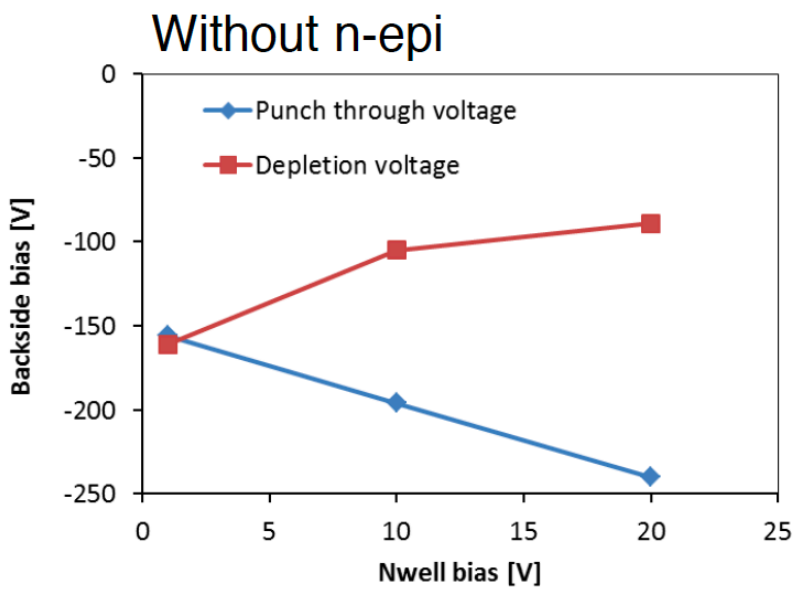
SEED monolithic sensor

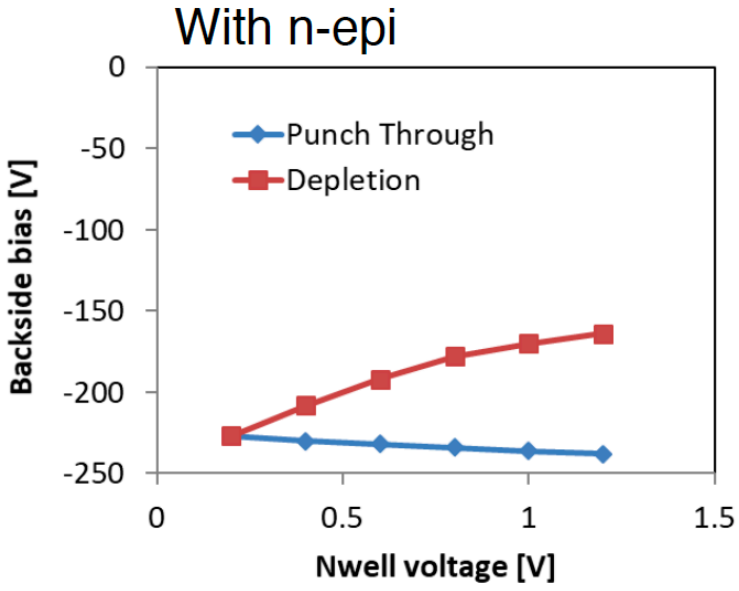


- Goal: full depletion in 100-500 um. The present prototype is 300 um.
- Technology: 110 nm CMOS technology, high-resistivity bulk
- Custom backside process developed (collab. industrial partner)
- The depletion starts from the backside
- At the backside, the main diode is surrounded by a guard-ring
- Both NMOS and PMOS transistors
- The pixel capacitance is kept low $\approx$ 20 fF

Sensor bias

- Bias voltage high enough for full depletion while avoiding early punch through
- Difference between punch through voltage and full depletion voltage must be maximized → larger field and faster charge collection
- Maximum N-well allowed voltage is 1.2 V
- Use of an N-epi layer makes it possible to increase the punch through voltage, enabling full depletion also with a low voltage CMOS process





Goal of the ARCADIA project

ARCADIA will target the development of a novel CMOS sensor platform allowing for:

- active sensor thickness in the range from 50 um to 500 um or more,
- operation in full depletion with fast charge collection only by drift,
- small charge collecting electrode for optimal signal-to-noise ratio,
- scalable readout architecture with ultra-low power capability ($O(10\ mW/cm^2)$),
- easy compatibility with standard CMOS fabrication processes,
- **deliverable**: full-size system-ready demonstrator consisting of a low-power high-density array of CMOS monolithic sensors

Applications

High Energy physics

- Excellent signal to noise ratio is offered by fully depleted sensors
- Large area sensors with less power imply lighter support and cooling infrastructure and improved tracking accuracy
- Large area 100 um thick fully depleted monolithic sensor could be used for sub-ns timing and dE/dx measurements

Space

- Better robustness (smaller number of parts making up the system) as compared to strips in tracking applications
- Low power dissipation essential in space application

Medical applications and X-ray imaging

- CMOS sensors with thick, fully depleted substrate could be exploited for X-ray imaging with energies in the 10 keV range (microscopy, imaging at FELs)
- Large area, thin sensors can be used as hadron probes to get 3D images with limited exposure for the patient

Work packages

- **WP1** - **CMOS Sensors**
  - TIFPA, PG, MI
- **WP2** - **Mixed-signal IP Block design and Chip integration**
  - BO, PV, PG, TO
- **WP3** - **Data Acquisition**
  - BO, TO
- **WP4** - **Application and system characterisation**
  - MI, PD, TIFPA
- **WP5** - **Radiation-hardness**
  - PD, PV

Personale impegnato nella ricerca - 2019

Personale impegnato nella sezione di Pavia		
Nome	**Posizione**	**Impegno**
Luigi Gaioni	RTDB	**30%**
Lodovico Ratti	PA	**10%**
Stefano Noli	PhD	**40%**
Gianluca Traversi (resp.loc.)	PA	**30%**
Carla Vacchi	RU	**40%**
FULL TIME EQUIVALENT		**1.5**

Impegno delle altre sezioni partecipanti:

- INFN Bologna – 1.5 FTE (A. Gabrielli resp. loc.)
- INFN Milano – 0.5 FTE (M. Caccia resp. loc.)
- INFN Padova – 1.1 FTE (P. Giubilato resp. loc.)
- INFN Perugia – 1 FTE (P. Placidi resp. loc.)
- INFN Torino – 3.1 FTE (M. D. Da Rocha Rolo resp. naz.)
- TIFPA Trento – 2.5 FTE (L. Pancheri resp. loc.)

TOTALE: 11.2 FTE

Personale impegnato nella ricerca nel triennio

RU	FTE assigned (without AdR requests)			FTE assigned (including AdR requests)		
	2019	**2020**	**2021**	**2019**	**2020**	**2021**
Bologna	1,50	1,50	1,50	1,50	2,50	1,50
Milano	0,53	0,53	0,73	0,53	0,53	1,73
Padova	1,10	1,10	1,10	2,1	1,10	1,1
Perugia	1,00	1,10	1,10	2,00	1,10	1,10
Pavia	1,50	1,50	1,50	1,50	2,50	1,50
TIFPA	2,50	2,50	2,50	3,50	3,50	2,50
Torino	3,10	5,10	5,10	4,10	5,10	5,10
Total	11,23	13,33	13,53	15,23	16,33	14,53

Richieste finanziarie della sezione di Pavia nel triennio

	2018		2019		2020	
Travels	Collaboration meetings	**2.5 kEuro**	Collaboration meetings	**1.5 kEuro**	Collaboration meetings	**1.5 kEuro**
			Conferences	**3 kEuro**	Conferences	**3 kEuro**
Consumables	Material for test circuits	**4 kEuro**	Material for test circuits	**4 kEuro**	Material for test circuits	**4 kEuro**
Investments	Workstation for CAD design	**5 kEuro**				
Human resources	Assegno di ricerca	**24 kEuro**				
	Total	**35.5 kEuro**	**Total**	**9.5 kEuro**	**Total**	**9.5 kEuro**

Richieste finanziarie globali nel triennio

	WP	Item description	Required funds (k EUR)			type
			2019	2020	2021	
TO	2	Workstation for CAD design	4,0	0,0	0,0	inv
	2	CAD/EDA License fee	1,0	1,0	1,0	lic
	2	CAD support and technical review with Cadence/IMEC	20,0	0,0	0,0	cons
	2	Human Resources (AdR)	24,0	0,0	0,0	AdR
	2	Front-end board for electrical characterisation	0,0	5,0	0,0	cons
	2	Probe-card for tests on wafer probe station	0,0	0,0	7,0	inv
	2	Full CMOS LF110 maskset production	0,0	185,0	0,0	cons
	2	Full maskset for backside processing	0,0	70,0	0,0	cons
	2	Wafer start 25 pcs front-side and back-side	0,0	85,0	0,0	cons
	2	Front-end side BEOL mask respin	0,0	0,0	20,0	cons
	2	Back-end side mask respin	0,0	0,0	20,0	cons
	2	Wafer start 25 pcs front-side and back-side	0,0	85,0	0,0	cons
	2	Collaboration meetings	4,1	5,1	5,1	travel
	2	Conferences	0,0	2,0	2,0	travel
	all	Project Coordination	2,0	2,0	2,0	travel
	1,2	Design meetings, design reviews and test	8,0	8,0	5,0	travel
		Total Torino	**63,1**	**448,1**	**62,1**	

Richieste finanziarie globali nel triennio

PD	5	Mezzanine design for large area sensor	3,0	2,0	0,0	
	5	Mezzanine production for large area sensor	5,0	2,0	0,0	cons
	5,6	Human Resources (AdR)	24,0	0,0	0,0	AdR
	6	Test-beam and x-ray irradiation setup components	5,0	5,0	5,0	cons
	6	Travel coverage and beam-time cost for the TIFPA facility irradiation	0,0	4,0	4,0	beam
	6	Collaboration meetings	1,1	1,1	2,1	travel
		Total Padova	**38,1**	**14,1**	**11,1**	
PG	1,2	Human Resources (AdR)	24,0	0,0	0,0	AdR
	1,2	TCAD/EDA License fee	2,0	2,0	2,0	lic
	1	Workstation for TCAD Simulations/VLSI Design	4,0	0,0	0,0	inv
	4	Travel expenses for characterisation activities	0,0	2,0	3,0	mis
	1,2	Travel expenses for collaboration meetings	2,1	1,1	1,1	mis
	1,2	Conference participations	0,0	3,0	3,0	mis
		Total Perugia	**32,1**	**8,1**	**9,1**	
TIFPA	1	Workstation for TCAD design	4,0	0,0	0,0	inv
	1	Human Resources (AdR)	24,0	24,0	0,0	AdR
	1	Design meetings, design reviews and test	4,0	4,0	4,0	travel
	1	Collaboration meetings	3,5	3,5	2,5	mis
	1	Conferences	0,0	3,0	3,0	mis
	1	Consumables for device testing	0,0	2,0	2,0	cons
		Total TIFPA	**35,5**	**36,5**	**11,5**	

Richieste finanziarie globali nel triennio

MI	4	PCB design and fabrication	0,0	3,0	5,0	cons
	4	Consumables for test beam preparation	0,0	0,0	2,0	cons
	4	Human Resources (AdR)	0,0	12,0	12,0	AdR
	1,4	Collaboration meetings	0,5	1,0	1,0	mis
	1,4	Conferences	0,0	1,0	1,0	mis
	4	Test-beam and proton irradiations travel expenses	0,0	0,0	2,0	mis
		Total Milano	**0,5**	**17,0**	**23,0**	
BO	2	Workstation for CAD design	2,0	2,0	0,0	inv
	3	PCB design and fabrication	5,0	15,0	15,0	cons
	2	Human Resources (AdR)	24,0	0,0	0,0	AdR
	2,3	Collaboration meetings	1,5	2,5	2.5	mis
	2,3	Conferences	1,0	2,0	2,0	mis
	2,3	Travel expenses for WP design and review activities	2,0	2,0	2,0	mis
	2,3	Consumables for circuit testing	1,0	1,0	1,0	cons
		Total Bologna	**36,5**	**24,5**	**20,0**	
		Total Requested Funds (k EUR)	**2019**	**2020**	**2021**	
		943,4	**241,3**	**556,8**	**145,3**	