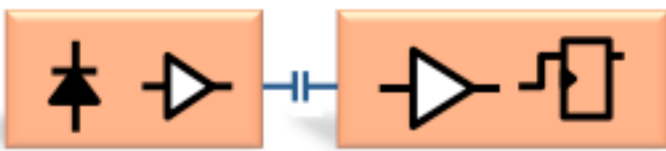


HVR_CCPD and ATLAS CMOS Sensor Development

A. Andreazza - INFN Milano

RD-FA Collaboration meeting, Milano, 6th July 2018

CSN5 Project, duration 2015—2017

Involving INFN and Indian institutes, with strong link to the ATLAS HV/HR-CMOS community

- INFN Bologna – C. Sbarra, A. Sidoti, A. Cervelli, F. Lasagni, G. Torromeo
- INFN Genova – G. Darbo, A. Gaudiello, C. Gemme, P. Morettini, L Rossi, M. Sannino, E. Ruscino, G. Gariano
- INFN Milano – A. Andreazza, M. Citterio, V. Liberali , C. Meroni, F. Ragusa, F. Manca, F. Sabatini, A. Stabile, S. Monzani

H. Shrimali, I. Yadav, A. Joshi

Introduction

- HVR_CCPD:
  the acronym reflects the two pillar of the proposal:

High **V**oltage/High **R**esistivity CMOS Pixel Detectors

- – Rivelatori CMOS con regione di svuotamento
- – Valutazione della tecnologia BCD8 di STMicroelectronics
  - dispositivi prodotti
  - test di irraggiamento
- – Sviluppo di dispositivi monolitici:
  - test della cella analogica in diversi tecnologie
  - primi prototipi monolitici
  - passi verso un rivelatore completo

Today presentation

Capacitive **C**oupled **P**ixel **D**etectors

- – Accoppiamento capacitivo tra sensore a pixel ed elettronica di lettura
  - processo più semplice ed economico rispetto a bump-bonding
- – Sviluppo della tecnica per garantire uniformità e ripetibilità del processo
- – Passi per industrializzazione del processo

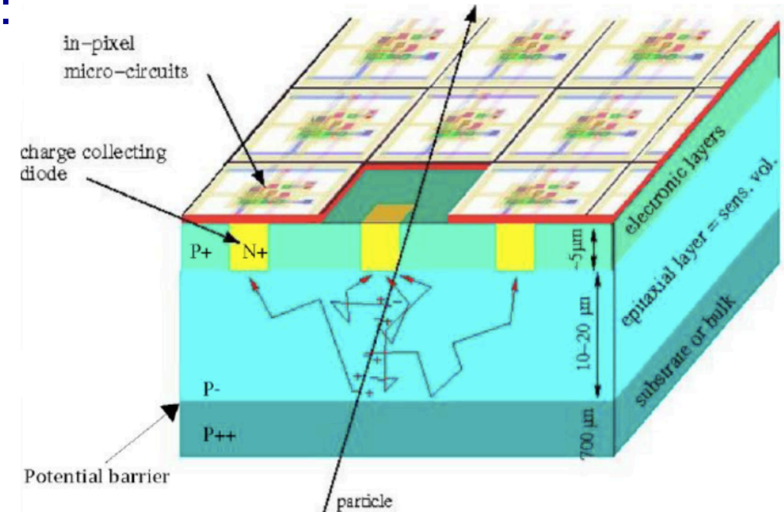
Backup slides

Depleted CMOS detectors

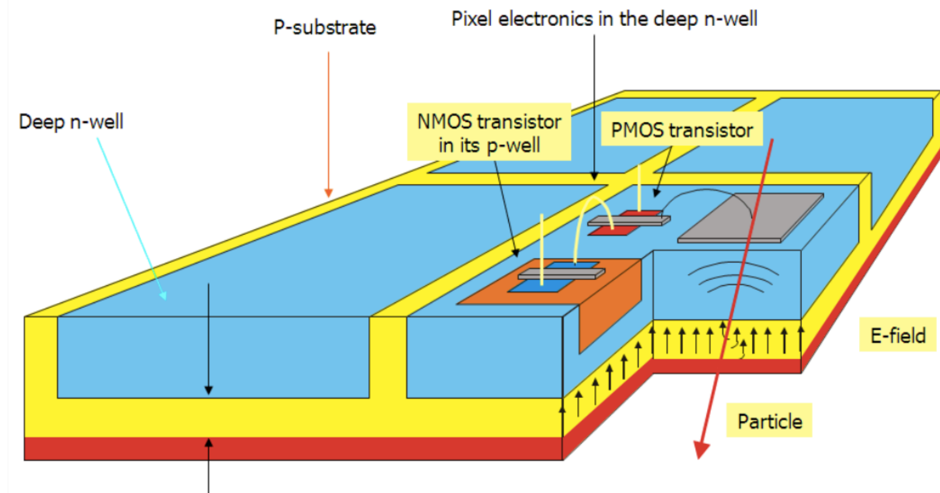
- Standard CMOS detectors collect charge by diffusion:
  - slow signal O(1 μs), not rad-hard (trapping)
- CMOS detector with a **depleted layer**
  - charge collection by drift:
    - full ionization signal (in the depleted region)
    - fast O(10 ns): no trapping
- Enabling technologies:

$$d = \sqrt{\varepsilon_{Si}\varepsilon_0\mu_{carrier}\rho(V + V_{BI})}$$

  - **High Voltage** processes
    - Availability of processes with high voltage capability,
      driven by automotive and power management applications
  - **High Resistivity** substrates
    - Foundries accepting/qualifying wafers or epitaxial substrates with mid-high resistivity
  - **130-180 nm feature size**
    - deep submicron technologies needed for the design of radiation hard electronics
    - multiple-well process to decouple front-end electronics from the sensitive region



I. Peric, Nucl. Instr. and Method A 582 (2007) 876



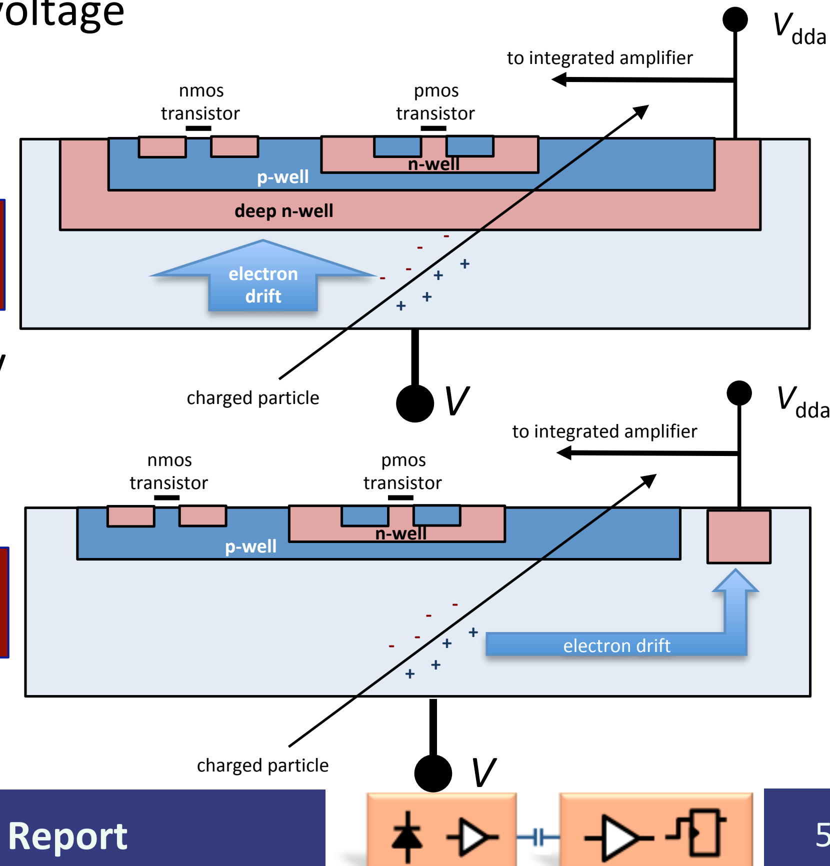
Depleted CMOS technologies

- Depletion zone built in a 10-30 µm mid-resistivity p-type epitaxial layer (ex.: AMS, TowerJazz)
  - Can be fully depleted with few Volt
  - Signal 1-2 ke
- Collection electrode is a deep n-well or a buried n-layer, implanted onto a p-type substrate (ex.: LFoundry, STMicroelectronics)
  - Size of depleted region limited by the breakdown voltage
  - Signal up to 10-20 ke (varying with irradiation)
- Front-end electronics **inside** the collecting well
  - **uniform charge collection**
  - **short drift path → less trapping**
  - **large electrode capacitance** ~100 fF, dominated by (parasitic capacitance between the deep wells)

large electrode /large fill factor

- Front-end electronics **outside** the collecting well
  - **non uniform drift field**
  - **long drift path → more sensitive to trapping**
  - **small electrode capacitance** <10 fF

small electrode /small fill factor



Collaborations

- Collaborative effort of ~25 ATLAS ITk institutes
- Capable of attracting also **non-ATLAS institutes** and resources

AIDA 2020

WP6: Novel high voltage and resistive CMOS sensors

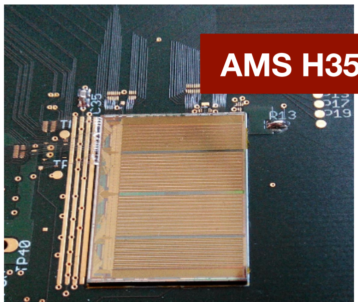
STREAM, Smart Sensor Technologies and Training for Radiation Enhanced Applications and Measurement

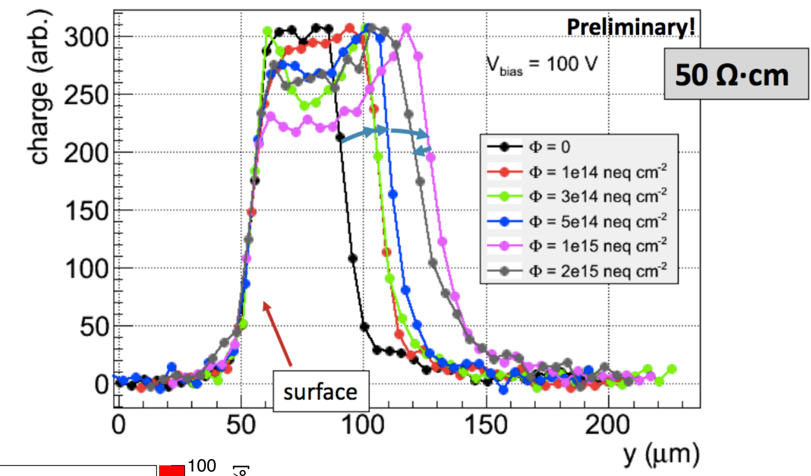
Innovative Training Network (ITN) under the Marie Skłodowska-Curie Actions

`https://stream.web.cern.ch/`

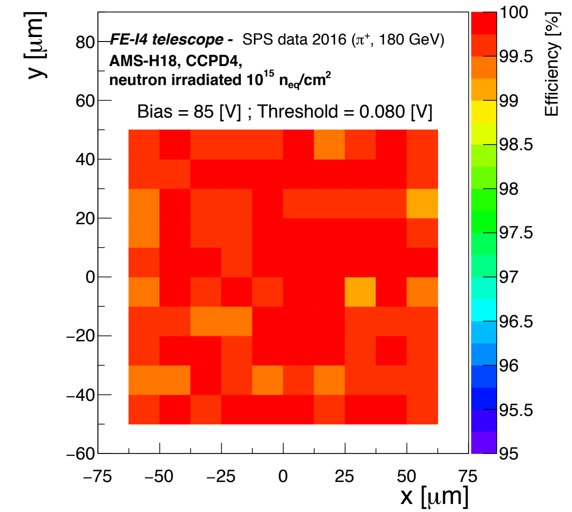
Large Electrode Prototypes

- Past years research showed depleted CMOS performance comparable to hybrid pixel detectors:
  - large size detectors

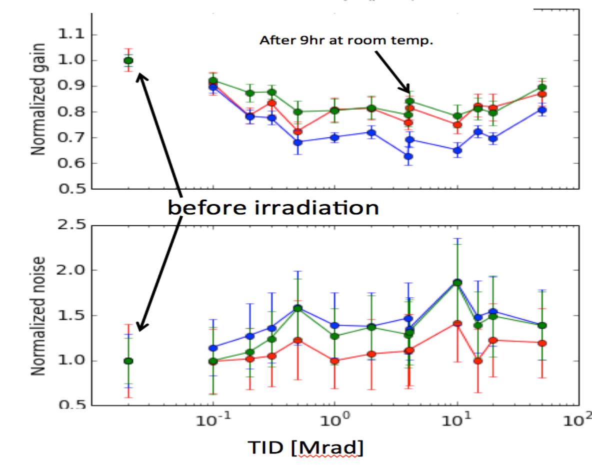




  - efficiency >99%



  - radiation hard up to NIEL 10^{15} n_{eq}/cm^2, dose 100 Mrad



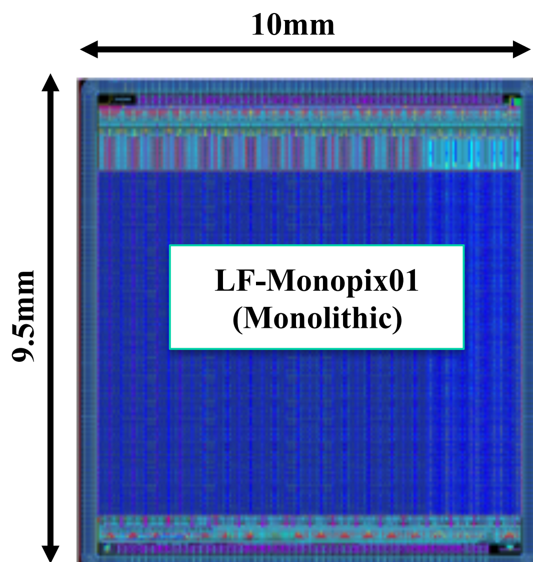
- but with some limitations:
  - marginal *timewalk* due to large pixel capacitance $t_{\mathrm{rise}} \propto \frac{1}{g_m} \frac{C_{\mathrm{in}}}{C_f}$
  - integration of CCPDs in a large scale detector: *through silicon vias, large power consumption, interface with RD53 FE*

INFN

ATLAS CMOS Prototypes

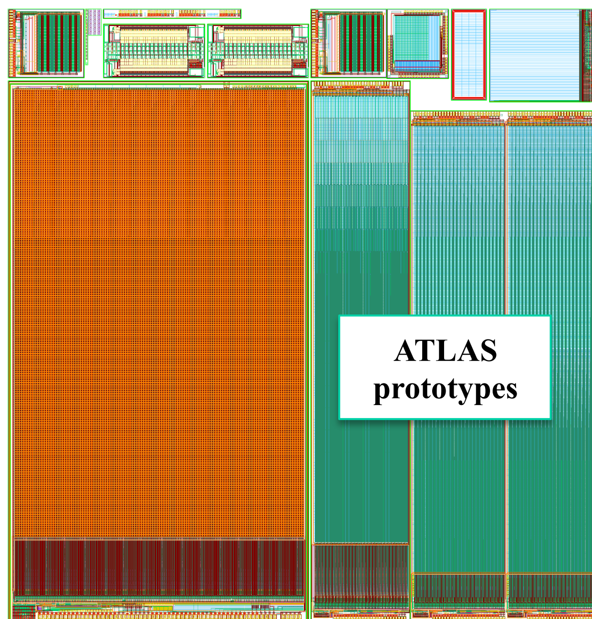
LFoundry

- Subm. in **Aug. 2016**
- **Monopix01** and **Coolpix1**
- 1 cm^2 size
- 50 x 250 μm^2 pixels
- Fast standalone R/O
- Column drain approach



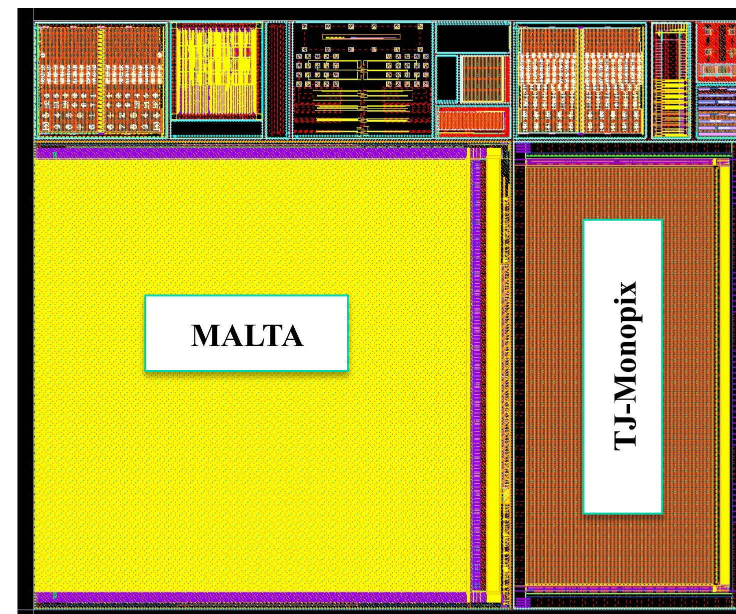
AMS H180

- Subm. in **Jan. 2017**
- **Mu3E** + **ATLAS** (monolithic)
- Additional production step – isolated PMOS
- 80 and 200 Ωcm wafers
- Reticle size about 21mm x 23mm



TowerJazz

- Subm. in **Sep. 2017**
- Two large scale demonstrators **MALTA** and **Monopix**:
  - Small fill-factor pixels
  - Asynchronous matrix readout (MALTA)
  - Column Drain Read-Out (Monopix)



Path towards monolithic sensors

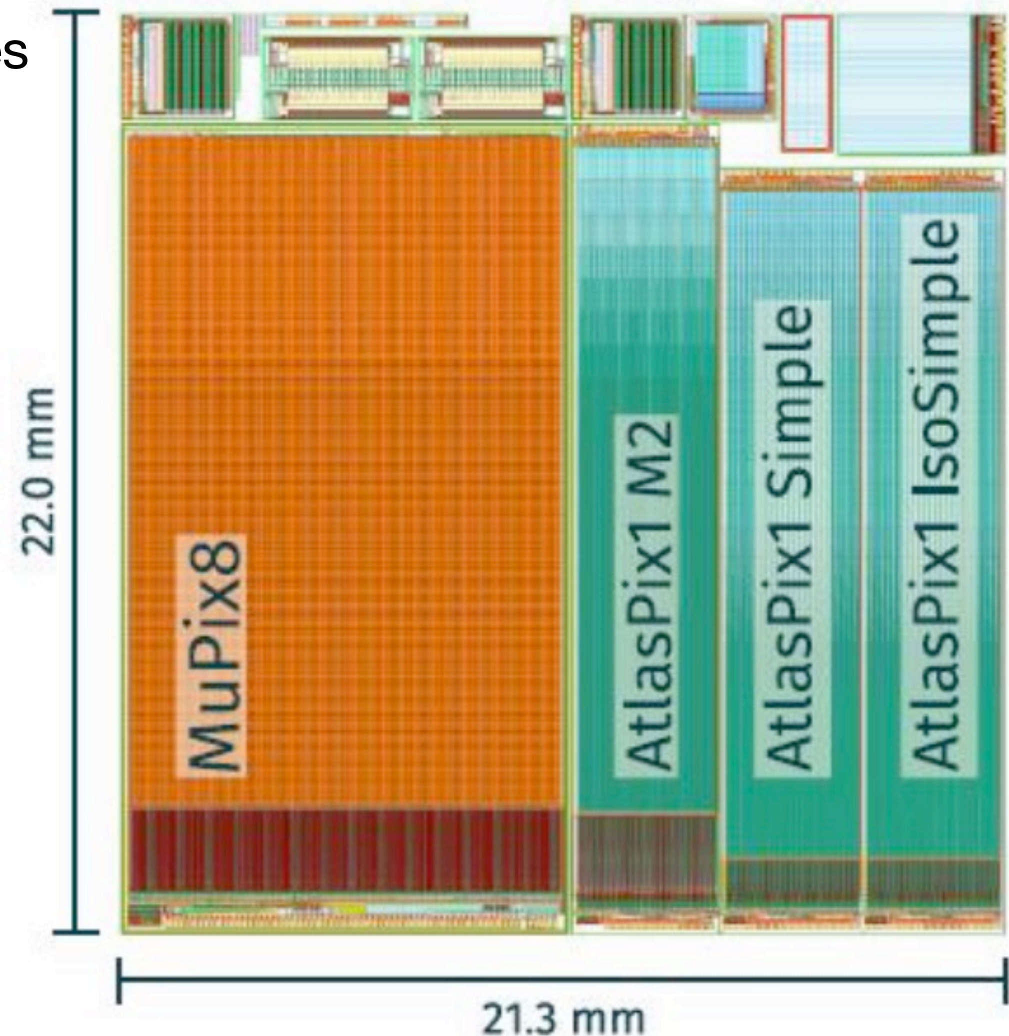
- Up to 2016: analog cell design and characterization (*)
- 2017 prototypes:
  - verify compatibility between analog cell and digital readout on column (#)
  - small fill factor radiation hardness qualification

Device	Process	Design	Pixel size	Matrix size	Availability date
*LF-CPIX	LFoundry 150 nm	Large-FF	$50 \times 250\ \mu m^2$	106×36	July 2016
#LF-Monopix	LFoundry 150 nm	Large-FF	$50 \times 250\ \mu m^2$	129×36	July 2017
MuPix8	ams aH18	Large-FF	$80 \times 81\ \mu m^2$	200×128	October 2017
#ATLASPIX_M2	ams aH18	Large-FF	$50 \times 60\ \mu m^2$	320×56	October 2017
#ATLASPIX_Simple	ams aH18	Large-FF	$40 \times 130\ \mu m^2$	400×25	October 2017 INFN
*Investigator	TowerJazz 180 nm	Small-FF	various		
#MALTA	TowerJazz 180 nm	Small-FF	$36.4 \times 36.4\ \mu m^2$	512×512	January 2018 INFN
#TJ-Monopix	TowerJazz 180 nm	Small-FF	$36 \times 40\ \mu m^2$	224×448	January 2018

- In 2018: add periphery and readout architecture suitable for HL-LHC operation:
  - readout rate at 1 Gbps
  - SEU hardened configuration registers
  - memory buffer for trigger latency

AMS aH18 devices

- Large-Electrode monolithic prototypes
- AMS 180 nm process
- **MuPix8** (Mu3e experiment at PSI)
  - 128×200 pixel matrix
  - 80×81 μm^2 pixel size
  - direct write to periphery, asynchronous readout
- **ATLASPix1 M2**
  - 320×56 pixel matrix
  - 50×60 μm^2 pixel size
  - triggered readout with local buffering
- **ATLASPix1 Simple**
  - 400×25 pixel matrix
  - 40×130 μm^2 pixel size
  - asynchronous readout
  - with and without ***p*-well isolation** layer



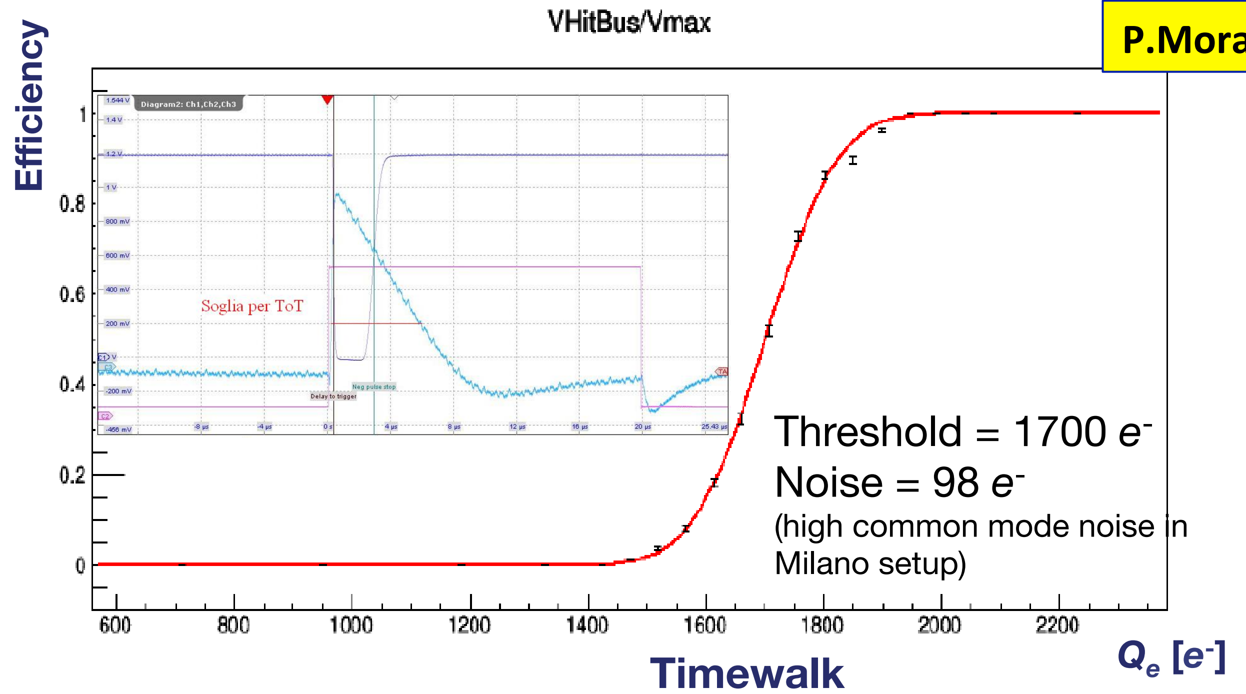
MuPix8: Analog cell characterization

P.Moraschi

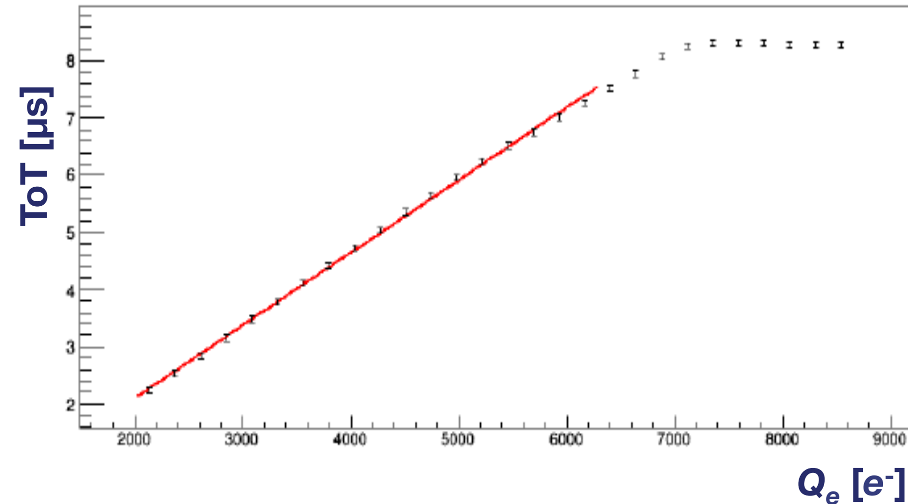
- Efficiency of discriminator pulse (HitBus)
- Average over 2000 injections
- Interpolating with an error function

$$Q_e = \frac{V_{inj} \cdot C_{inj}}{q}$$

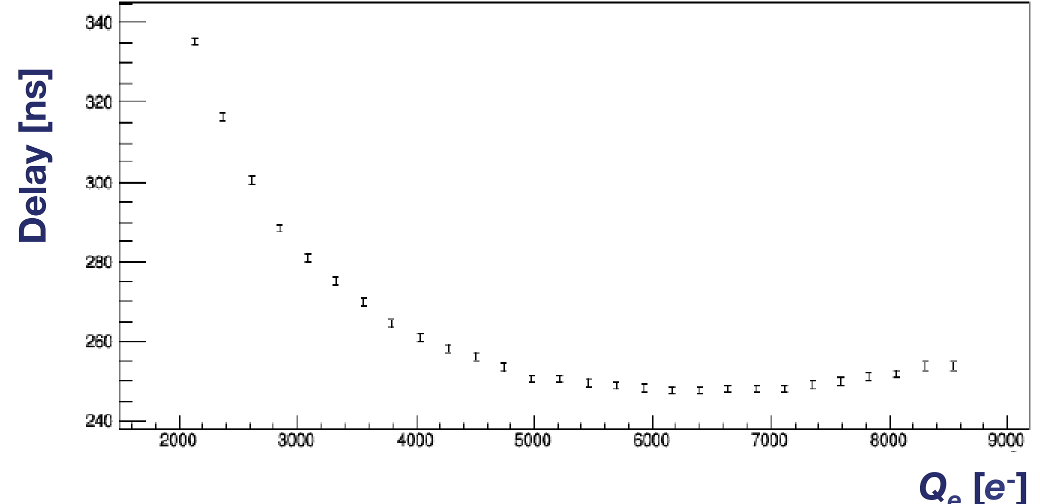
$$C_{inj} = 0.76\, fF$$



Time over Threshold

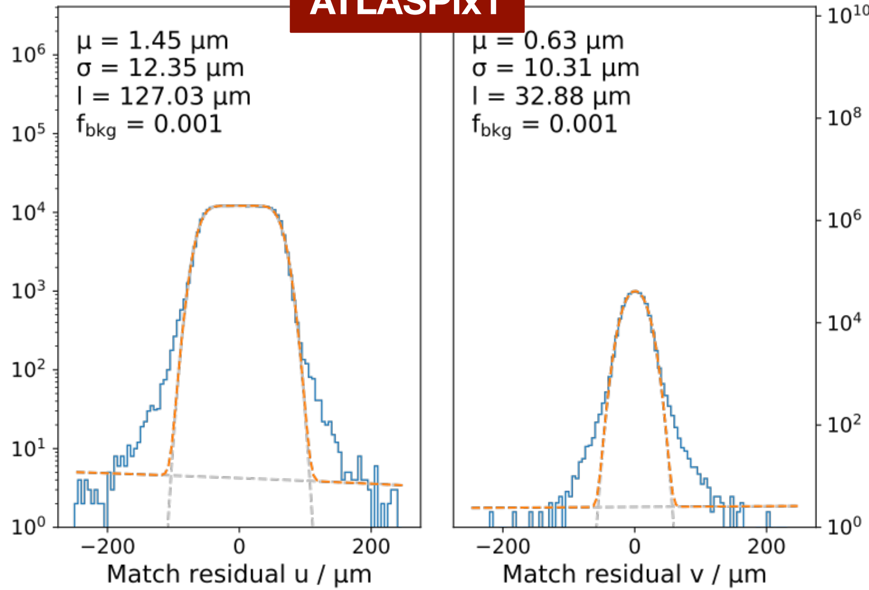


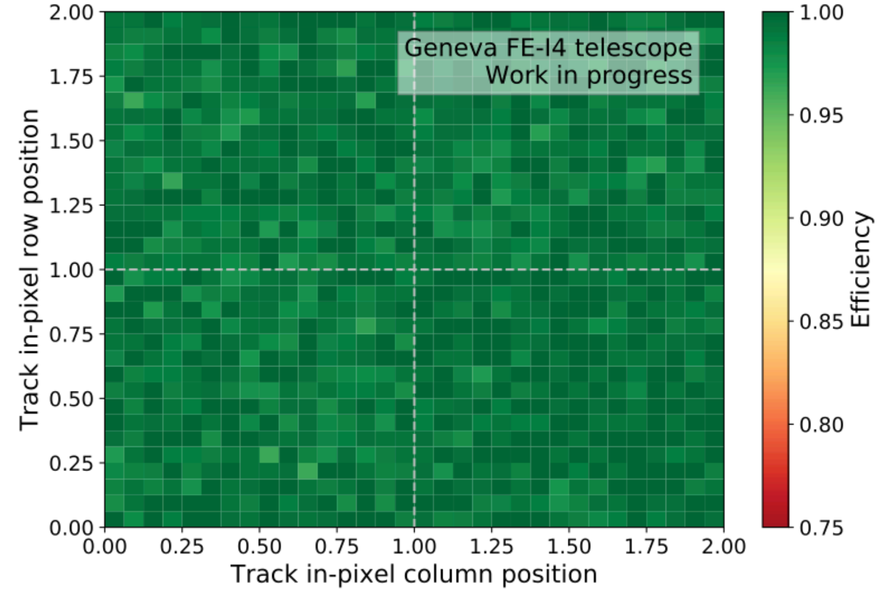
Timewalk



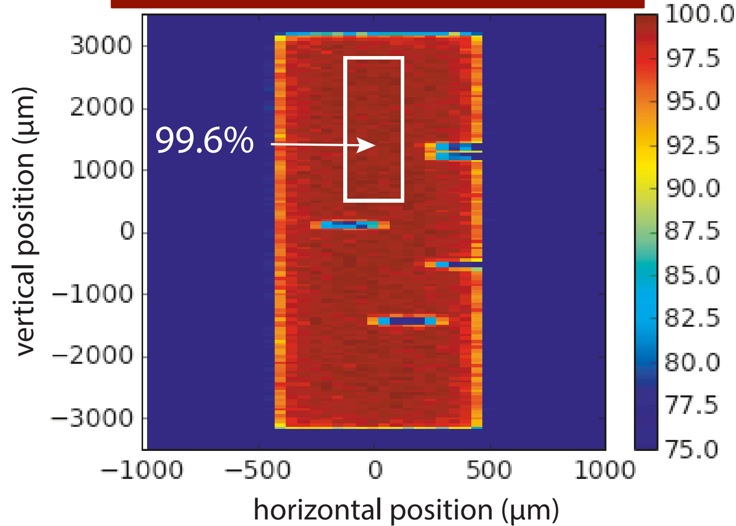
Large FF monolithics: test beam results

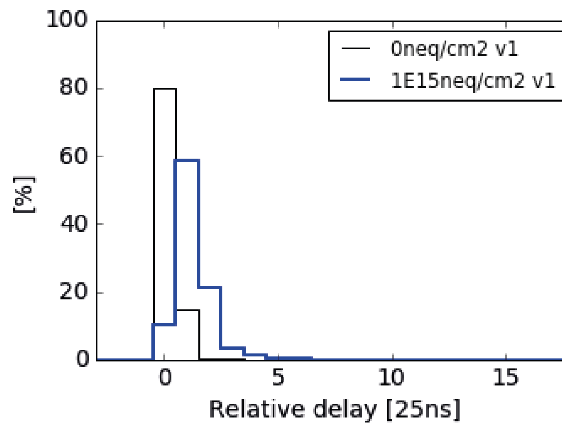
ATLASPix1



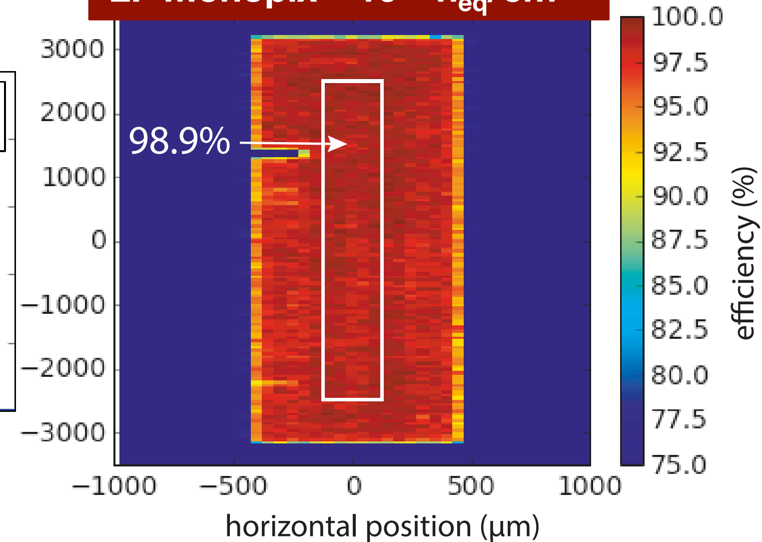


LF Monopix – not irradiated

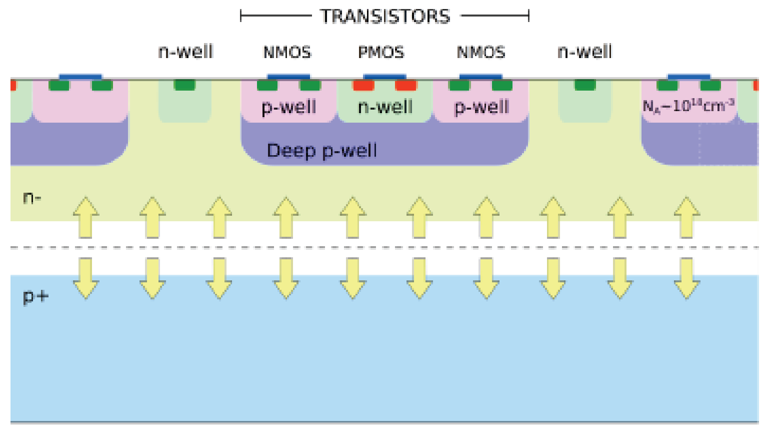


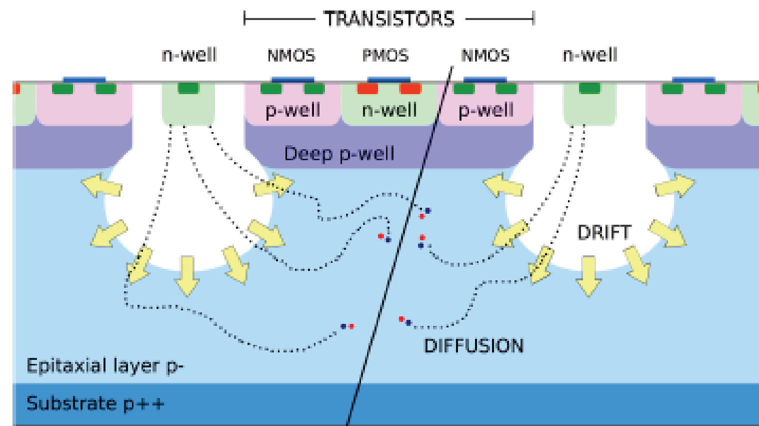


LF Monopix – 10^{15} n_{eq}/cm^2



TowerJazz Investigator chip





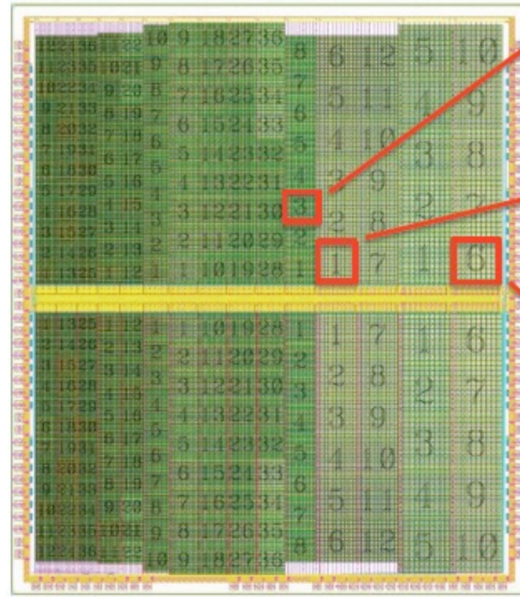
Modified Process

- Added a planar junction on the whole sensor area
- Keeping low capacitance (~fF):
  - fast signal
  - low noise
- Increasing radiation hardness

- CERN SPS Test Beams in 2016 and 2017
  - 180 GeV pion beam

Standard Process

- Difficult to extend depletion region below the p-well
- Limited radiation hardness



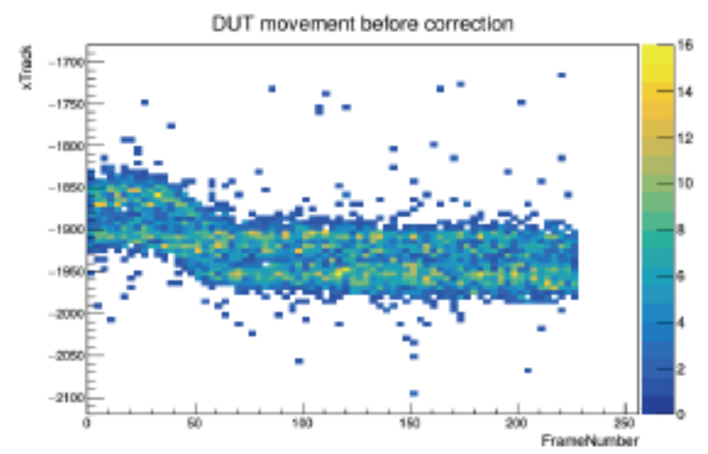
Minimatrix 106
- Pixel size 30x30μm^2
- Electrode size 3x3μm^2
- Opening 3μm

Minimatrix 112
- Pixel size 40x40
- Electrode size 3x3μm^2
- Opening 30μm

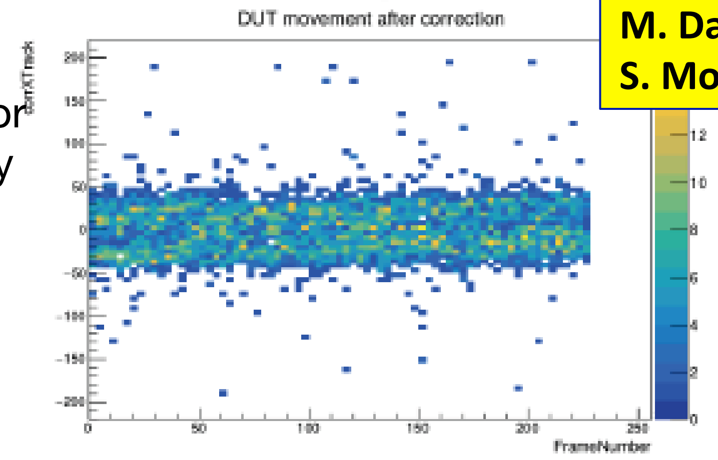
Minimatrix 129
- Pixel size 50x50μm^2
- Electrode size 3x3μm^2
- Opening 40μm

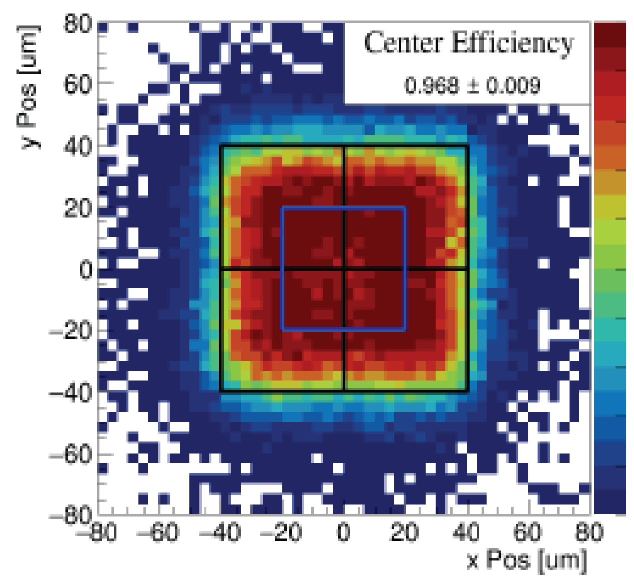
TowerJazz Investigator chip: test beam

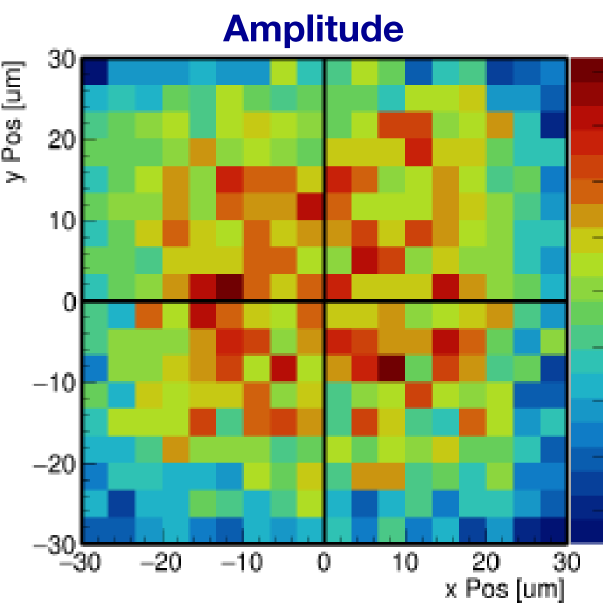
M. Dalla
S. Monzani

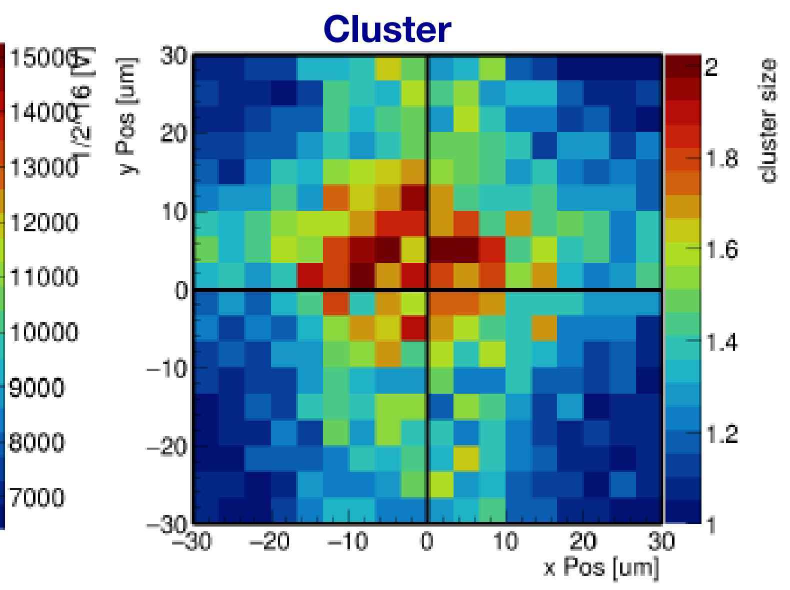


Correction of detector movement due to dry ice evaporation







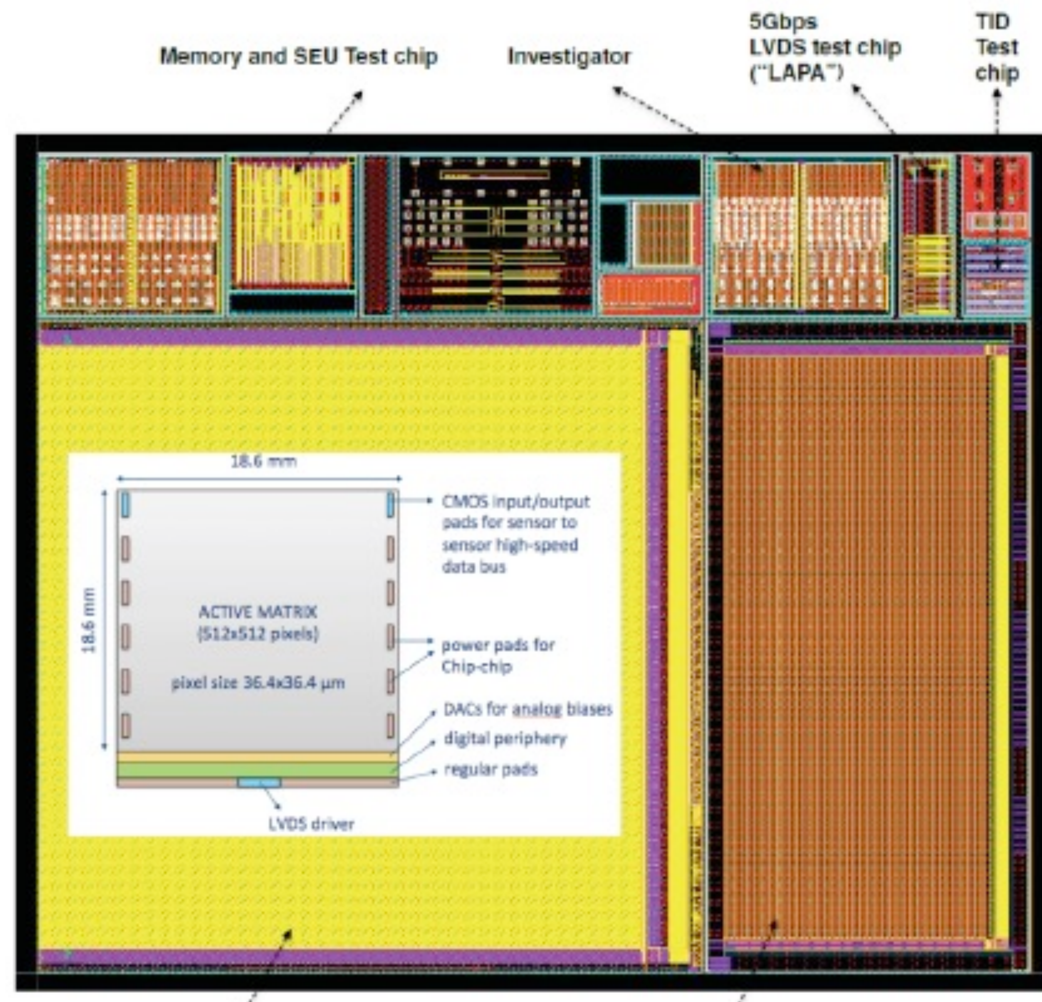


- 40 µm square pixels, irradiate at 10^{15} n/cm^2, 30 µm spacing, 3 µm electrode size
- **97% efficiency** after irradiation: ***matching ITk requirements***

TowerJazz monolithic prototypes

MALTA

- 20x22 mm (full size ITk sensor)
- 512x512 pixels, 36.4x36.4 μm^2
- Asynchronous readout
- Fast signal, with pulse clipping (no Time over Threshold measurement)
- Pulse height estimated from timewalk
- 40 bit parallel bus differential **output at 2 GHz**
- Possibility of data and power chain between chips

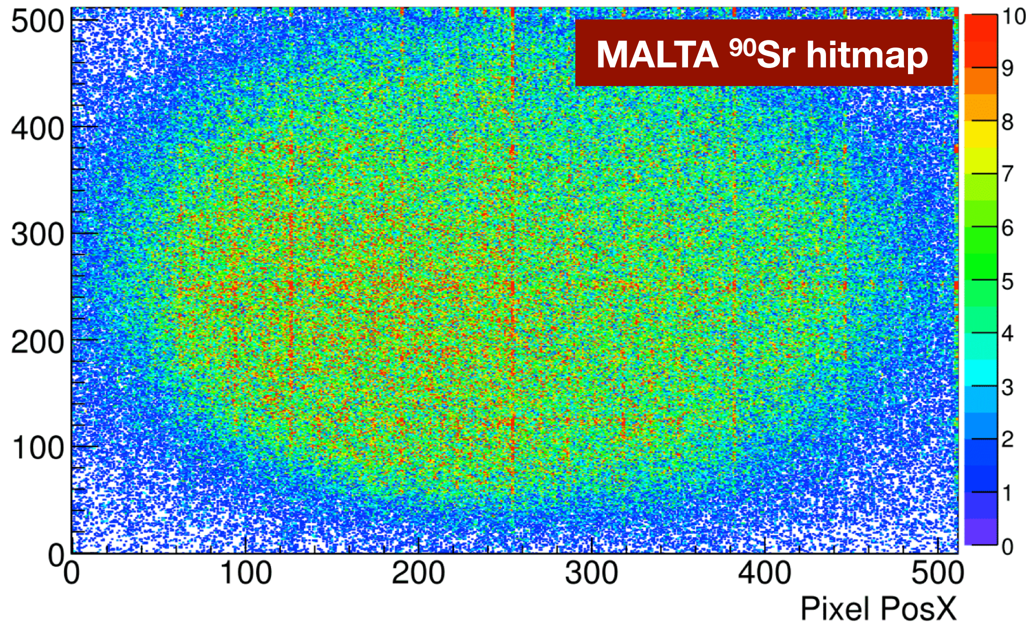


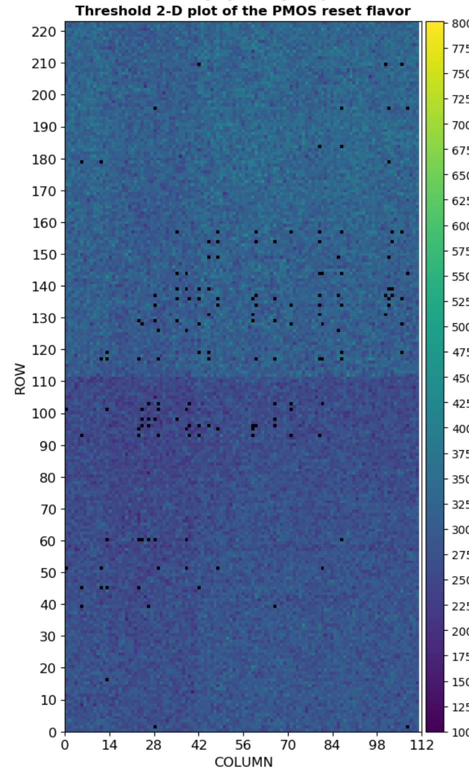
MONOPIX

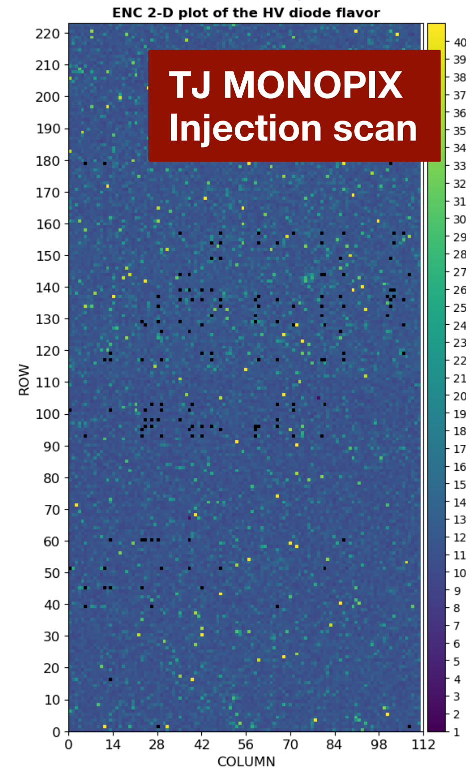
- 20x10 mm (half size ITk sensor)
- 448x224 pixels
- 36x40 μm^2 pixel size
- Same analog cell as MALTA, without pulse clipping (ToT measurement)
- Classic column drain architecture

TowerJazz preview

- Very early results from **Bonn** and **CERN** groups
- First test on beams on ELSA in Bonn (not shown)
- Installing on SPS beam line right now
- Preparation of irradiated samples ongoing







- **ENC: 5-10 e^- at 500 e^- threshold**
- Time delay along the matrix 12.2 ns
- All in agreement with simulation

- **Threshold 230-300 e^-** (different electrode layout)
- **Threshold dispersion 15-20 e^-, ENC: 10 e^-**

HV/HR CMOS status for ATLAS

- CMOS detectors are presented in the ITk pixel TDR as an *opportunity* with respect to baseline hybrid detectors:
  - targeting outermost pixel barrel layer:
    - rate should be manageable with the available 150-180 nm integration scales
    - less strict radiation hardness qualification and risk
    - still significant economic and schedule gain (20% of silicon surface)
  - Schedule comparable with TSMC 65 nm chips
    - Full size-preproduction chip by 2nd quarter 2019
- PDR: October 2018

Next step for completing R&D

- Need to show the technology is capable for integration in a real HL-LHC experiment:
  - **Hit data Memory and Trigger**
    - Analysing memory design in order to efficiently use bandwidth, distribute power and use little space (150-180 nm node instead of 65 nm)
    - Consider to "pack" hit information of multiple hits into "clusters" to achieve more efficient storage
  - **Serializer and output**
    - Data out after trigger is serializer with 640 / 1280 Mbps (Data output is LVDS driver with pre-amphasis)
    - Interface with DAQ I/O, PLL
  - **Power and bias**
    - Generate all bias voltages internally
    - Serial power: internal regulators for 1.8V
    - Substrate bias voltage supply (or internal generation)
  - **SEU hardening**

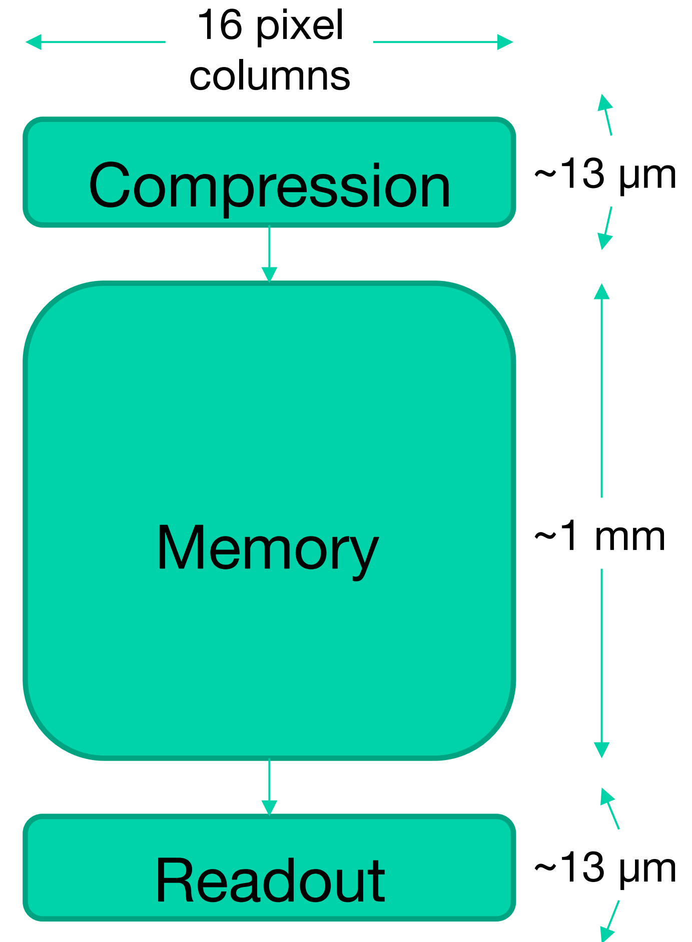
MALTA Trigger Memory

L. Vigorelli

Example:

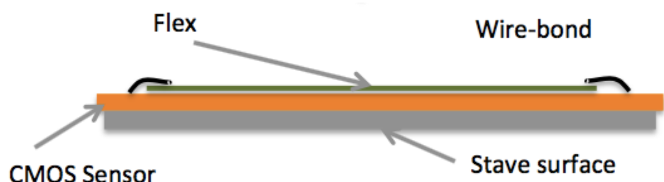
- MALTA transfers hits asynchronously from matrix to periphery: hit data must be stored waiting until trigger latency is elapsed

- Compression algorithm to reduce the information required to store the bunch crossing ID
- A 30% gain in area is achieved by exploiting 2 redundancies:
  - ID repetition
  - ID constant increase
- Sufficient to store a flag if the hits belongs of does not belong to the same bunch crossing of previous hits
- The code is already synthesisable (even if there is still a lot of refinement work to do)
- From synthesis we find that compression and readout logic will add around 13 µm on top and 13 µm at the bottom

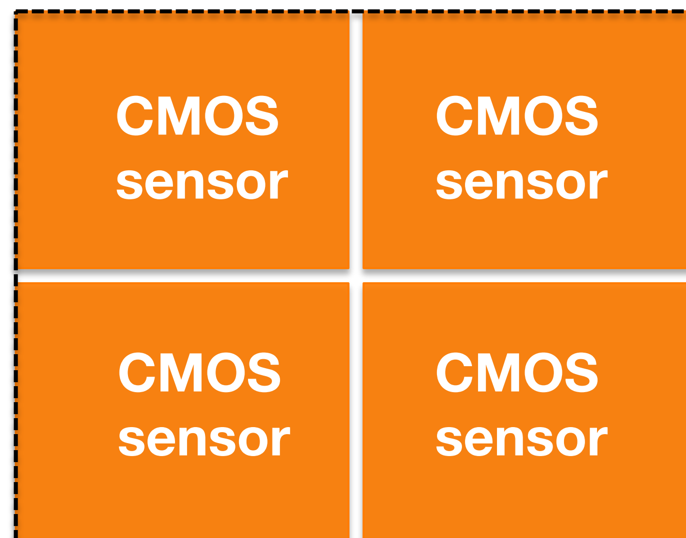


CMOS Modules in ATLAS

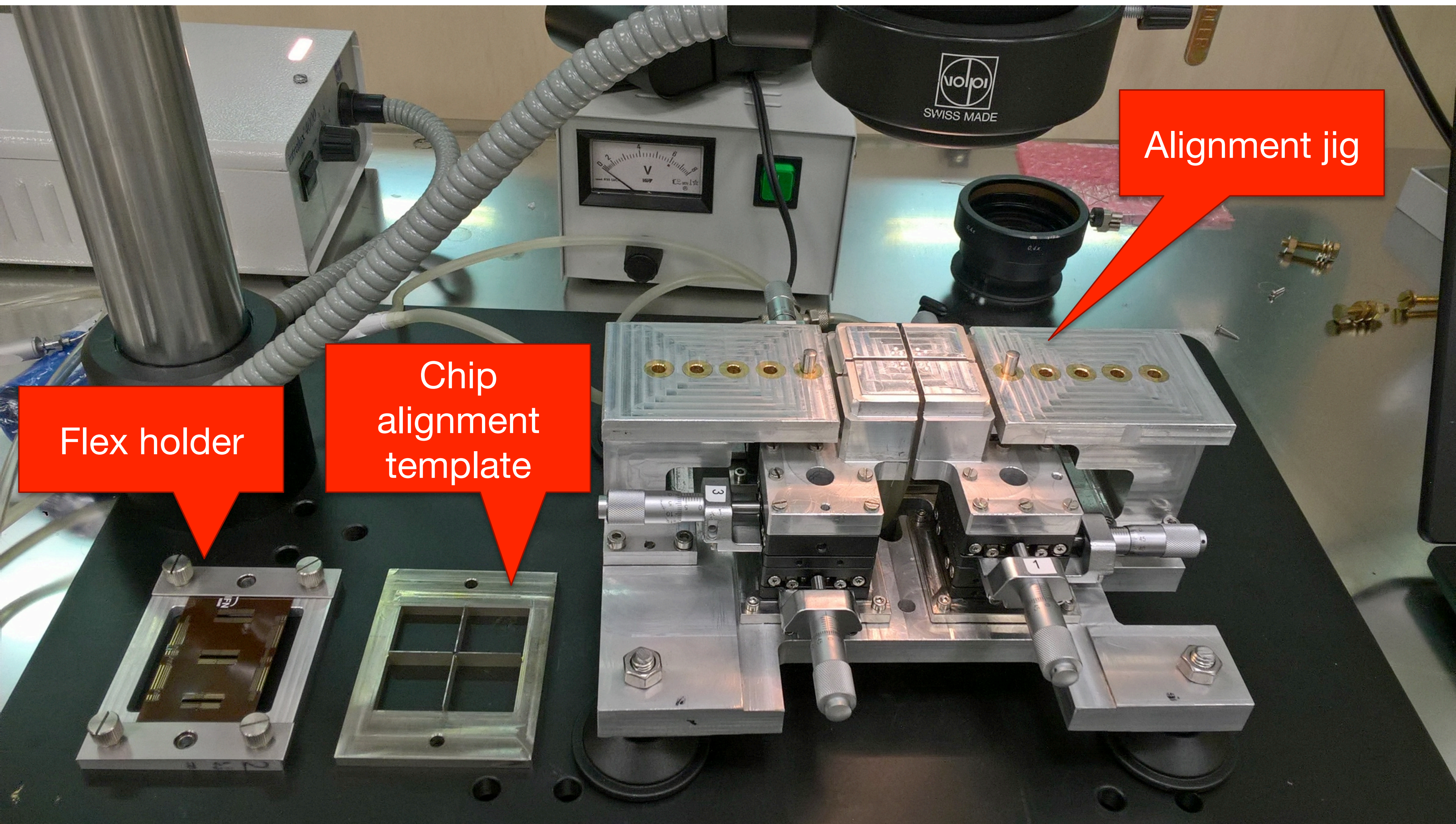
- Pseudo-quad modules (similar to 3D in R0 or L1)
  - FE-to-FE alignment done at assembly level
  - Either relative alignment of 4 FEs, or alignment of FEs to Flex
- No sensor tile
  - Rigidity needs to be provided by flex
  - Signals on FE surface may couple to flex
  - HV insulation between local support and sensor backside



- Minimizing active area gaps
  - Dead region between chips
  - To minimize gaps require placement position at least at the level of **dicing tolerances**
  - Should target physical gaps ≤ 150 μm
  - ALICE achieved 150 μm on active area gaps

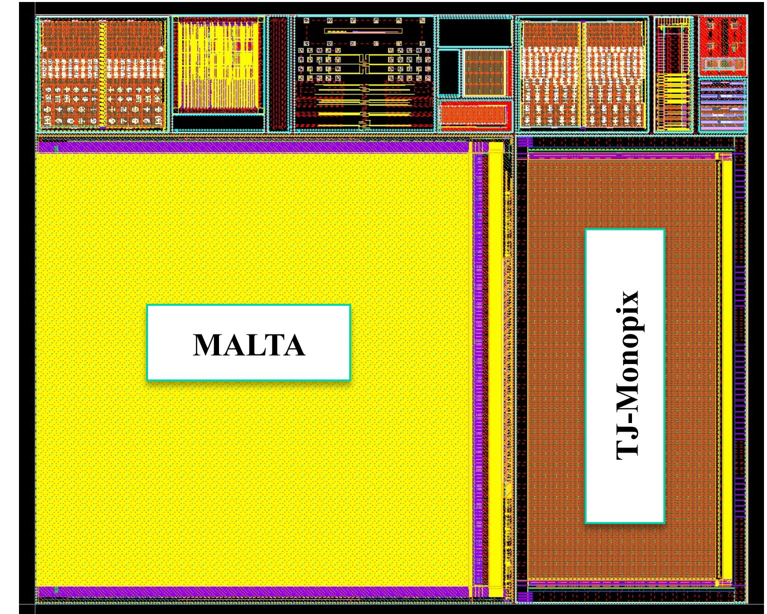


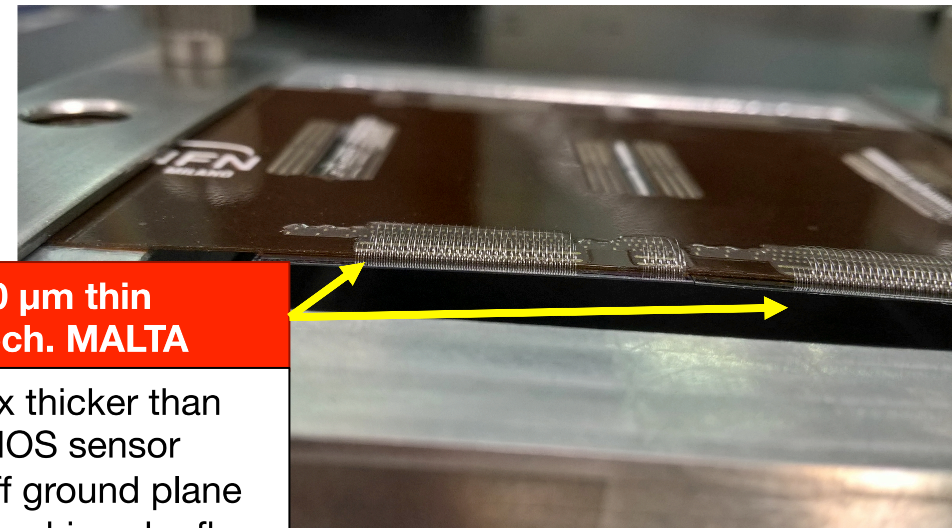
Alignment Jig



Module components

- Mechanical flexes for MALTA and ATLASPix
  - 2 layers, 35 µm copper
  - bottom layer: ground plane to provide stiffness to assembly
  - top layer: pad layout to check wire bonding
- Mechanical MALTA chips from TowerJazz:
  - only top metal layer,
  - chips thinned to 100 µm thickness



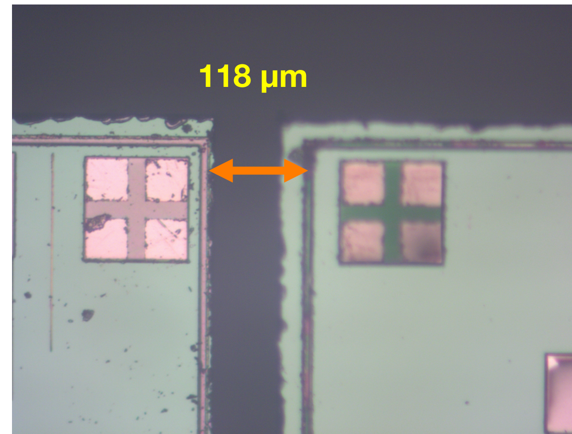


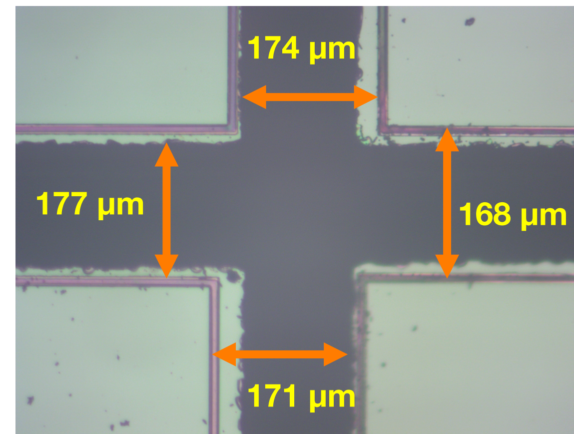
100 µm thin mech. MALTA

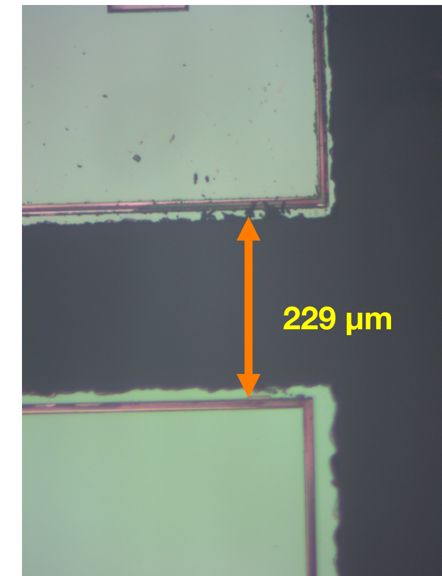
Flex thicker than CMOS sensor
Stiff ground plane
Bow driven by flex

Alignment results

- Limited experience, with only three assemblies
- Different target distances between scribe lines: 170 µm, 80 µm, **100 µm**
- **Central position**
  - **distance between chips scribe lines <10 µm**
  - measurements reproducibility σ = 4 µm
- **Parallelism**
  - more critical: seen deviations up to 60 µm/20 mm on first assembly
    - attributed to vibrations when switching on the vacuum
  - Improved in later assemblies (<30 µm/20 mm)
- Most tedious operation is the check of the far edges: completely manual stage with micromanipulators and 60 mm range

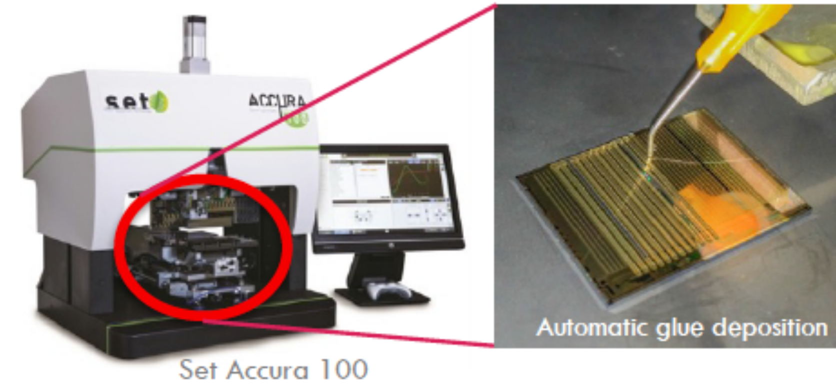


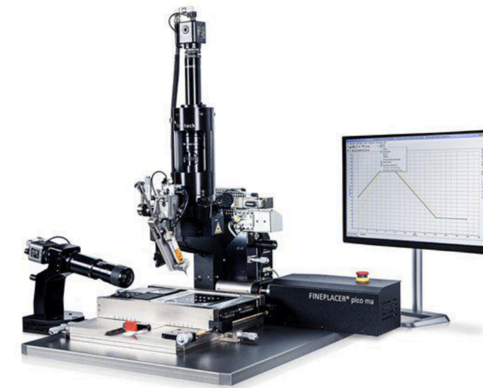


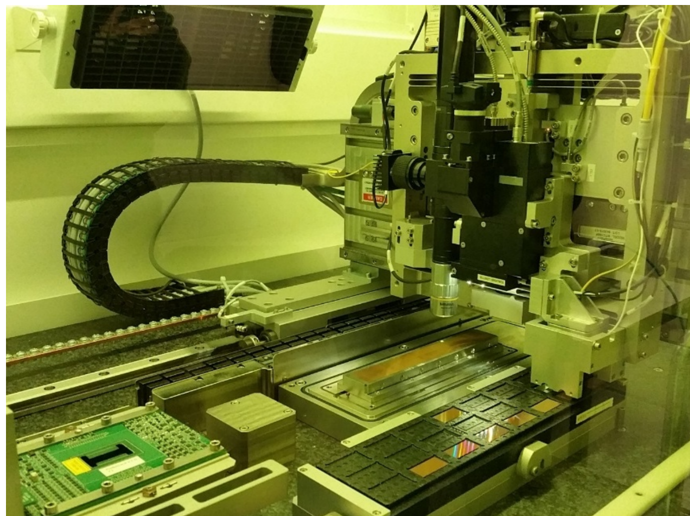


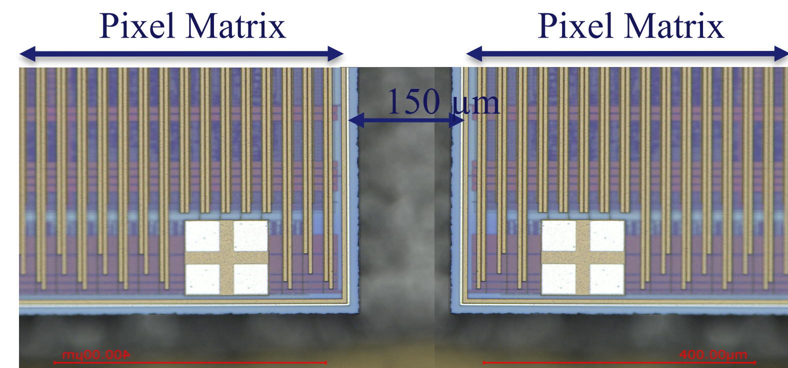
Final target

- Pick and place of flip-chip machine:
  - placement accuracy at ~10 μm precision
  - controlled glue deposition
  - curing
  - possibility of C4 bonding
- Flex to aligned FE (à la ALICE)
  or FE to Flex (microelectronic integration)?
  - alignment marks on CMOS sensors and flexes
  - try to benefit at most from ALICE experience









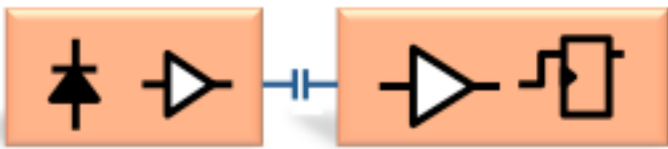
Summary and outlook

- Depleted CMOS detectors have significantly increased their level of maturity in the past years:
  - Large electrode design demonstrated radiation hardness up to NIEL 10^{15} n_{eq}/cm^2, dose 100 Mrad
  - Fully monolithic design is feasible:
    - baseline solution for Mu3e experiment
    - **proposal for ATLAS HL-LHC upgrade**
    - Tested analog properties of devices in LFoundry, AMS and TowerJazz processes
    - First set of large size devices available in September 2017 (AMS) and January 2018 (TJ)
    - Preparation of a full size, rad-hard, completely integrated device
- Thanks to HVR_CCPD, INFN is well introduced in this R&D line
  - AIDA 2020 WP6
  - ITN STREAM
  - "ATLAS" CMOS groups

What matters to RD_FA?

- Reasonable hope is to have a depleted CMOS which could be operated at the LHC:
  - rate ~1 MHz/mm^2
  - time resolution <<25 ns
  - rad hard: *even if it fails not an issue for e^+e^- colliders*
  - cost 22 Eur/cm2 (at 100% yield)
  - availability end of 2019
- Depleted MAPS for e^+e^- colliders?
  - Goal is to have thin sensors:
    - small fill factors are better suited:
      - thin sensitive region
      - low power design (small input capacitance+asynchronous readout) **<75 mW/cm^2**
      - may not need pixel-by-pixel tuning → small pitch
  - Is the additional time resolution w.r.t. MAPS needed?

What is the way to re-use ATLAS activities for RD_FA?



HVR - CCPD

BACKUP SLIDES

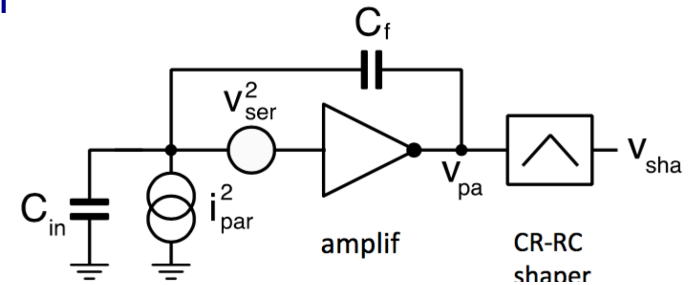
Istituto Nazionale di Fisica Nucleare

Other activities (in backup)

- Developed a CCPD prototype with STMicrolectronics
  - Indication of acceptable radiation hardness of the process
  - Completion of characterization after regaining access to irradiated samples in LNS
  - Difficult to move toward a full scale application
- Capacitive Coupling hybridisation technique
  - demonstrated highly uniform spacer deposition
  - improved uniformity by 20% with respect to standard flip-chip
  - testing wafer reconstruction technique:
    - bridging the gap between electronics and sensor manufacturers, aiming to wafer-to-wafer bonding

Capacitance, risetime, noise

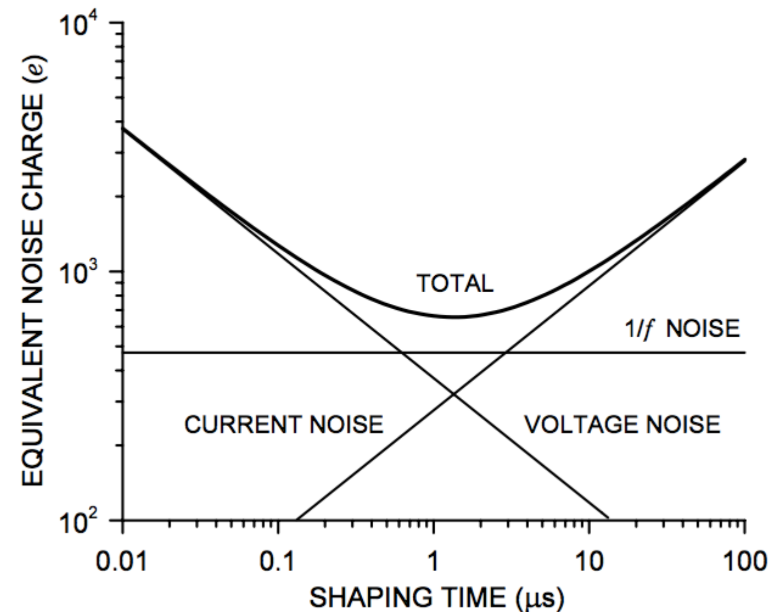
- Integrated front-end electronics: charge amplifier+shaper
- Equivalent Noise Charge (ENC)
  noise measured as equivalent signal at input



$$ENC^2 = \frac{e^2}{4q^2}\left(\frac{\tau}{2}I_0 + \frac{1}{2\tau}V_0 C_{in}^2 + 2V_{-1}C_{in}^2\right)$$

- $e = 2.718$, q = electron charge 1.6×10^{-19} C
- τ = shaping time
- $I_0 = 2qI_{leak}$ from detector leackage current
- $V_0 = \frac{8}{3}\frac{kT}{g_m}$ from transistor channel noise
- $V_{-1} = \frac{K_f}{C_{ox}WL}$ from excess flicker (1/f) noise

K_f = $1/f$ noise energy
C_{ox} = oxide capacitance per unit area
W,L = transistor width and length



- Risetime $t_{rise} \propto \frac{1}{g_m}\frac{C_{in}}{C_f}$

- High **input capacitance C_{in}** can be compensated with **transconductance g_m**, at price of power (ALPIDE 24 mW/cm², ATLAS target 500 mW/cm²)

INFN

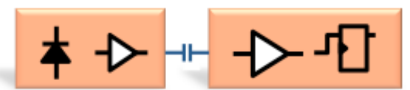
Bologna

Genova

Milano

IIT Mandi

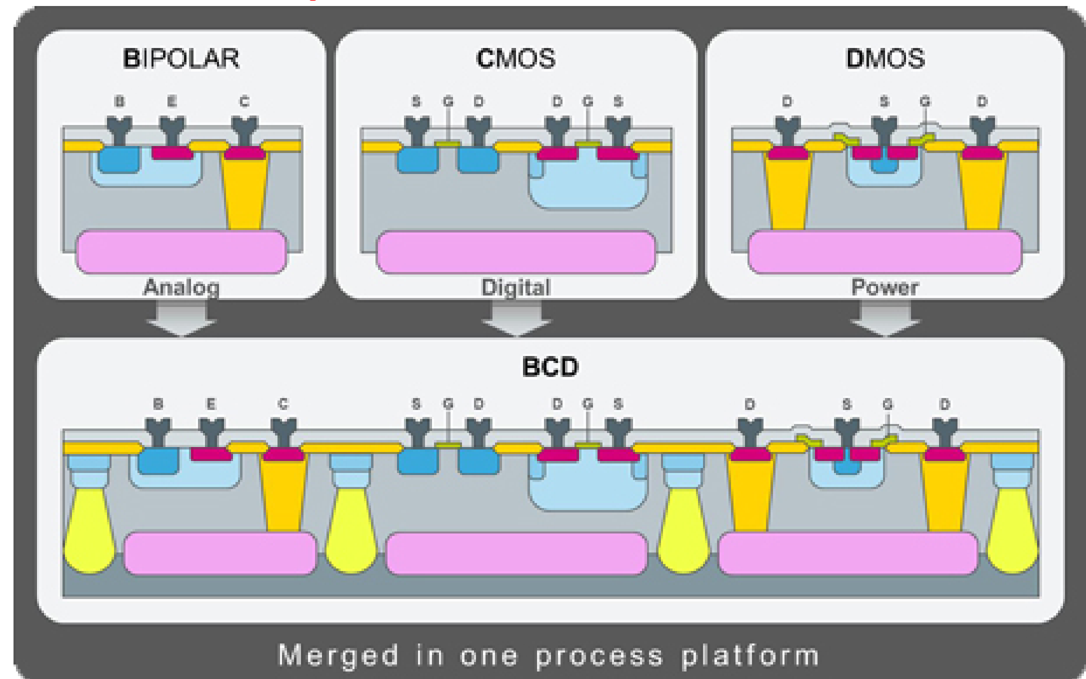
CHARACTERIZATION OF BCD8 PROCESS



Investigation of STMicroelectronics BCD8

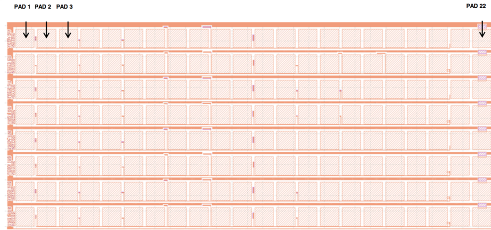
- HV/HR technologies
  - HV CMOS
    - **AMS 350 nm**
    - **AMS 180 nm**
  - HR CMOS
    - **LFoundry 150 nm**
    - Global Foundry 130 nm
    - ESPROS 150 nm
    - Toshiba 130 nm
    - **TowerJazz 180 nm**
    - IBM T3 130 nm
    - STM 180 nm
    - ON Semiconductor 180 nm
- SOI – CMOS Pixel
  - **XFAB 180 nm (Bonn)**

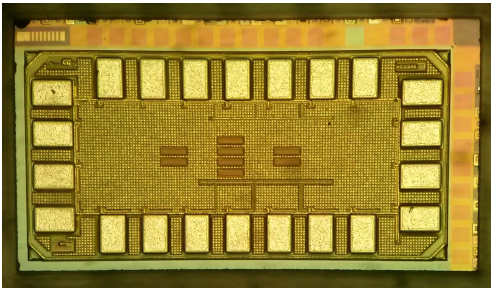
BCD = Bipolar + CMOS + DMOS

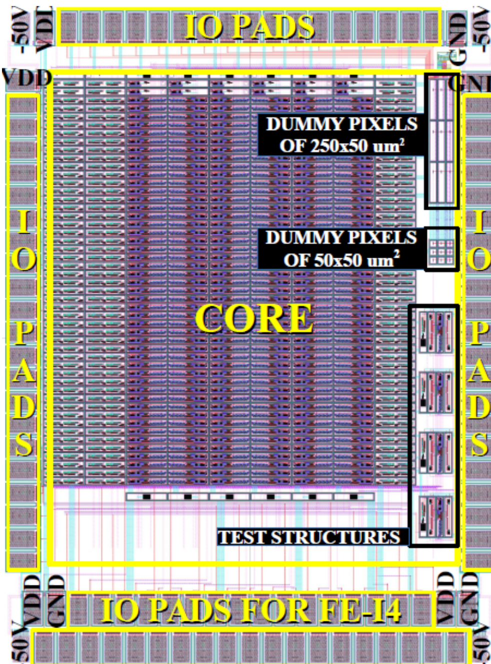


- 180 nm process, optically scaled to **160 nm**
- **epitaxial process**: can grow on different substrates (125 Ω·cm used)
- **rated up to 50 V**: possible to reach depletion layers up to 30 μm
- **long-term availability**: it is one of the major production line for ST automotive products.

STM devices







KC01

- Test chip provided by STMicroelectronics
- Transistor arrays: pmos and nmos, linear and enclosed layouts, sizes 1-10 μm

KC53 (available March 2015)

- IIT Mandi + INFN Milano and Genova:
  - 50×250 μm^2 passive diodes
  - studies of depletion and charge collection

KE15 (available November 2016)

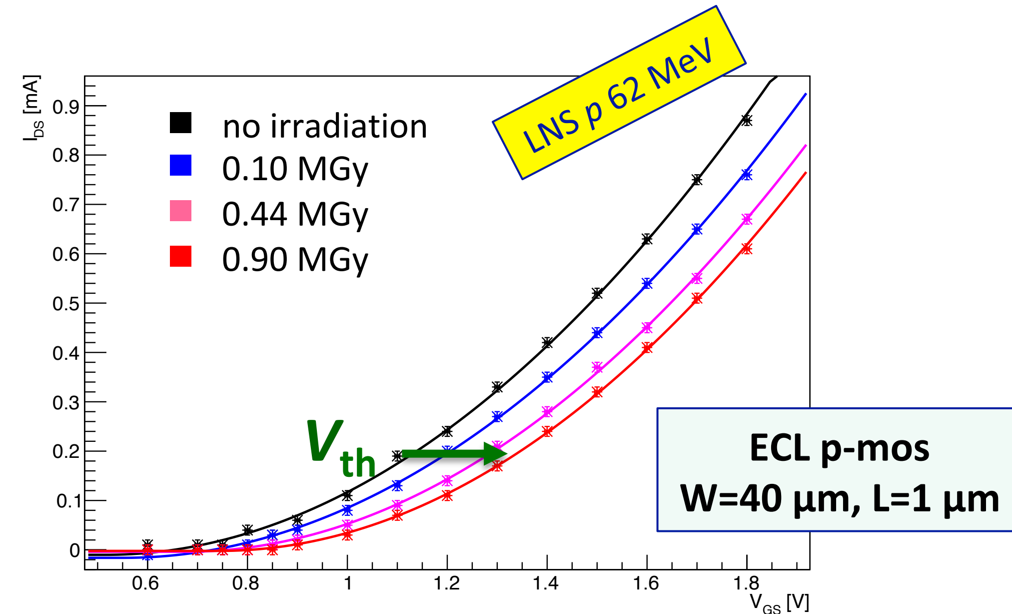
- IIT Mandi + INFN Milano and Genova:
  - 6×48 pixels matrix
  - 50×250 μm^2 pixels, which can be readout after hybridzation with the ATLAS FE-I4 pixel readout chip
  - passive diodes 50×250 μm^2 and 50×50 μm^2
  - amplifier+comparator (tunable by 5-bit DAC)

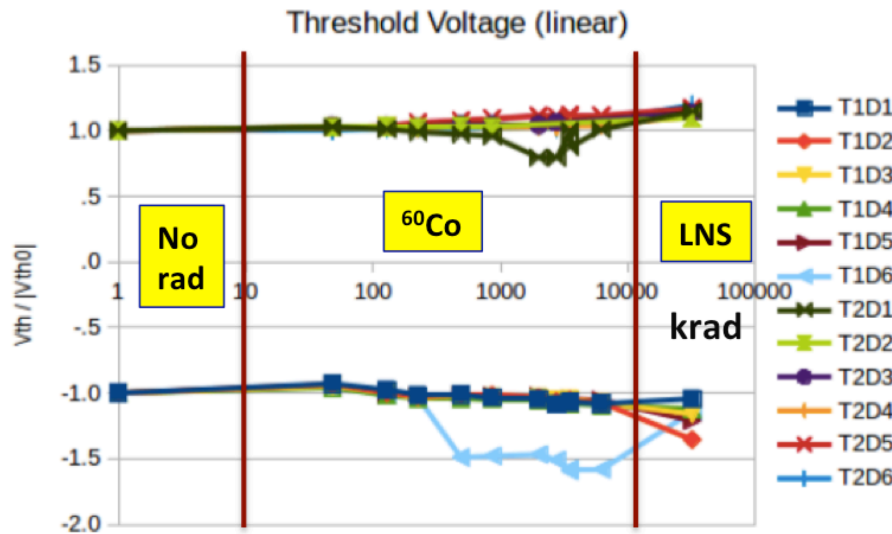
KC01 irradiation results

- Measurement of:
  - transistor threshold, V_{th}
  - transconductance, K

$$I_D = \begin{cases} I_0 & V_{GS} < V_{th} \\ I_0 + K(V_{GS} - V_{th})^2 & V_{GS} > V_{th} \end{cases}$$

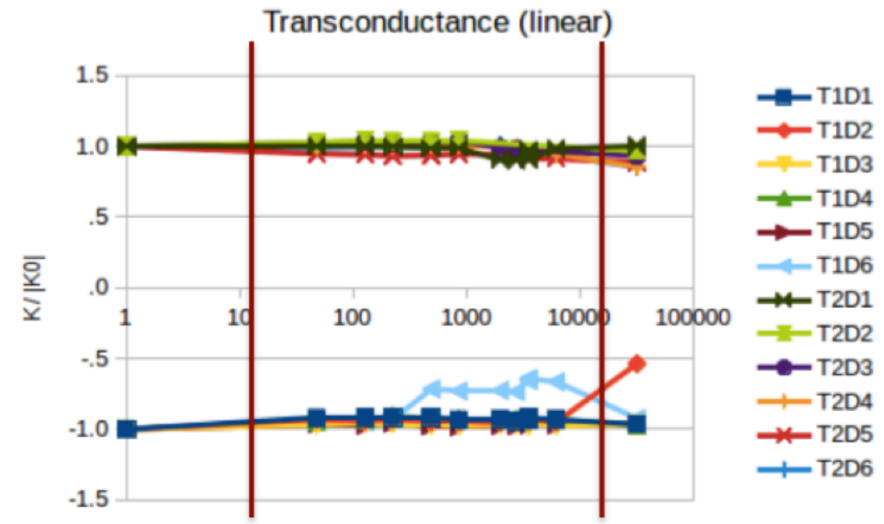
- Overall small effect on n-mos
- Limited 0.2 V V_{th} shift for p-mos
- **No show-stopper for radiation hardness,**





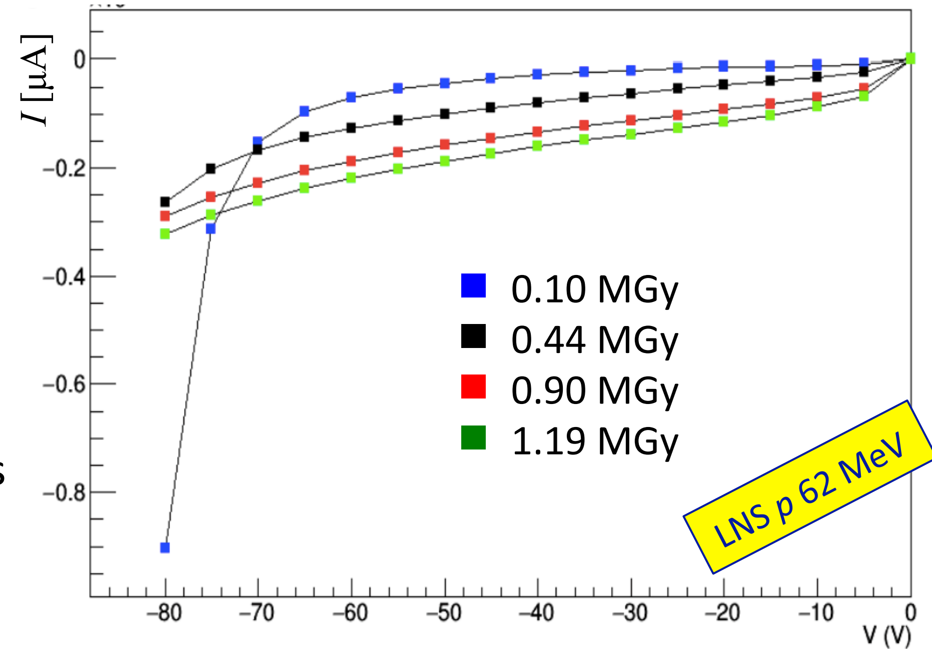
nmos

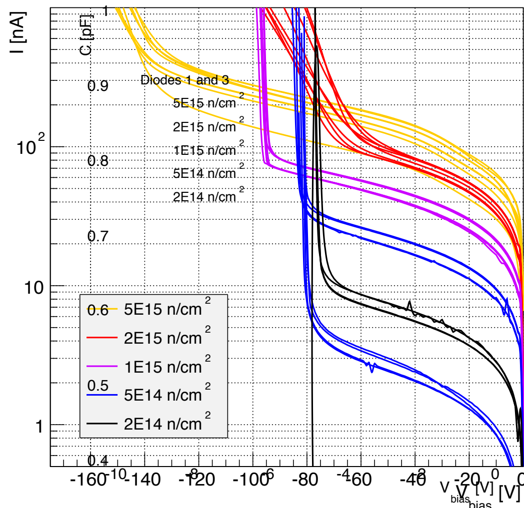
pmos

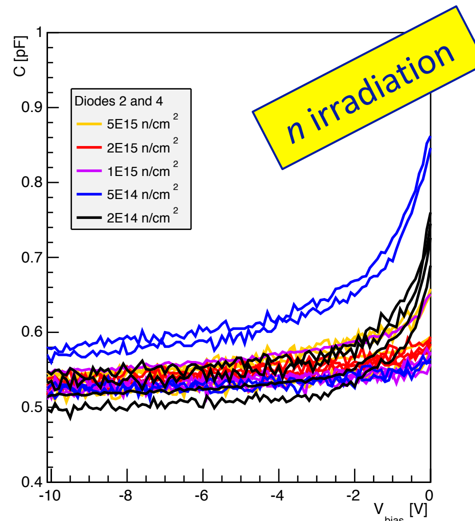


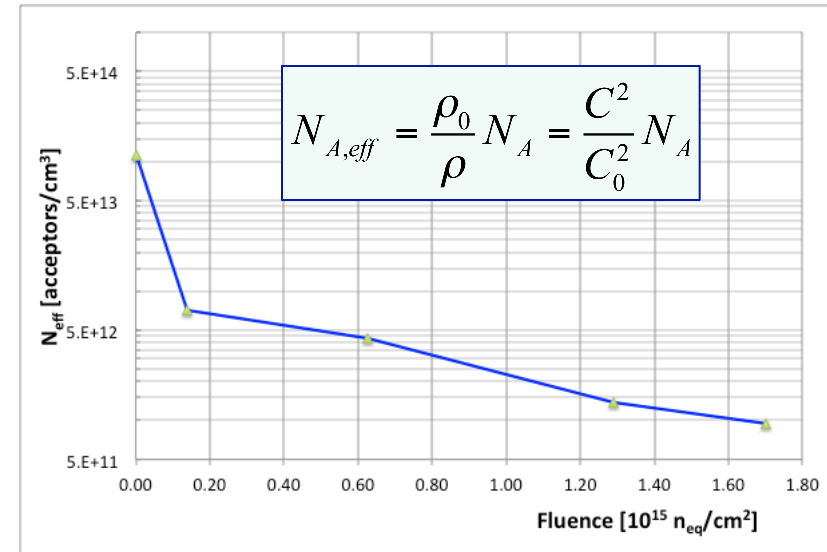
KC53 Characterization

- **I-V measurements**
  - Linear increase of current with fluence
  - Increase of breakdown voltage
- **C-V measurements**
  - Detector capacitance, $C\text{-}C_p \propto 1/\sqrt{\rho} \propto 1/\sqrt{N_A}$
  - Observation of an acceptor removal effect
  - Qualitatively consistent with *n* irradiation results from other groups and p-mos behaviour.
- **Increase of sensitive volume**





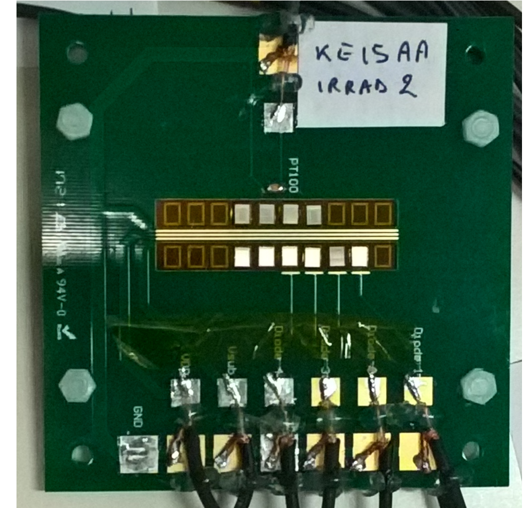


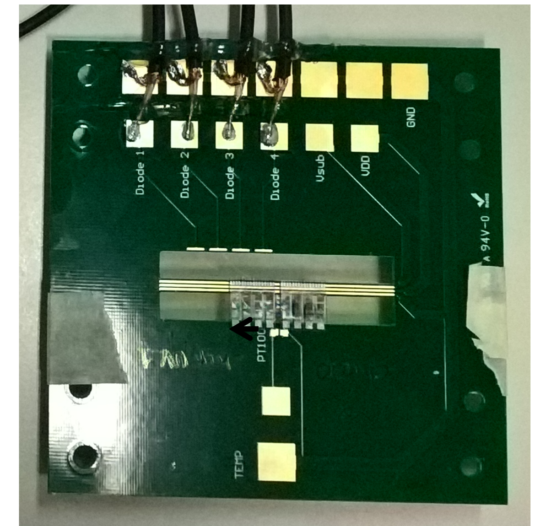


$$N_{A,eff} = \frac{\rho_0}{\rho} N_A = \frac{C^2}{C_0^2} N_A$$

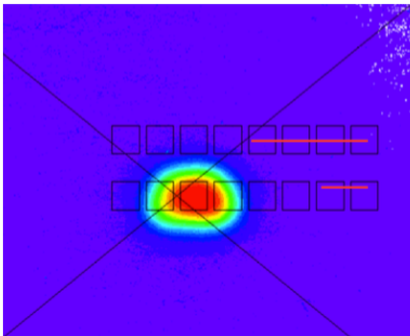
2017 Irradiation at LNS

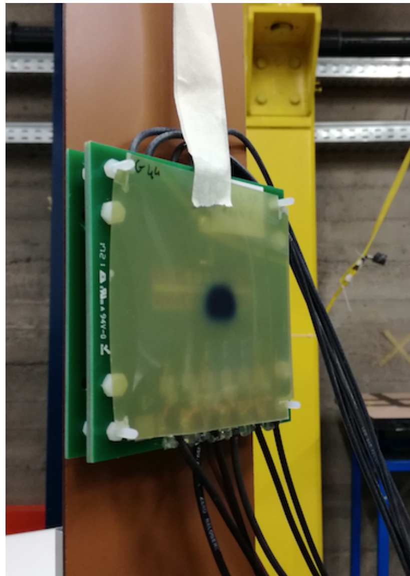
- 62 MeV protons at LNS for more than 12h run (Dec 2017)
  - Narrow Beam (GAF analysis): $\sigma_x \approx 3.3$ mm, $\sigma_y \approx 3.8$ mm
  - Max proton flux (I =35 nA) ≈ 2.8×10^{11} cm^{-2}s^{-1}
- Devices under test:
  - **KE15 chips**
  - **Capacitors** (dielectric properties of hybridization glue)
  - **Waiting for radiation cooldown in a fridge at LNS…**
- **NIEL ≈ 1.8×10^{16} n_{eq}/cm^2**, or **> 11 MGy** at central position
  (other chips ranges from 8×10^{13} to 8×10^{15} n_{eq}/cm^2)

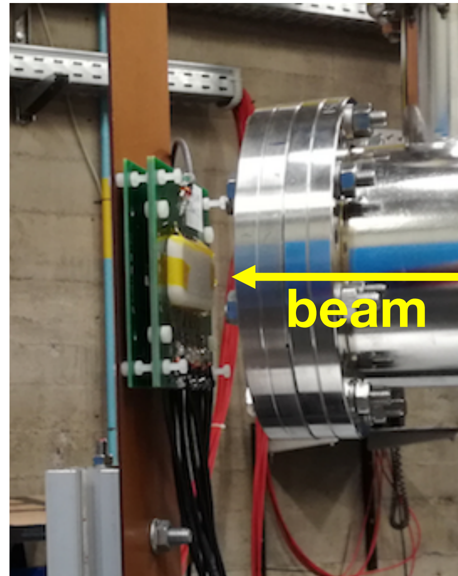




GAF image







KC01 Legend

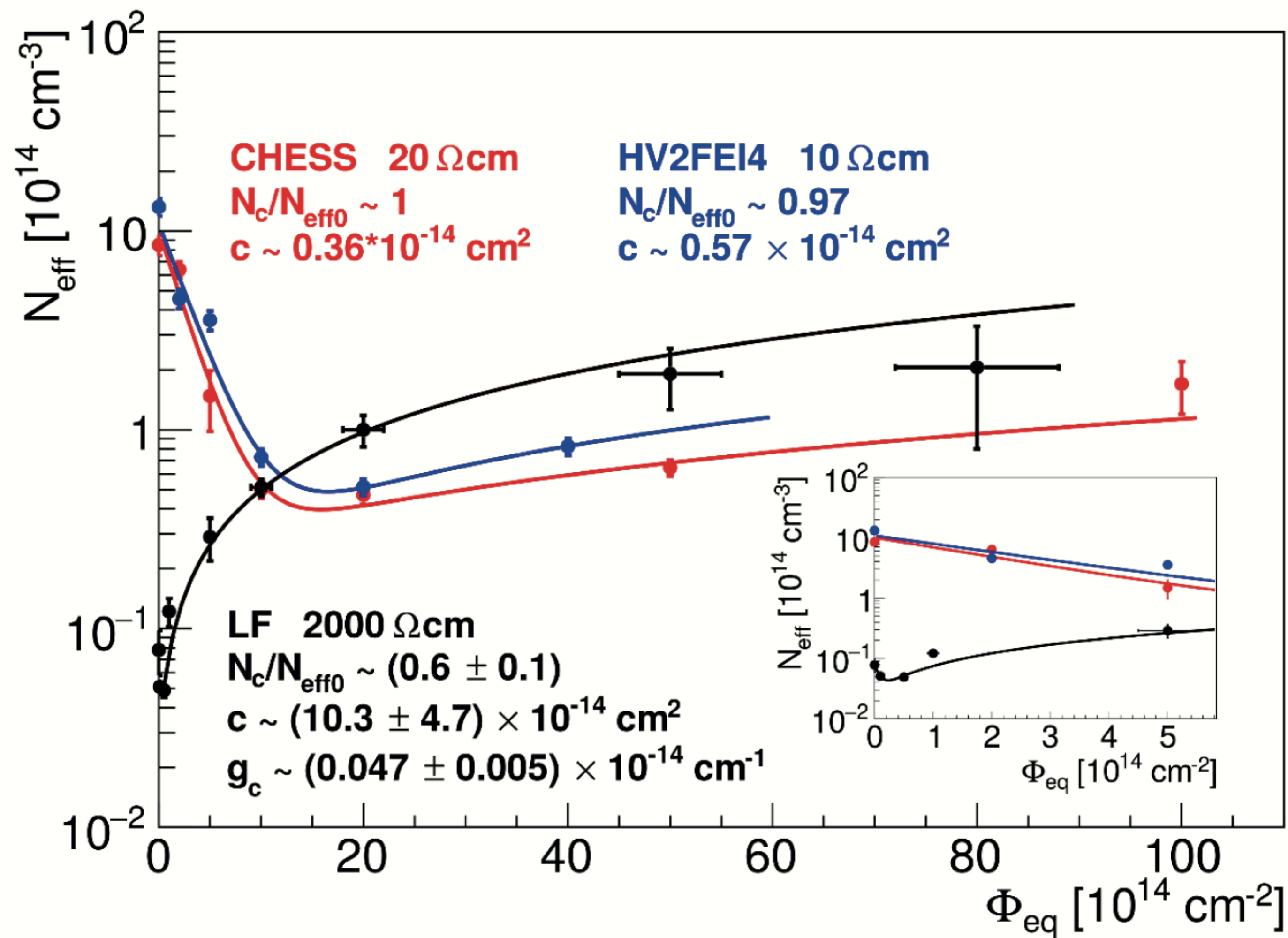
		$Teg1 - 1V8CMOS$		
		W_{EL} (μm)	L (μm)	Notes
T1D1	1V8Pch	10	10	NG=2
T1D2	1V8Pch	10	1	NG=2
T1D3	1V8Pch	20	1	NG=2
T1D4	1V8Pch	40	1	NG=2
T1D5	1V8Pch	100	1	NG=2
T1D6	1V8Pch	100	1	NG=20

		$Teg2 - 1V8CMOS$		
		W_{EL} (μm)	L (μm)	Notes
T2D1	1V8Nch	10	10	NG=2
T2D2	1V8Nch	10	1	NG=2
T2D3	1V8Nch	20	1	NG=2
T2D4	1V8Nch	40	1	NG=2
T2D5	1V8Nch	100	1	NG=2
T2D6	1V8Nch	100	1	NG=20

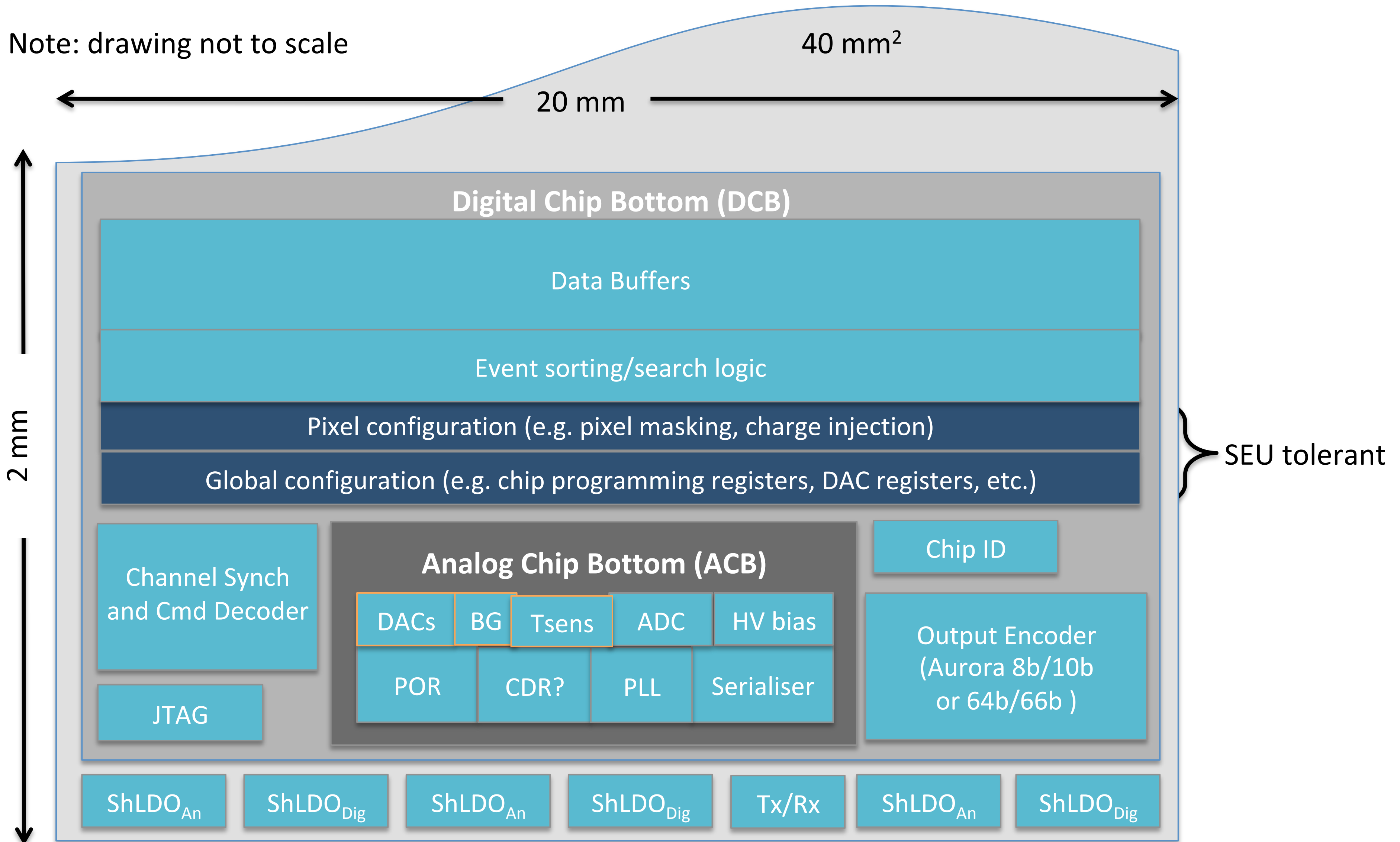
		$Teg3 - 1V8CMOS - Closed$		
		W_{EL} (μm)	L (μm)	Notes
T3D2	1V8Pch	10	1	NG=2
T3D3	1V8Pch	20	1	NG=2
T3D4	1V8Pch	40	1	NG=2
T3D5	1V8Pch	100	1	NG=2
T3D6	1V8Pch	100	1	NG=20

		$Teg4 - 1V8CMOS - Closed$		
		W_{EL} (μm)	L (μm)	Notes
T4D2	1V8Nch	10	1	NG=2
T4D3	1V8Nch	20	1	NG=2
T4D4	1V8Nch	40	1	NG=2
T4D5	1V8Nch	100	1	NG=2
T4D6	1V8Nch	100	1	NG=20

Acceptor removal

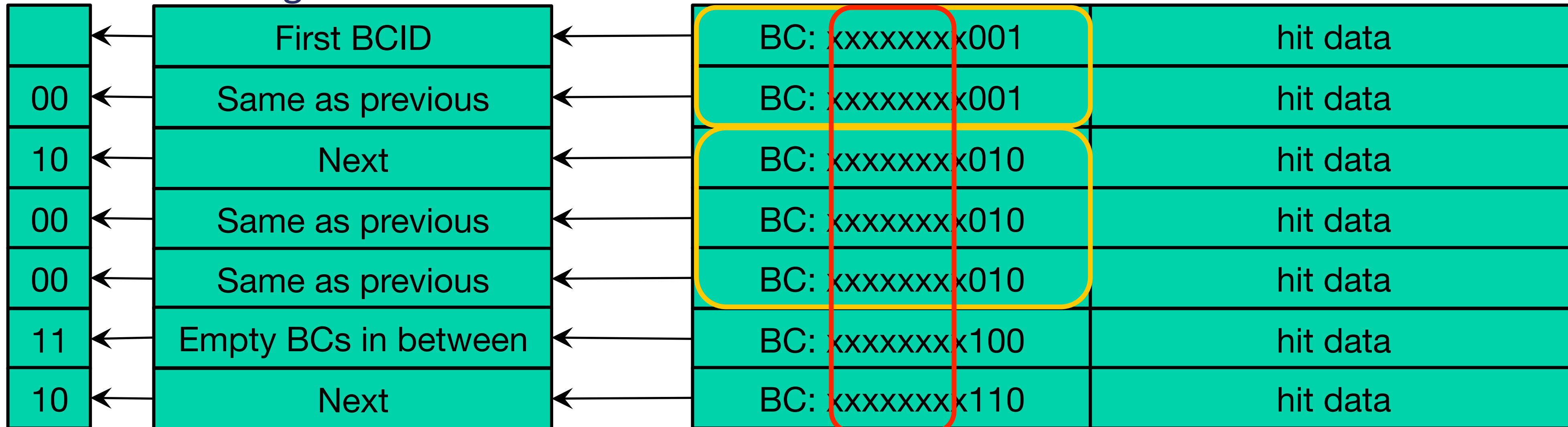


- Depleted region thickness from Transient Current Technique measurements
- Effective acceptor concentration from $d = \sqrt{\frac{\varepsilon_{Si}\varepsilon_0 \left(V + V_{BI}\right)}{eN_{eff}}}$


Note: drawing not to scale
40 mm²
20 mm
2 mm
Digital Chip Bottom (DCB)
Data Buffers
Event sorting/search logic
Pixel configuration (e.g. pixel masking, charge injection)
Global configuration (e.g. chip programming registers, DAC registers, etc.)
SEU tolerant
Channel Synch and Cmd Decoder
JTAG
Analog Chip Bottom (ACB)
DACs
BG
Tsens
ADC
HV bias
POR
CDR?
PLL
Serialiser
Chip ID
Output Encoder (Aurora 8b/10b or 64b/66b)
ShLDO An
ShLDO Dig
ShLDO An
ShLDO Dig
Tx/Rx
ShLDO An
ShLDO Dig

Bunch crossing ID compression

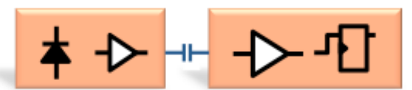
- Instead of storing the full Bunch Crossing ID for each hit we may exploit the fact that the data are stored in the memory in chronological order
- It is possible to write only a flag to state if:
  - The hit belongs to the same BC as the previous
  - The hit belongs to the following BC
  - There is one or more bunch crossing without hits in between (in this case the bunch crossing ID for the following data is stored in the hit position)
- As there are three cases we can encode them with 2 bits
- This is useful considering that (on average) there are lots of hits for each bunch crossing



INFN

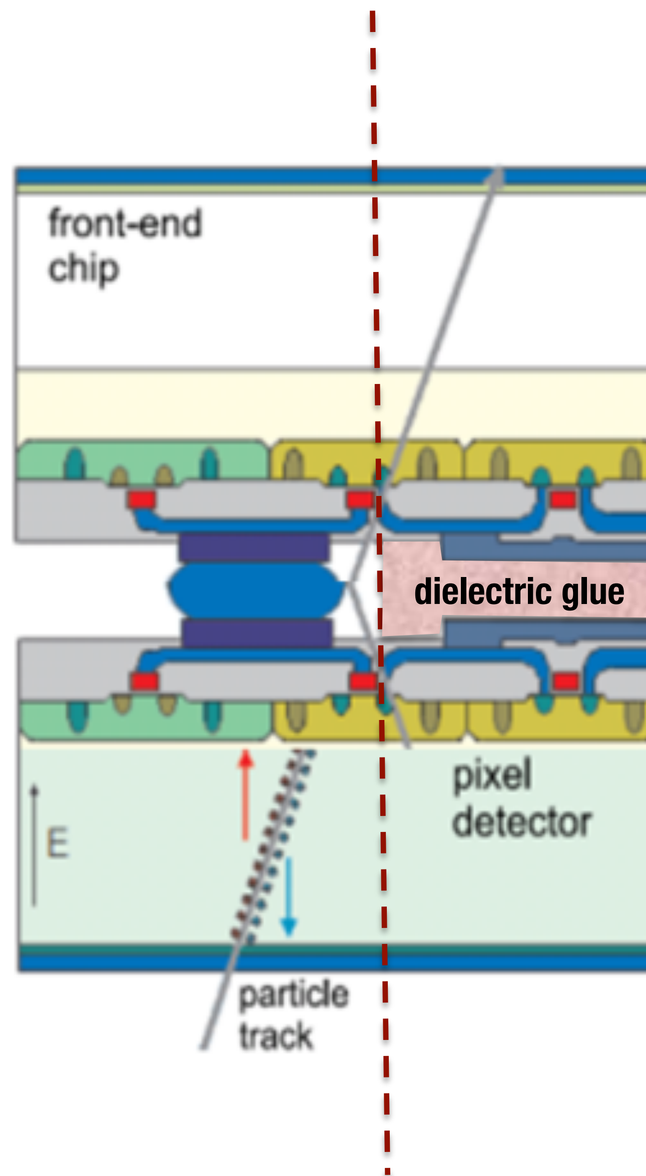
Genova

CAPACITIVE COUPLING

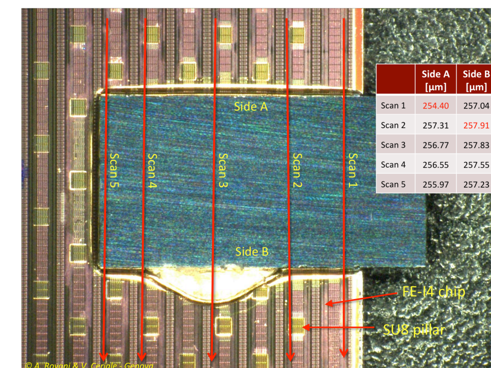


Capacitive Coupling

- Connection of passive sensors to a front-end chip by bump-bonding is a mature technology.
- The interconnection cost is significant fraction of the total detector cost
  - similar to sensitive part
- Challenges for HL-LHC detectors:
  - ×5 bump density
  - thin detector and chips (planarity)



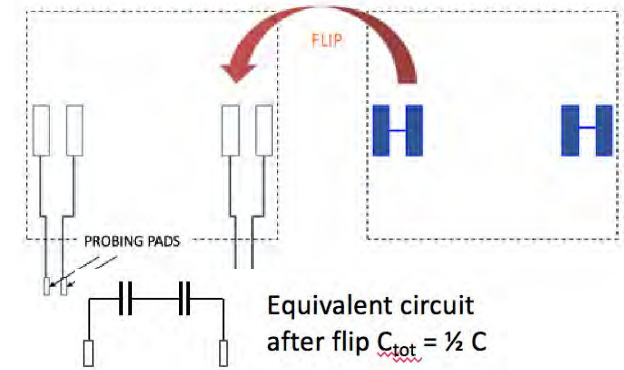
- Exploit local amplification integrated in front-end
  - or broadcast digital signal
- via capacitive coupling
  - dielectric glue layer
  - provides both mechanical and electrical coupling.
  - **simpler and faster process**
- **Separate functionalities** of **smart sensor** and readout chip:
  - may exploit best available technologies on each side



	Side A [μm]	Side B [μm]
Scan 1	254.40	257.04
Scan 2	257.31	257.91
Scan 3	256.77	257.83
Scan 4	256.55	257.55
Scan 5	255.97	257.23

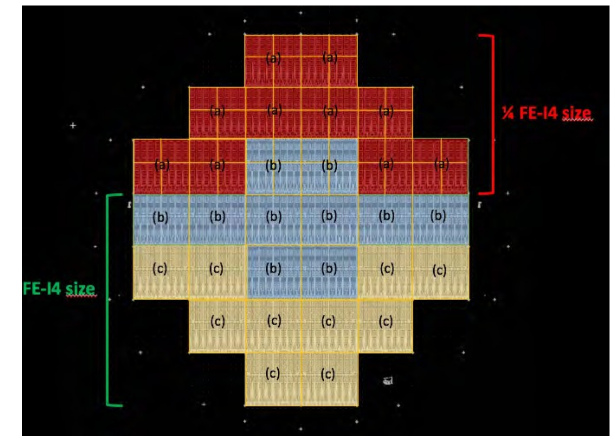
Introduction

The idea is to use pillars to control the distance between dies and its uniformity



Bonding quality tested by matrix of capacitors

⇒ Bonding parameters can be optimized to achieve the wanted coupling distance and uniformity.

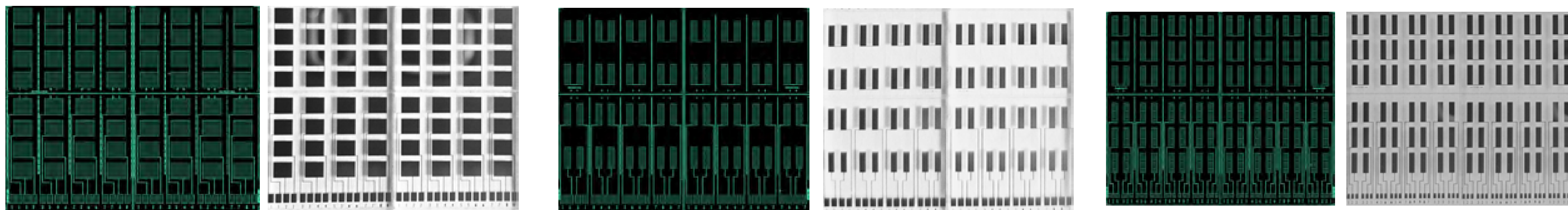


A batch of 4 6" wafers have been commissioned to *MicroFab Solutions* (Trento) choosing fused quartz (electrical resistivity of > $10^{18}\ \Omega \cdot m$**) as deposition substrate.**

Different depositions options:

- One wafer w/o pillars
- 3 wafers with 3, 5 (x2) µm thick pillars respectively.
  - The pillars by Microchem KPMR, high contrast, epoxy based photoresist

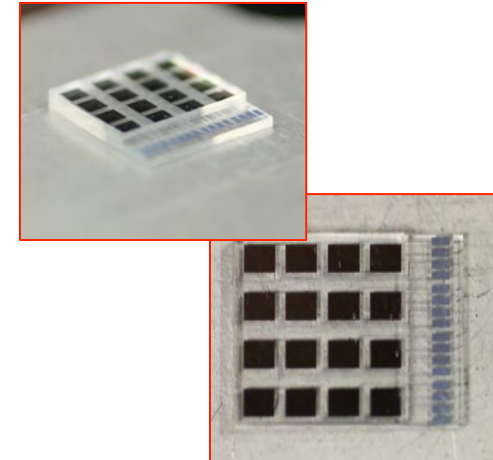
Two different plate area designs: 1.5×1.5 and 0.5 × 1.5 mm² and density.



Capacitive tiles

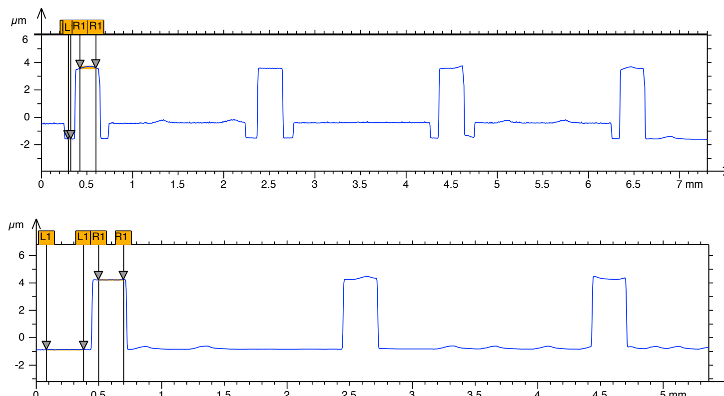
Tiles assembled:

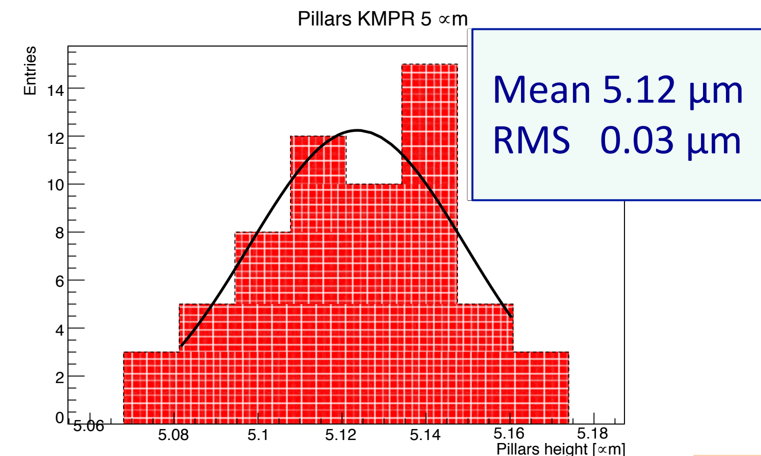
- 3 different glues used: Araldite 2011, 2020 and Masterbond
    - **Masterbond** UV15DC80LV is a dual cure epoxy based system which offers a primary cure utilizing UV light (365 nm) along with a secondary heat curing mechanism (80 C)
- Assemblies and test with and w/o pillars have been performed in Genova (1x1 cm^2 tiles) and together with Université de Genéve and CERN (2x2 cm^2 tiles) during last months.



Before Assembly:

- Visual inspection of the electrical lines
- Height and uniformity 3/5 µm pillars/surface wafers checks (using Profilometer)

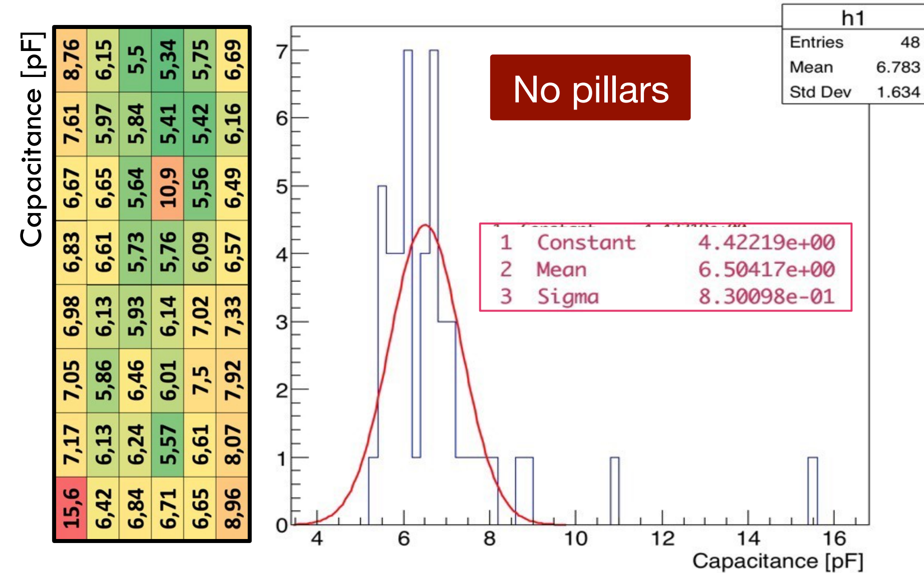


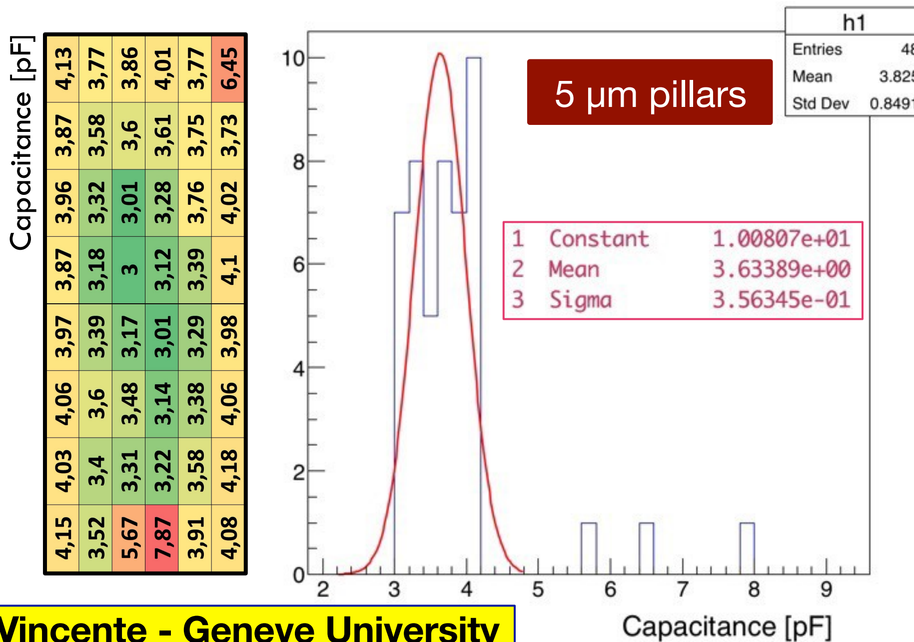


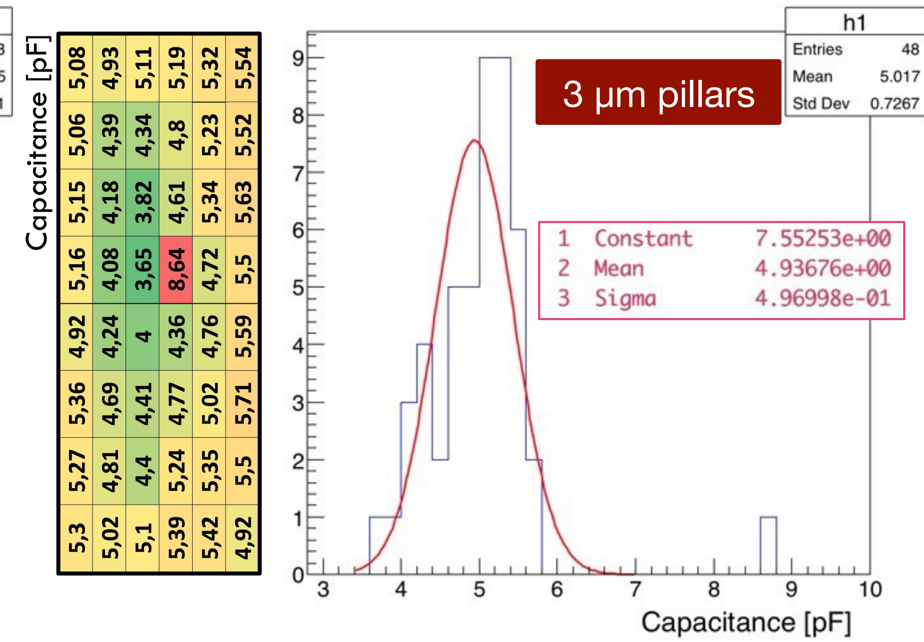
AC coupled tiles

Capacitance measurements

- Uniform capacitance
- Radial gradient: larger gap in the center of the assembly
- With no pillars: σ = 83 fF
- Smaller σ in samples with pillars
  ⇒ **improved parallelism**





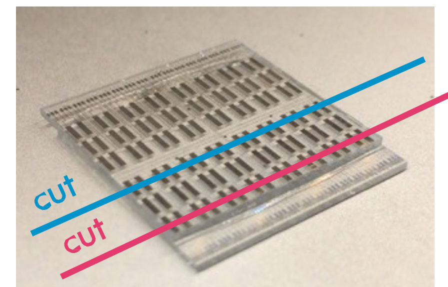


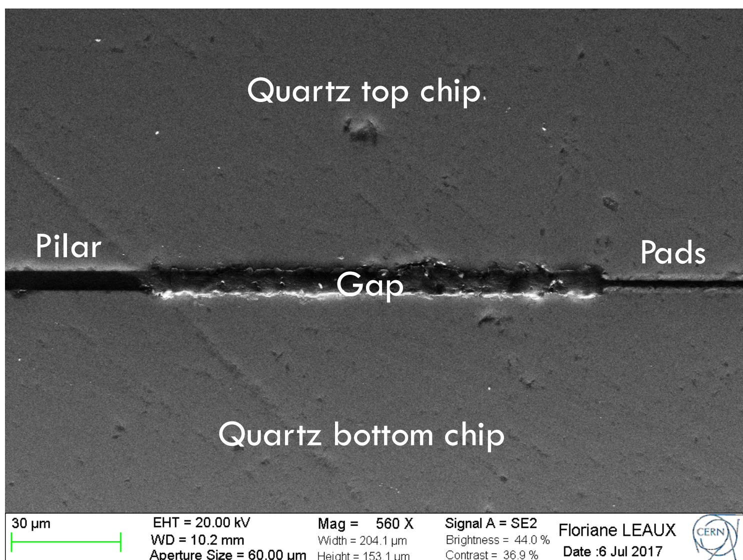
Credits: M.Vincente - Geneve University

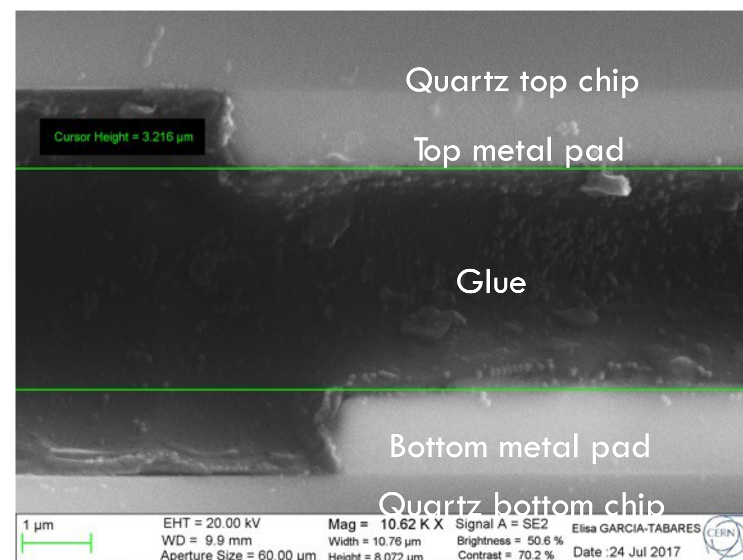
Scanning Electron Microscopy

SEM measurement with CERN EN-MME-MM

- Sample embedded in resin
- Cross-section cut passing through all capacitor columns
- SEM pictures done at CERN







Credits: M.Vincente - Geneve University

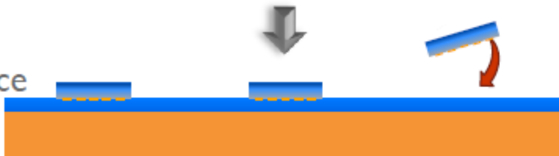
Results and steps towards industrialization

- Considering the uncertainties on metal pads height and on the relative permittivity value of the glue, the extrapolated heights from the capacitance look in good agreement with direct measurements by electron microscopy within 0.5 μm
- The capacitive tiles have proven to be a good method to measure the height between the die and check the flip-chip machine head alignment
  - Using Geneva flip-chip machine (Accμra 100) the pillars give an improvement of about ~20% on the height dispersion, increasing the parallelism of the tiles.
  - This technique can be useful to improve parallelism if needed
- Plan to summarize all the measurements in a paper.
- Industrialization of the process:
  - CMOS lines are typically 12”, but MEMS lines (e.g. to pillars deposition) are below 8” … how to match this two worlds?
  - .. a possible solution came from Wafer Packaging technique (next slides)

Wafer Level Packaging

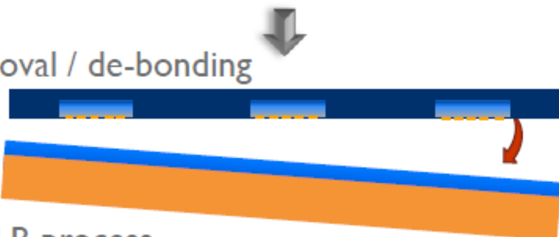
Tape lamination

Pick and place

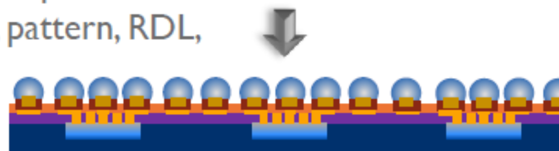


Wafer level Molding

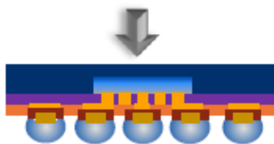
Carrier removal / de-bonding



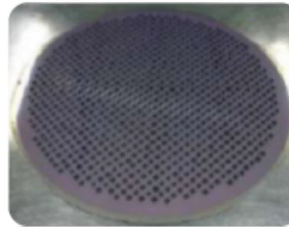
Standard WLB process (Passivation, pattern, RDL, bonding)



Dicing



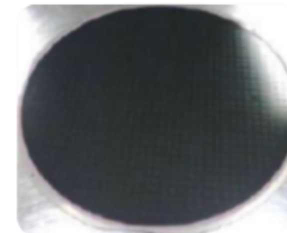
Carrier with foil and chips

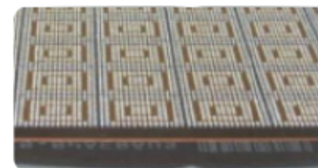


Carrier (Metal)

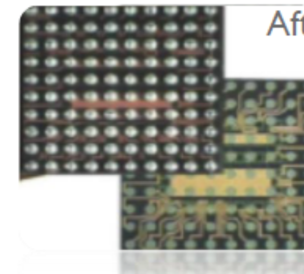
Molding with liquid moldcompound

Reconstituted wafer after molding





WLP Fan-Out wafer

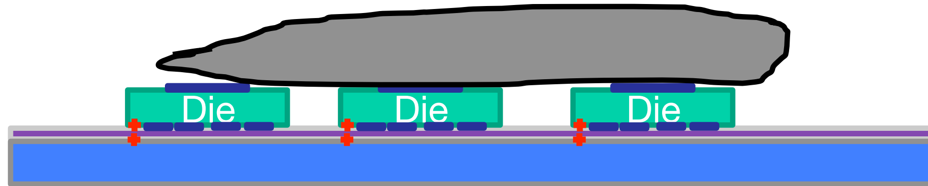


After singulation

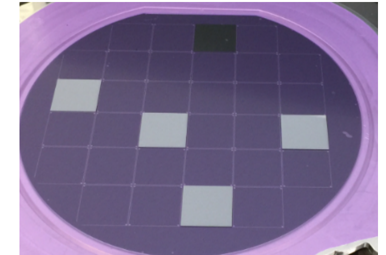
Wafer Level Packaging at MFS

Started a collaboration with MicroFabSolutions (Trento)

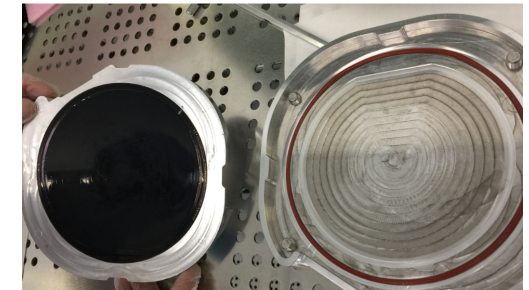
- 6 silicon wafers 300 µm thick for Dummy Chip 20x20 mm^2 + 3 reusable support wafers
- Designed and fabricated mould for WLP Compression moulding



Chips placement and epoxy deposition opposite to Foaming Layer side

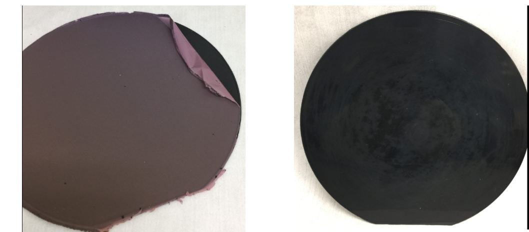


Curing T=130 C 10 min



Foaming T=190 C 1 min

Peeling T=20 C



- Best results with Panasonic resin
- Next: **systematic studies of resin thickness vs wafer mechanical properties**