ARCADIA

Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays

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INFN - Sezione Torino

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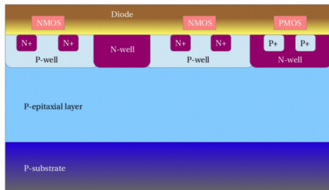
Monolithic sensors



Monolithic technology

- Sensor and readout electronics are built in the same silicon wafer
- Low material budget
- Low cost because only one fabrication process is needed

Partially depleted

- The sensing region extends for few tens of um
- The charge collection is performed mainly by **diffusion**
- Collection time > 10 ns
- Competitive charge collection → **low efficiency**
- Maximum radiation tolerance ~10^{13} neq/cm^2
- Low SNR

Fully depleted

- The charge collection is performed mainly by **drift**
- **Fast charge collection** (<10 ns)
- CMOS circuitry can be implemented
- **Competitive charge collection is avoided → good efficiency**
- High radiation tolerance
- Good SNR

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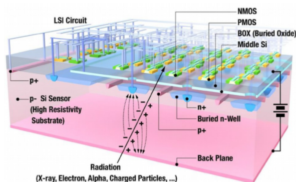
Some possible solutions



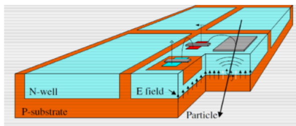
Y. Arai, IEEE IEDM 2017

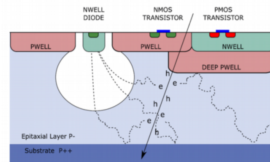
FD SOI

- Buried oxide used to separate the sensor from the electronics
- High resistivity substrate
- Buried oxide →gate effect →2 buried oxide layers used
- Radiation tolerance up to 10Mrad

HV-CMOS

- High resistivity p-substrate (>2kΩ cm)
- The collector node is a deep nwell
- High voltages can be applied
- Fast charge collection
- High efficiency
- CMOS electronics built in the sensing node → high sensor capacitance → high noise





J.P. Crooks, et al., IEEE TNS 2007

ALPIDE

- High resistivity p-substrate (> 1kΩ cm) + epitaxial layer
- Partial depletion
- Sensing node shielded by a deep pwell
- Small sensor capacitance
- Radiation tolerance (TID) up to 700 krad

SEED Project

- **SEED : Sensor with Embedded Electronics Development**
- Goal: fully depleted monolithic pixel sensor
- Good timing resolution O(ns)
- Integrated CMOS pixel electronics
- Process development with an industrial partner: **LFoundry**
- INFN Divisions: Torino, Padova, Trento, Frascati, Perugia
- INFN-LFoundry patent pending

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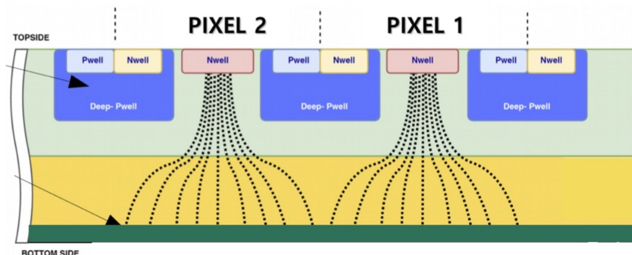
SEED: Proposed monolithic sensor

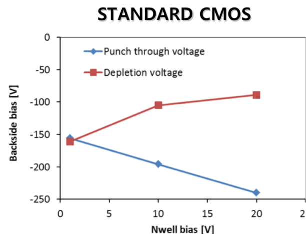


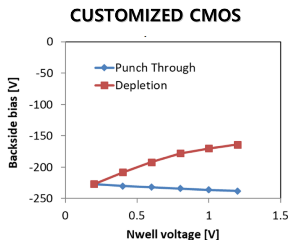
- Goal: full depletion in 100-500 um. The present prototype is 300 um.
- Technology: 110 nm CMOS technology, high-resistivity bulk
- Custom backside process developed (collab. industrial partner)
- The depletion starts from the backside
- At the backside, the main diode is surrounded by a guard-ring
- Both NMOS and PMOS transistors
- The pixel capacitance is kept low $\approx$ 20 fF

Sensor bias

Ingredients for reliability

- The bias voltage high enough to reach the **full depletion** avoiding an early **punch through**
- The difference between the punch through voltage and the full depletion voltage must be maximized. This allows to increase the electrical field and thus to get a much faster charge collection.

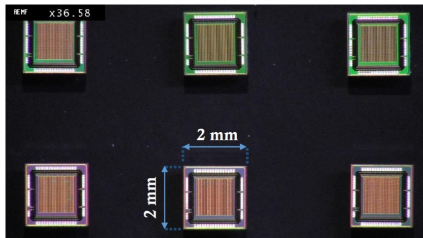




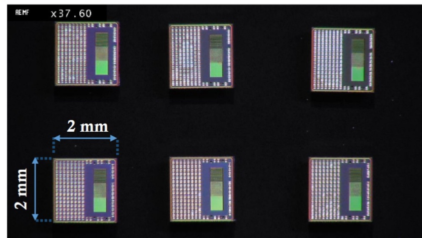
- The **maximum n-well** voltage allowed: 1.2 V
- The use of a **n-epi layer allows to increase the punch though voltage** allowing the full depletion also with low voltage CMOS process.

First silicon prototyping

Complete monolithic sensor



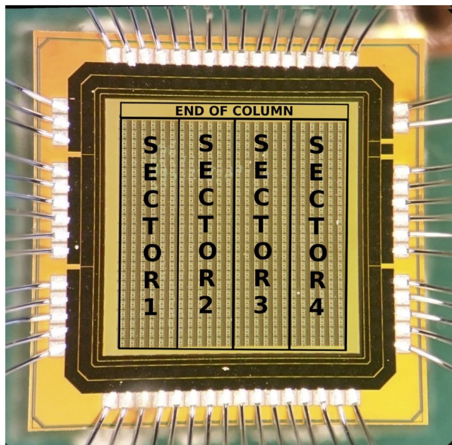
Test chip



Technology	110 nm double side CMOS technology
Metal layers	6
Size	2 X 2 mm^2

- Wafers with small different epitaxial layer thickness have been used for the production

The MATISSE Demonstrator



- MATISSE is a full monolithic sensor with embedded electronics on board.
- The electronics built on the top side is compatible with a standard CMOS process fabrication flow
- matrix of 24 x 24 pixels organised in 4 columns
- Each pixel implements an analog readout in global shutter
- 2x2 mm^2 die, VDD=1.2V

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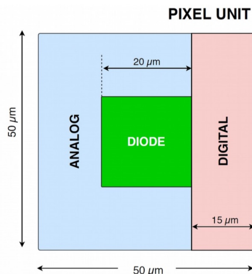
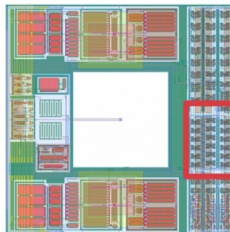
MATISSE Pixel Architecture





Large digital buffer

ANALOG

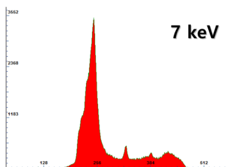
- Amplification stage
- Two memories
- Two buffers to drive the transmission bus
- Test pulse injection system
- Baseline regulation system

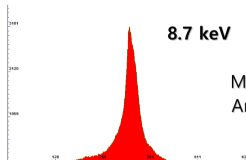
DIGITAL

- Logic for masking
- Registers for local programming
- Large digital buffer to test the digital noise injection from digital circuits

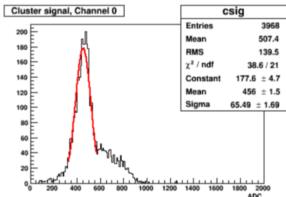
MATISSE Characterisation: X-Ray

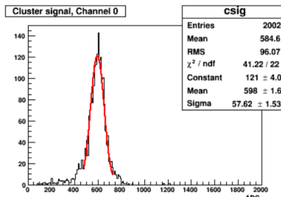
- Calibration made by means of the facility for total dose RP-149 Semiconductor Irradiation System.
- A monochromator has been used to get a monochrome spectrum.
- Two different energies selected: 7 KeV and 8.7 KeV.





Measured with the Amptek XR-100CR



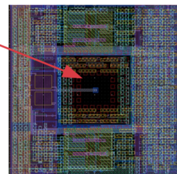


Measured with MATISSE

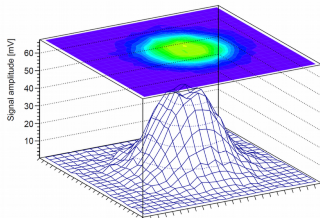
MATISSE Characterisation: Laser measurements

- The metal fillers of the channel has been designed so that left free the pixel centre for optical measurements.
- A laser of with a **wavelength 1060 nm** has been used for the measurements
- The laser spot has been focused up to reach a diameter 8 um
- Laser sent to 16 pixels in the matrix

Low metal density

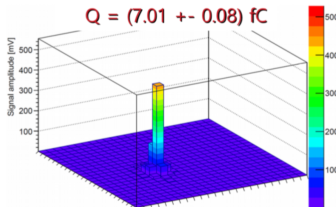


Non focused pulse



Focused pulse

Q = (7.01 +- 0.08) fC



Outlook for developments with SEED Technology

- First production: 300 um **fully depleted thick monolithic CMOS sensor** developed and tested with excellent results
- good process for X-ray imaging (backside optimisation)
- lower thickness envisaged for particle trackers
- limited device portfolio with current LF11IS PDK

- Future steps:
  - Processing of thinner substrates (down to 100 μm)
  - qualification of low-Vth FET devices
  - Dedicated laser measurements to study the charge collection
  - Studies of radiation damage with neutrons

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◇ **ARCADIA : Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays**

- INFN CSNV Call Project: budget $\approx 1 MEur$
- INFN Divisions: Bologna, Milano, Padova, Pavia, Perugia, Torino, TIFPA , $\approx$ 14 FTE
- Evaluation results by September 2018 $\rightarrow$ kick-off January 2019
- Project duration: 3 years

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ARCADIA: roadmap and deliverables

ARCADIA will target the development of a novel CMOS sensor platform allowing for:

- Active sensor thickness in the range 50 um to 500 um or more;
- Operation in full depletion with fast charge collection only by drift;
- Small charge collecting electrode for optimal signal-to-noise ratio;
- Scalable readout architecture with ultra-low power capability (O(10 mW/cm2));
- Easy compatibility with standard CMOS fabrication processes.
- Deliverable: full-size system-ready demonstrator of a low-power high-density pixel matrix CMOS monolithic sensor

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ARCADIA: organisation

- **WP1** - **CMOS Sensors**
  - TIFPA, PG, MI
- **WP2** - **Mixed-signal IP Block design and Chip integration**
  - BO, PV, PG, TO
- **WP3** - **Data Acquisition**
  - BO, TO
- **WP4** - **Application and system characterisation**
  - MI, PD, TIFPA
- **WP5** - **Radiation-hardness**
  - PD, PV

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ARCADIA platform

INFN Sez. Bologna, Milano, Padova, Perugia, Pavia, TIFPA, Torino

A. Gabrielli, D. Falchieri, G. D'Amen, F. Alfonsi, N. Giangiacomi, A. Cervelli, A. Andreazza, M. Caccia, R. Santoro, A. De Angelis, P. Giubilato, J. Wyss, A. Candelori, R. Rando, D. Bastieri, G. Ambrosi, P. Placidi, D. Passeri, L. Servoli, A. Scorzoni, G. Traversi, L. Ratti, C. Vacchi, L. Gaioni, S. Noli, L. Pancheri, G.-F. Dalla Betta, A. Ficorella, M. Zarghami, M. Favaro, R. Iuppa, P. Zuccon, F. Nozzoli, B. Di Ruzza, E. Ricci, M. Rolo, R. Giampaolo, A. Rivetti, S. Cometti, S. Beole', R. Wheadon, F. Tosello, N. Demaria, A. Di Salvo