Fabrication of Graphene sensors for HEP applications

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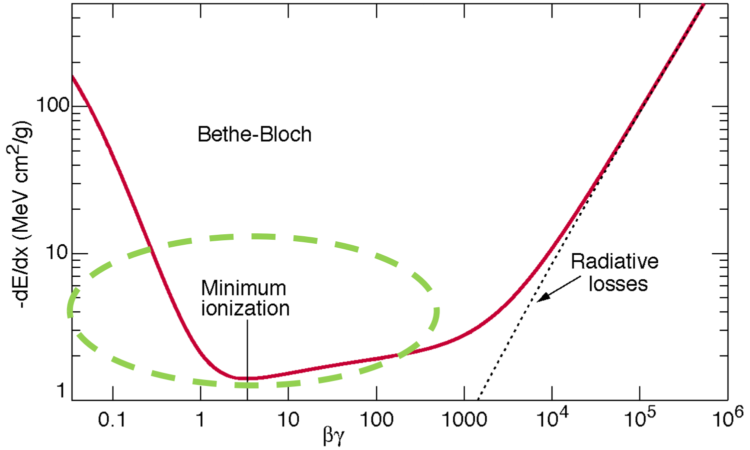
National Enterprise for nanoScience and nanoTechnology

Outline

- Detector key concept
- How we realized it
- Design: in collaboration with FBK
- Fabrication of the Si-absorber @FBK
- Graphene transfer and device fabrication @NEST

Detector key concept - 1

- Particle lose energy in semiconductor
- e-h pairs generation
- Carriers collected by E field
- Electrical signal (Ramo theorem)



In practical cases, most relativistic particles (e.g., cosmic-rays, muons) have mean energy loss rates close to the minimum, and are said to be MIPs.

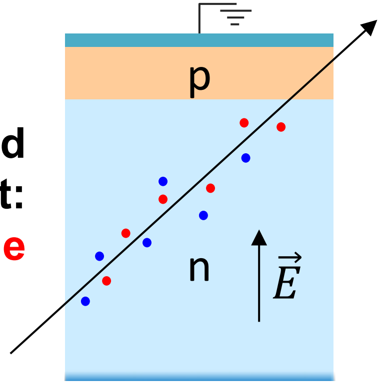
$$\langle N_{eh} \rangle = \frac{E_P}{w}$$

MIP in Si wafer

$$\left.\begin{aligned} \text{Silicon:} \quad w &= 3.6\text{eV} \\ &\sim 80\ e^-/\mu\text{m} \end{aligned}\right\} \ \mathbf{3.8\ fC}\ \text{in } 300\ \mu\text{m}$$

Sensor Architecture

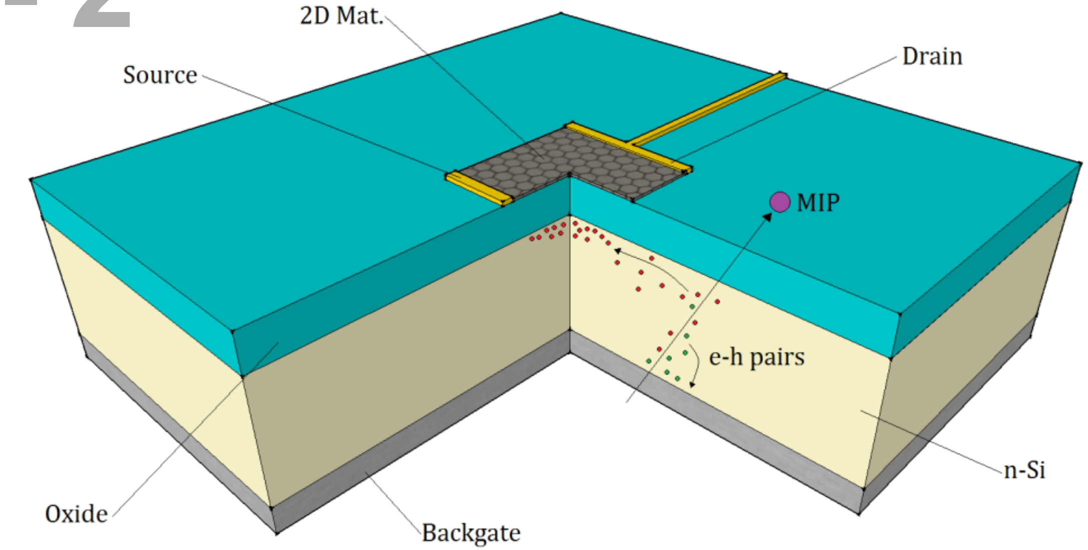
To have strong field and suppress leakage current: reverse biased diode



Detector key concept - 2

G-FET on Si/SiO_2 substrate

- Ionization charges in Si
- Induced field on FET channel (2D mat.)
- Fermi energy shift
- Conductivity modulation



- 2D-mat. **not** interacting with radiation
- **Signal**: output current modulation
- Hybrid system: Si bulk + 2D sensor

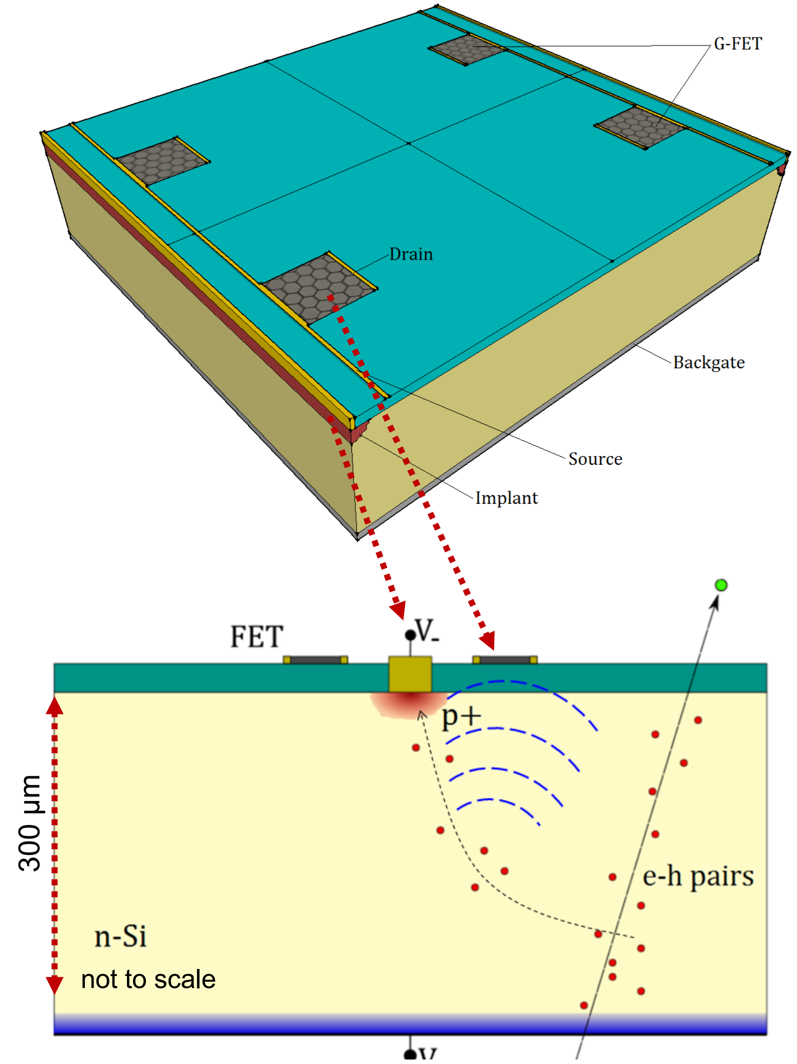
Possible advantages:

- Built-in amplification
- High SNR
- Simple fabrication

Built-in preamp: similar to monolithic design,
but…**Much simpler** construction!

How we realized it

- Optimal device design obtained from simulations – INFN, UniPisa
- Use of the well-established fabrication methods to realize the Si-based absorber – FBK (Fondazione Bruno Kessler, Trento)
- Graphene synthesis, manipulation and devices fabrication – NEST, Pisa
- Detector performances– INFN, UniPisa



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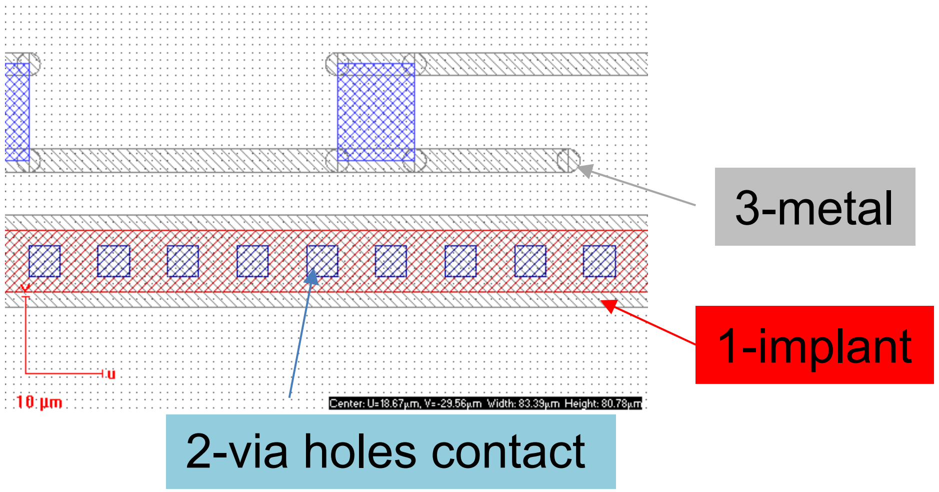
Fabrication steps

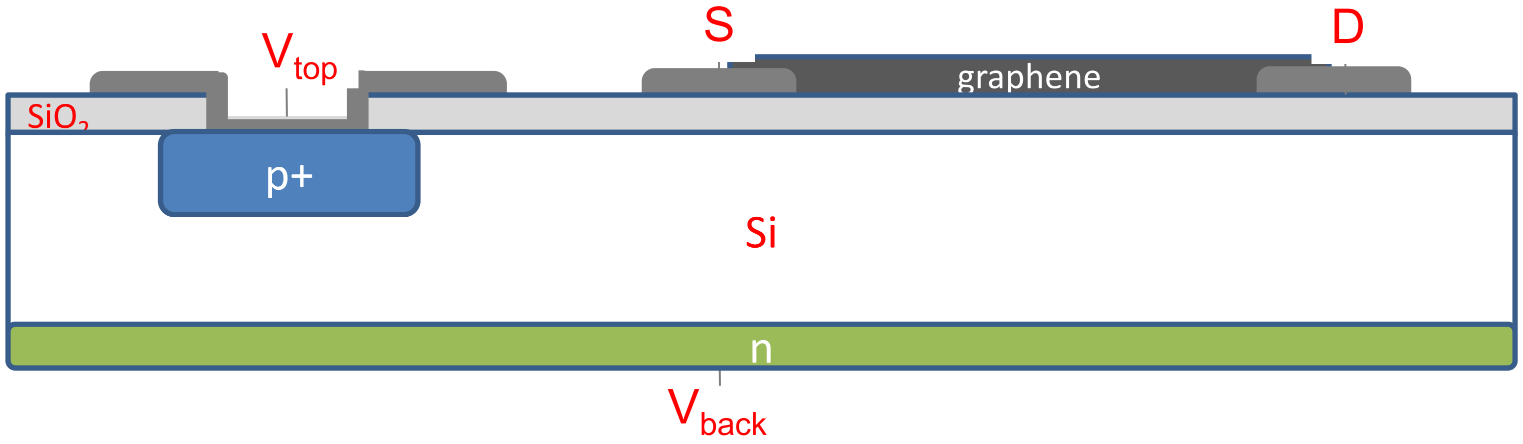


Si-absorber Fabrication@FBK
(3-layers of litho)

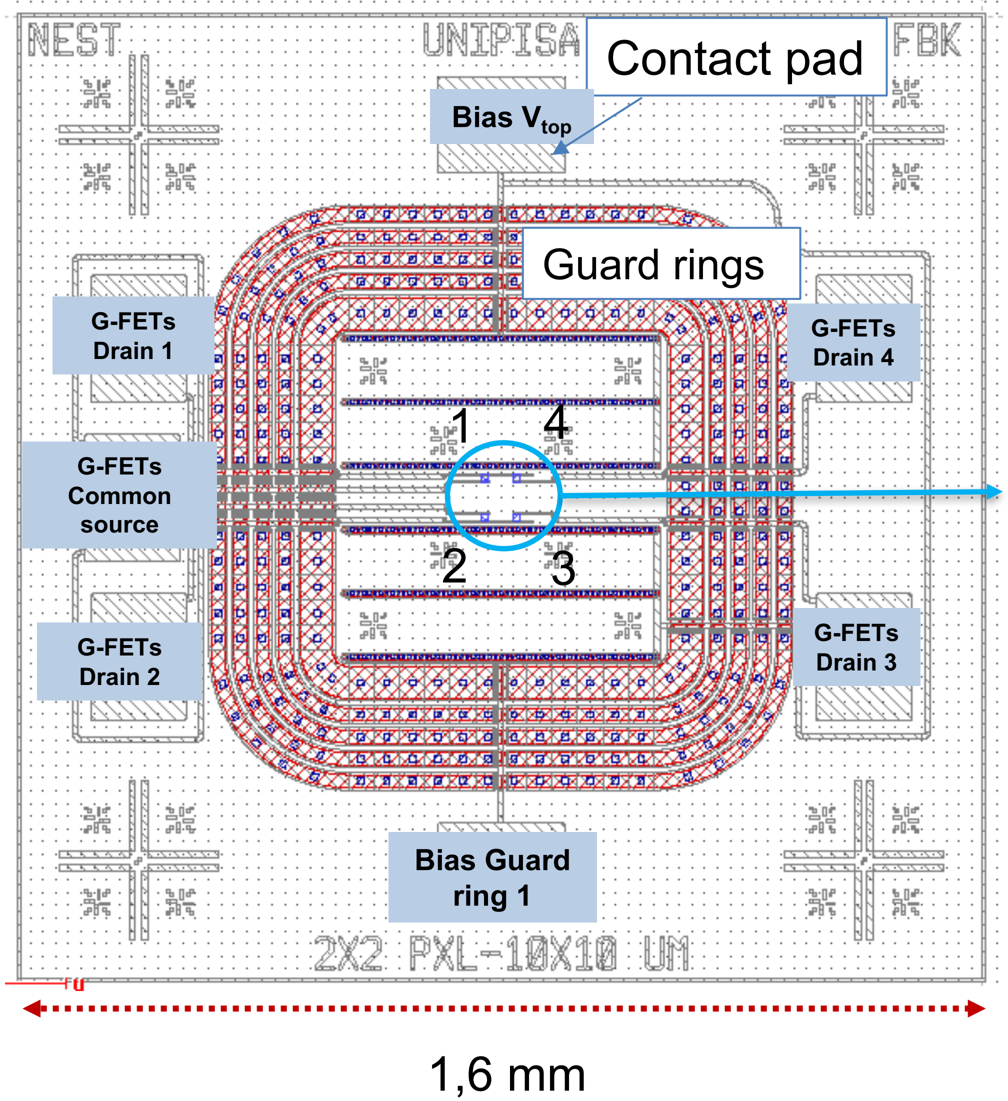
- SiO2 depostion (no litho)
- Back gate Implant (no litho)
- 1- p+ implant
- 2- Via holes contact
- 3- Metal (Al) contact
- Wafer dicing

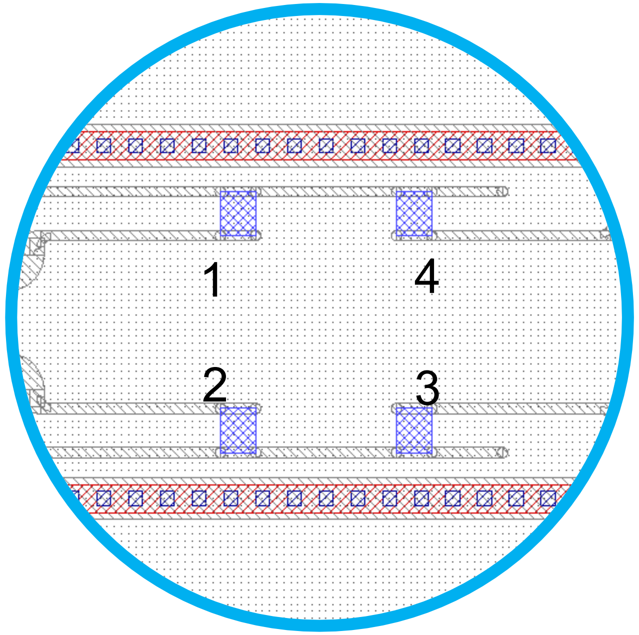
G-FET Fabrication@NEST

- Graphene transfer
- Channel definition (EB litho)
- Cr/Au overlay for contact recovery (if needed)



Unit cell design





Sensor active area

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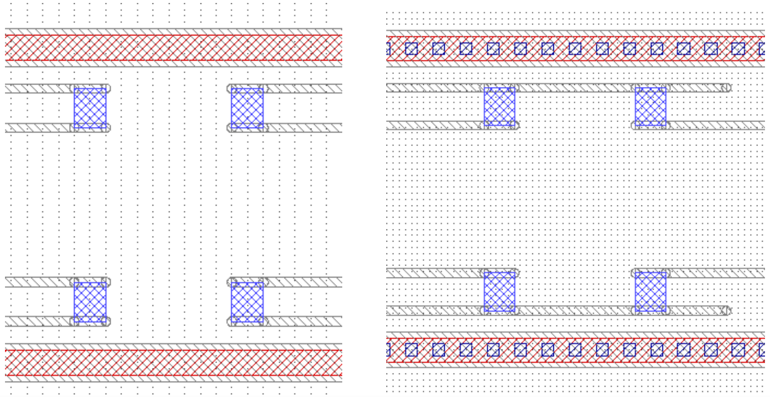
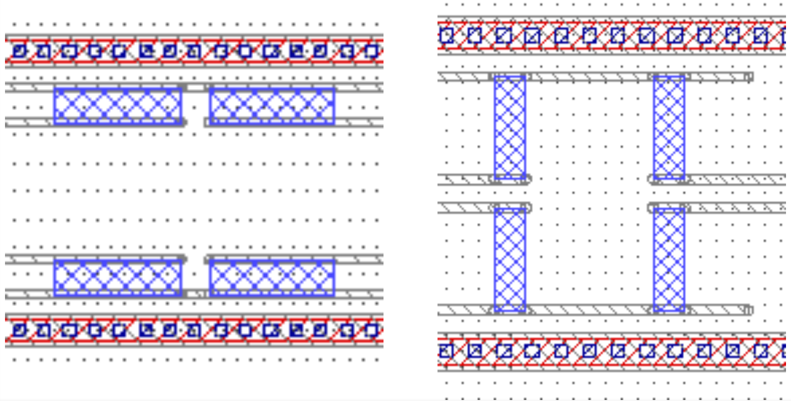
Design variations

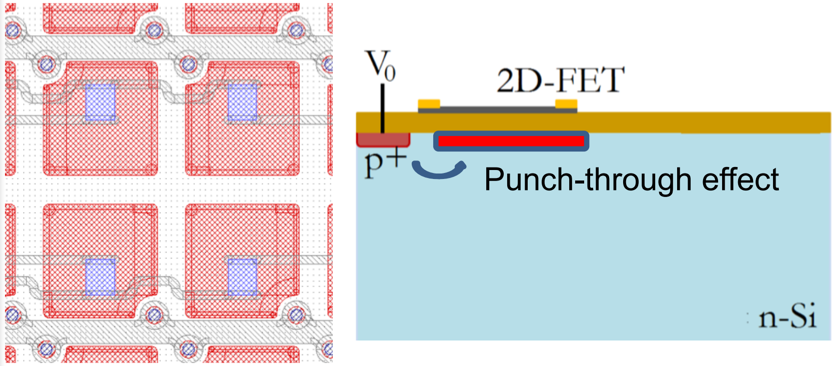
Symmetric and asymmetric



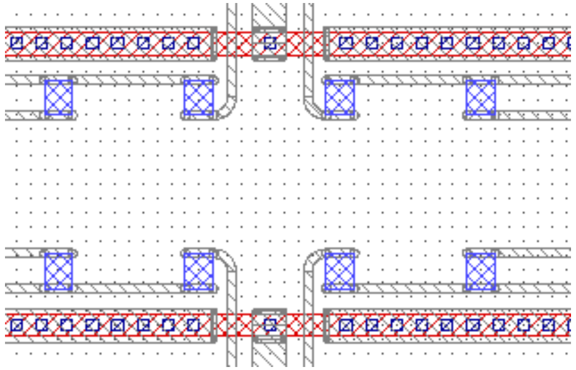
Different aspect ratio



Punch-through

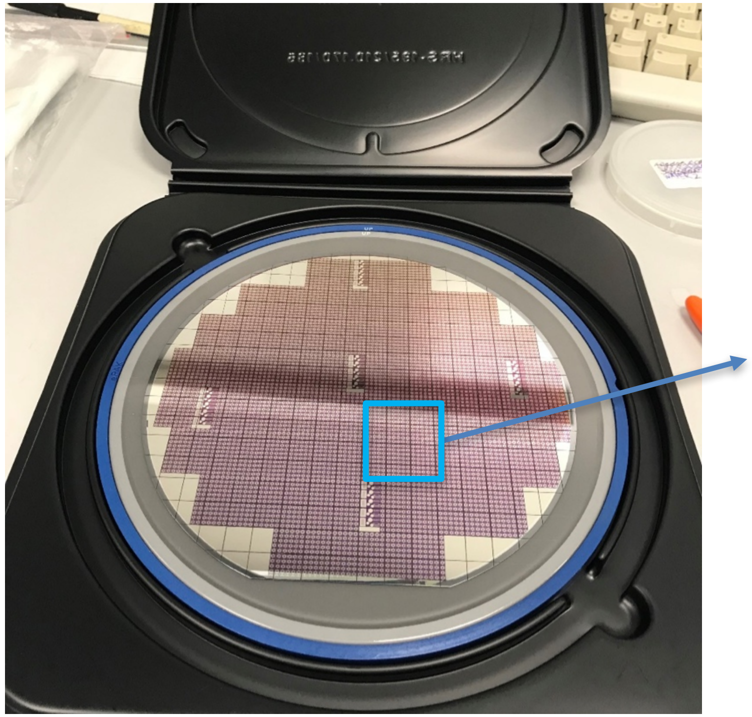


Array 4x2

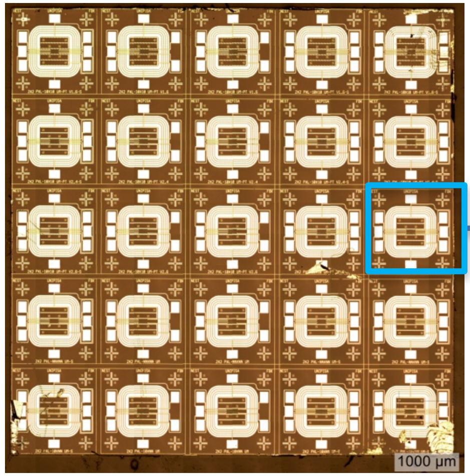


FBK wafer 1st run

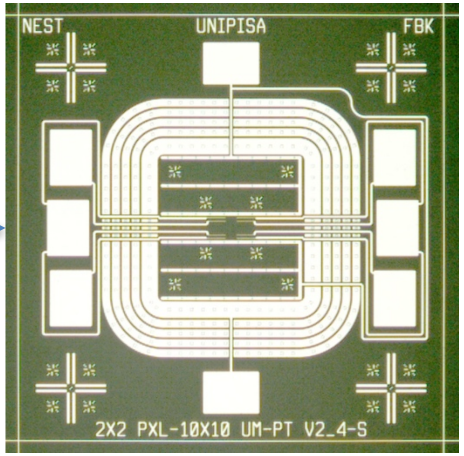
1st batch: two wafers with different SiO_2 thickness, 300 nm and 100 nm



6-inches wafer (FBK)



8x8 mm die (NEST)



1,6x1,6 mm unit cell

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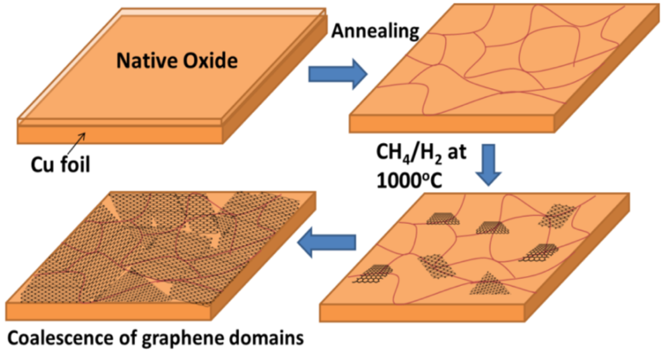
CVD @NEST

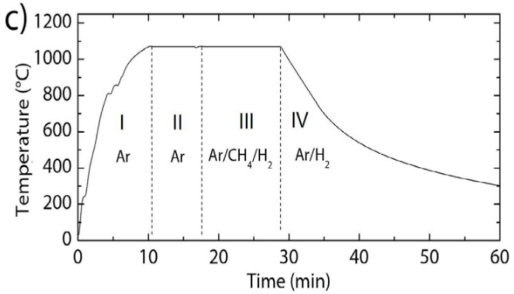


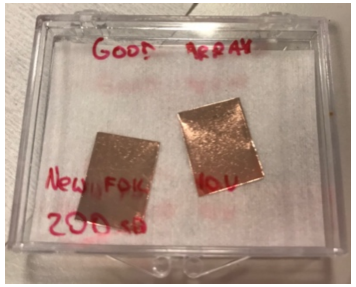
Chemical Vapor Deposition (CVD) on transition metal substrates is the most promising, readily accessible, and inexpensive method to obtain high-quality graphene on large area

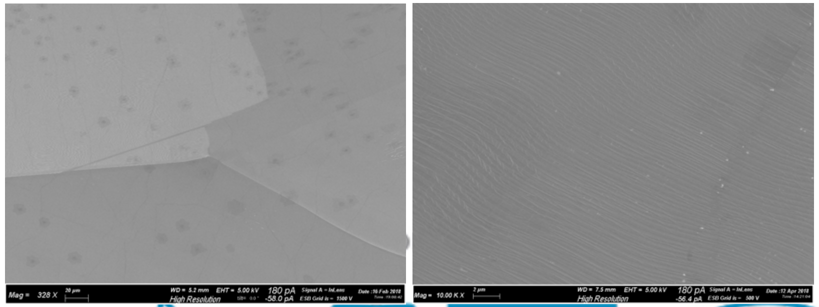
Growth Parameters (Cu substrate):

1. *Pressure (0.05 Torr – atm. P)*
2. *H2/CH4/Ar partial pressures ratio*
3. *Temperature (950-1050, Cu-Tmelt)*
4. *Pre-Annealing conditions, surface preparation*

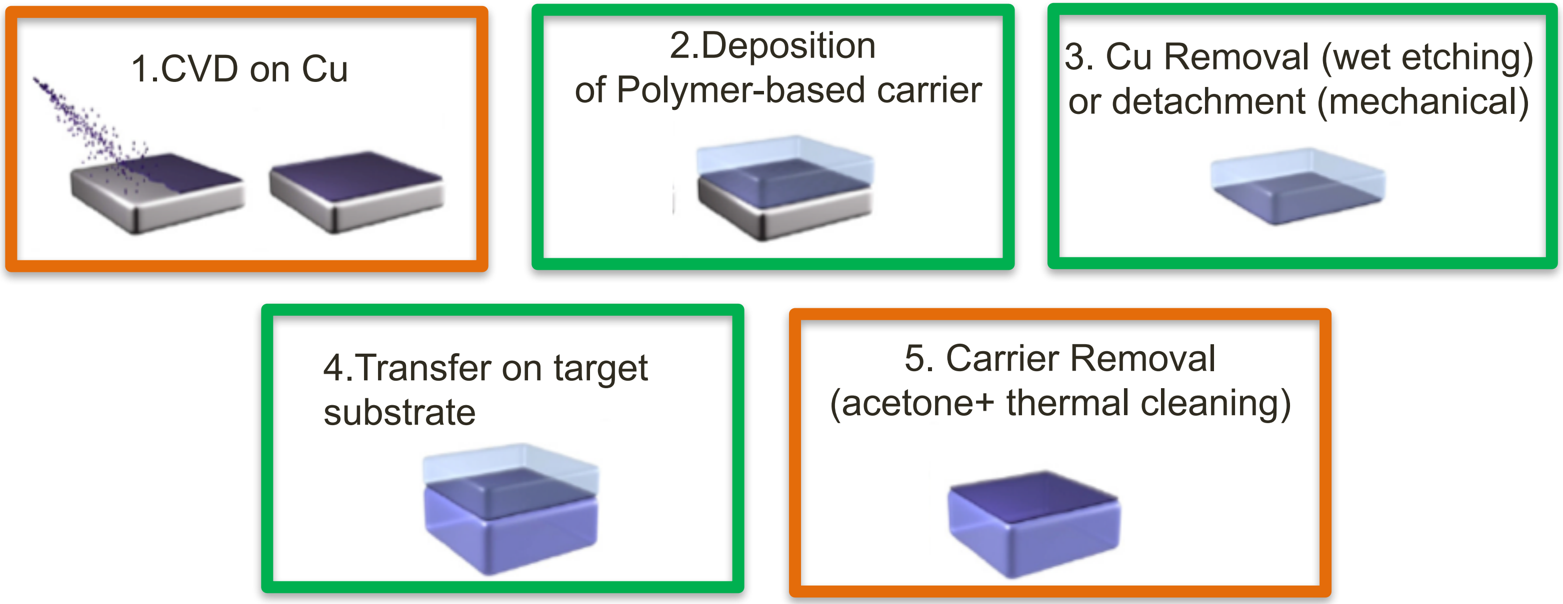
Aixtron Black-Magic: Cold-wall reactor enabling very fast graphene synthesis on cm-scale sample







Graphene transfer on Si absorber



1.CVD on Cu

2.Deposition of Polymer-based carrier

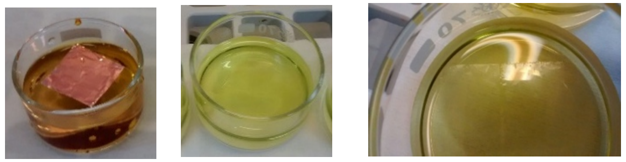
3. Cu Removal (wet etching) or detachment (mechanical)

4.Transfer on target substrate

5. Carrier Removal (acetone+ thermal cleaning)

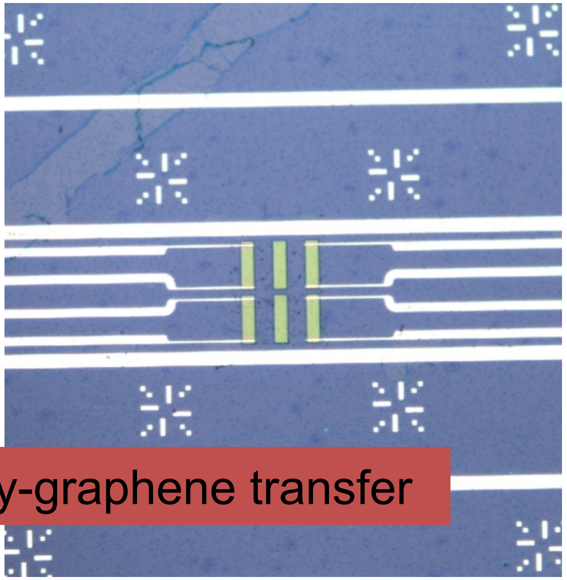
We used this approach first on poly polycrystalline graphene:

- Optimal CVD not critical, full coverage of the Cu substrate with single layer poly-graphene
- Grain size up to 10 um; higher reliability (easiest manipulation, large area compatible)

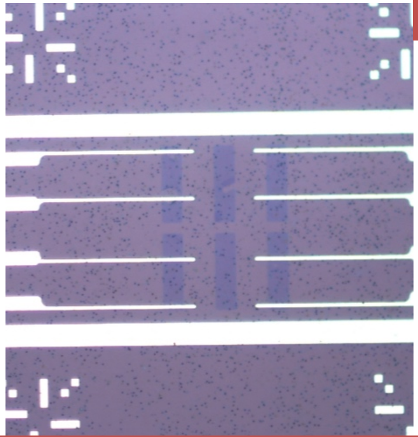


Removal of the Cu substrate via chemical wet etching

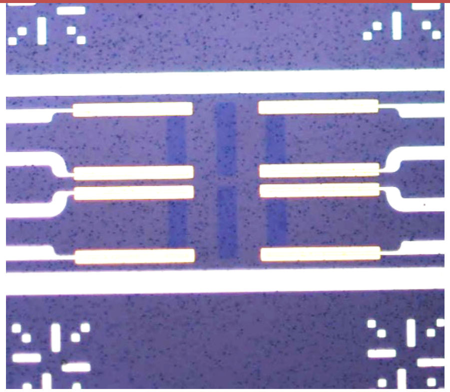
poly-graphene sensors



Poly-graphene transfer

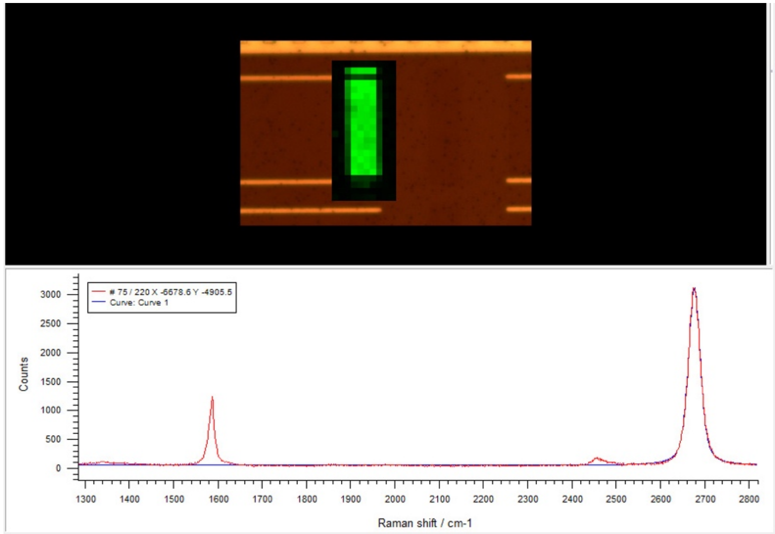


EB litho + graphene etching



Cr/Au overlay contact recovery

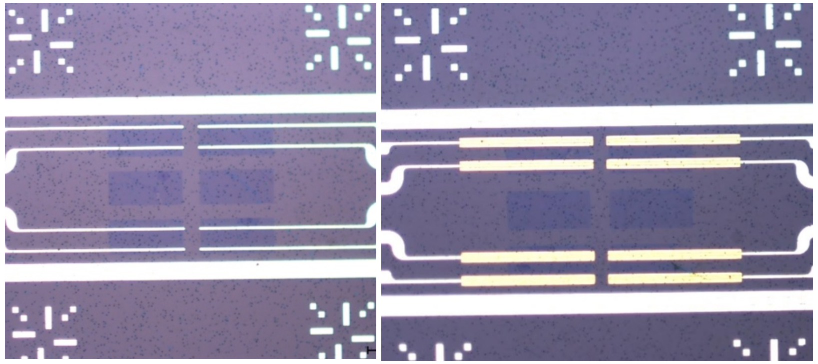
See Daniele’s talk for IV results



Raman spectroscopy

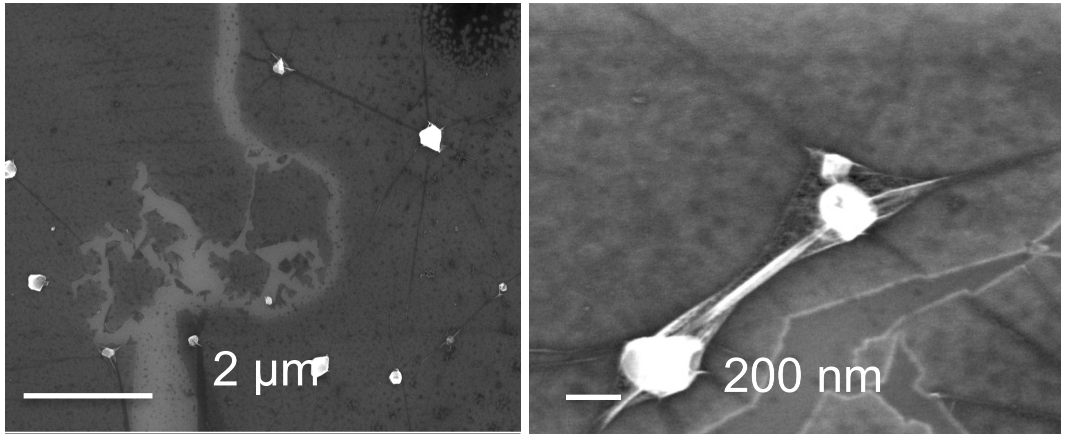
FWHM (2D peak) = 32 cm^{-1}
I2D/IG = 3
Weak evidence of D-peak

Critical issues



Aluminium is not suitable for graphene ohmic contacts because of the thin native oxide

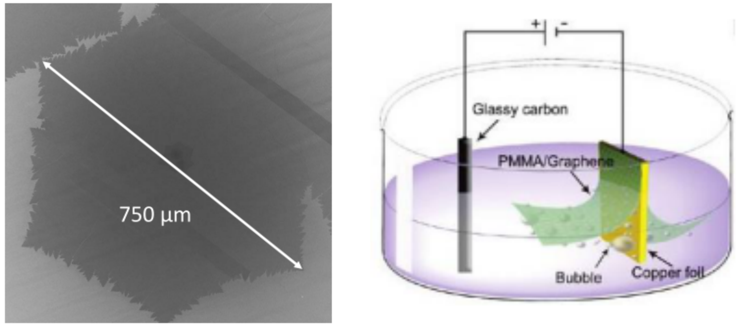
Our solution: after graphene transfer, evaporate an additional Cr/Au overlay on top of graphene/Al



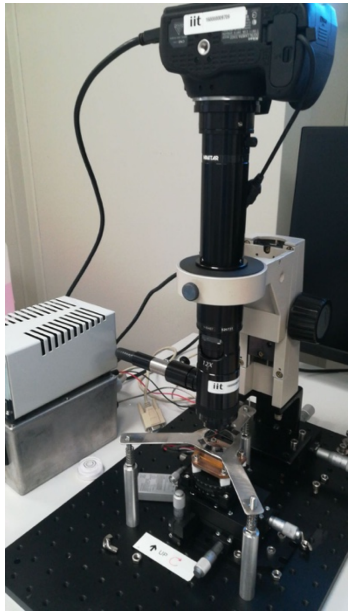
Residual Silicon particles (200 nm) arising from the aluminium etching step during FBK wafer processing.

Next wafer run will be without Aluminium.

single crystal graphene

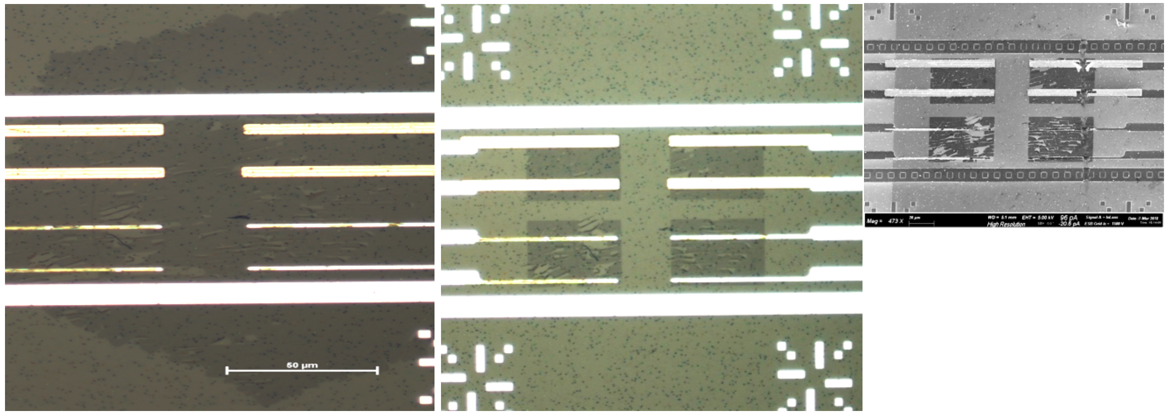


Miseikis et al, 2D mater. 2015



Different CVD growth condition lead to synthesis of single crystal graphene, with size up to 1mm

Also requires a different transfer method (galvanic detachment, etchant free)



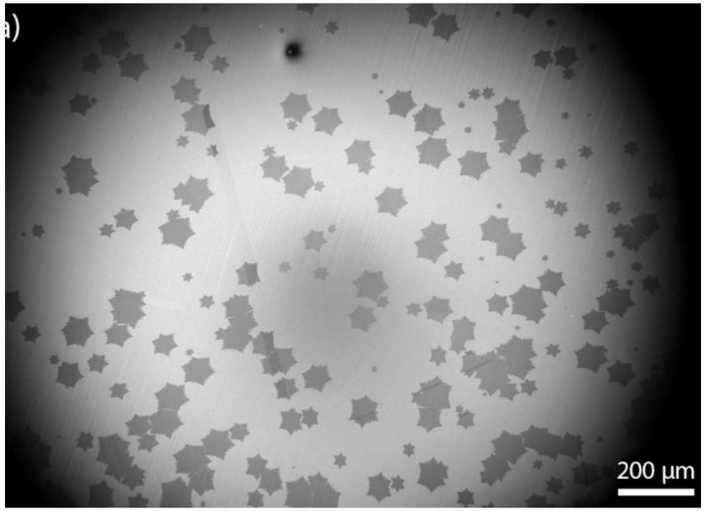
Higher quality graphene,
But presently much lower yield

Progress status and possible improvements

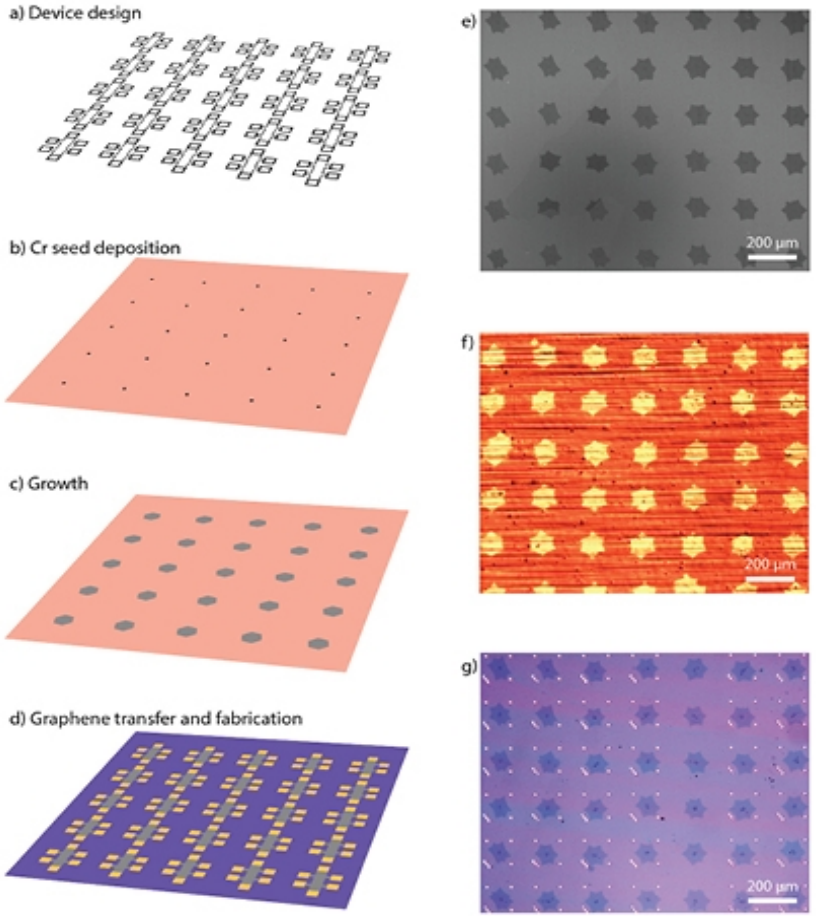
1 run: successfully fabricated 2 samples with poly-G with several good G-FETs + 1 more sample ready

2 run: in progress @FBK; Cr/Au contacts.

Random position of graphene crystals



Deterministic patterned growth



…a path towards wafer scale integration
V. Miseikis et al 2017 2D Mater.