Characterization of the Graphene Devices

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Main properties of graphene to exploit

- it's characterized by a strong ambipolar effect;
- the presence of the Dirac point.

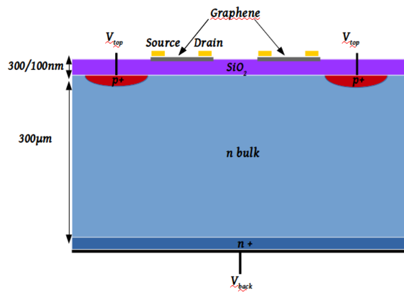
R (kOhm)
2.0
1.5
1.0
0.5
-3x10^7
-2
-1
0
1
2
3
Electric Field (V/m)

Outline

- simulation of the prototype structures ;
- characterization of the silicon wafers;
- study of the structures without graphene;
- determination of the Dirac point for the structure with synthesized and transferred graphene;

Layout of the device

A silicon sensor with a thickness of $300\ \mu m$ covered in the upper part with a layer of SiO_2 and with a sheet of graphene on top constitutes the prototype detector.



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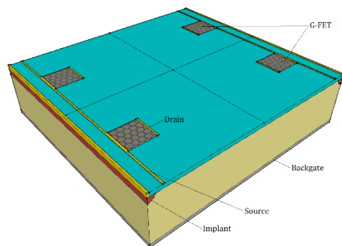


(b)

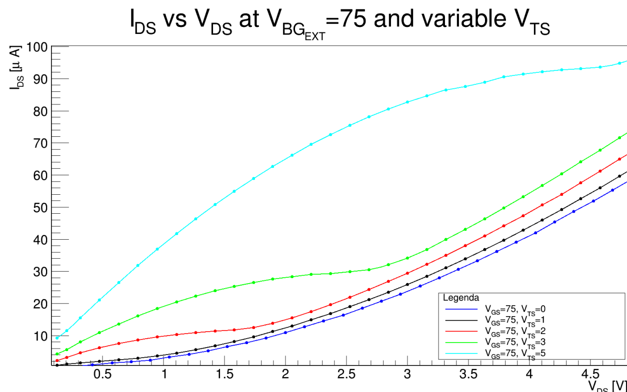
Simulations

- A 2D and a 3D design of the prototype structures were performed using **Sentaurus TCAD©**;
- An electrostatic study of the 2D simulations was performed;
- The response of the device to a **MIP** was simulated by adding an optical beam that for a certain time strikes the designed prototype with an appropriate intensity and wavelength.

2D simulations results

The transistor-like behavior of the G-FET is obtained if the bulk is over-depleted applying a $V_{back} = 75\ V$ at fixed values of V_{top} and varying th V_{DS} from $0\ V$ to $5\ V$.

The results are in good agreement with the expected behavior from literature.



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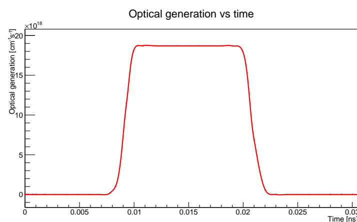
2D simulations results

A MIP was simulated including an optical beam that induces in the bulk around 23.000 e-h pairs.
The signal induced from such a beam during a time-dependent simulation is shown below.



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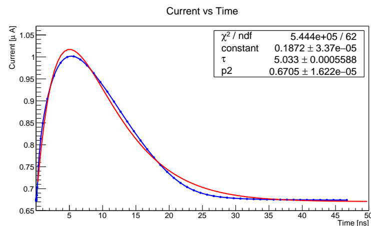
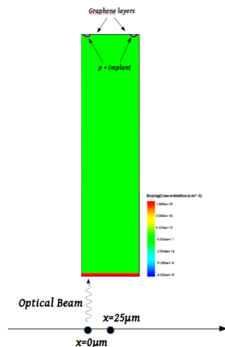


(d)

2D simulations results

I studied the response of the device for different position of the striking beam.



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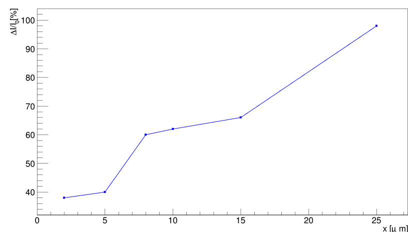
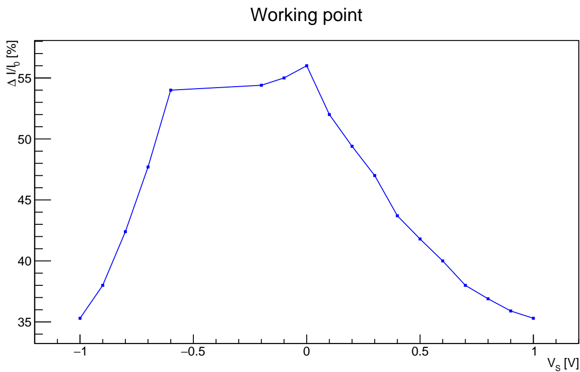


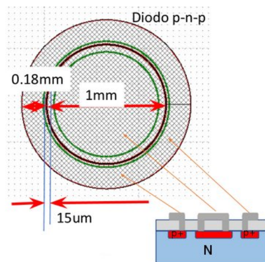
(f)

I studied the response of the device at different voltage for the source maintining the voltage difference between drain and source of 100 mV in order to find the optimal working point for the device.



Silicon wafer characterization

GRD and GCD were used to characterize the wafer.



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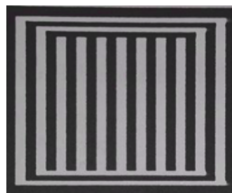
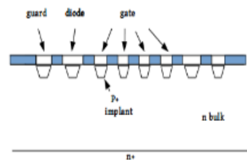
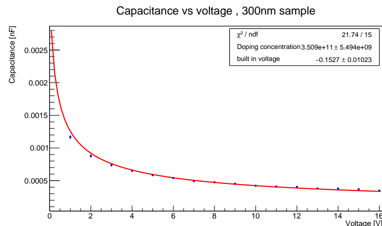




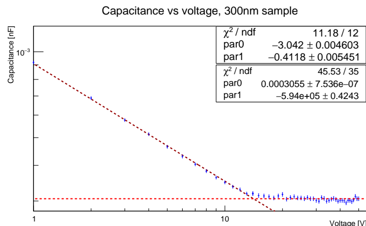
(h)

GRD

It's a pn junction provided with a guard ring. From a C-V measurement it's possible to extract the information on: the **width** of the bulk, the **doping concentration** in the bulk, and the **depletion voltage** the device.



(i)



(j)

Figure : (g) C-V curve of the 300 nm sample. (h) LogC-LogV plot for the same sample.

Silicon wafer characterization

The characterization was performed to update the simulations and also to double check the presence, measured at first by FBK, of a **higher surface leakage current** of around one order of magnitude than what was expected by producers.

Table 3.1: Characterization of the wafer with SiO_2 300 nm thick

Parameter	Value
Depletion width maximum	276 ± 7 [μm]
Voltage at total depletion	16 ± 3 [V]
Doping concentration from C-V curve	$(2.8 \pm 0.5) \cdot 10^{11}$ [1/cm^3]
Doping concentration from $\frac{\delta 1/C^2}{\delta V}$	$[(2 \pm 0.1) \cdot 10^{11}$; $(6 \pm 0.6) \cdot 10^{11}]$ [1/cm^3]

Table 3.2: Characterization of the wafer with SiO_2 100 nm thick

Parameter	Value
Depletion width maximum	271 ± 5 [μm]
Voltage at total depletion	15 ± 2 [V]
Doping concentration from C-V curve	$(3.1 \pm 0.5) \cdot 10^{11}$ [1/cm^3]
Doping concentration from $\frac{\delta 1/C^2}{\delta V}$	$[(2 \pm 0.2) \cdot 10^{11}$; $(8 \pm 0.6) \cdot 10^{11}]$ [1/cm^3]

GCD

GCDs are used to measure the generation of carriers at the interface *Si-SiO*$_2$ to evaluate its quality when the voltage between the gate and the substrate is varied.

Igate vs Vgate, x09y03 sample central structure

Igate [A] ($\times 10^{-9}$)

0, −0.05, −0.1, −0.15, −0.2

I_{vol}

$I_{vol'} + I_{vol''}$

$I_{vol} + I_{vol'} + I_{Sup}$

Legenda

Leakage current vs V_{gate} at V_{bias}=1V

−10, −8, −6, −4, −2, 0

Vgate [V]

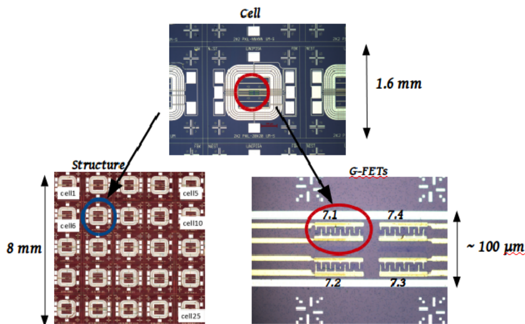
Silicon wafer characterization

The surface leakage current value was confirmed, as expected from the measurements done by FBK, to be :

- $5.7 \pm 0.8\ nA/cm^2$ for the *300 nm* SiO_2 thick;
- $12 \pm 0.2\ nA/cm^2$ for the *100 nm* SiO_2 thick.

Real prototypes layout

The wafers are divided in cm-size chips each of which constituted by **25 cells** that can host a number from **4 to 8 graphene layers** depending on their internal design. The the electrical characterization have been done using a probe station that is contained in a black box to shield the device from light sources.

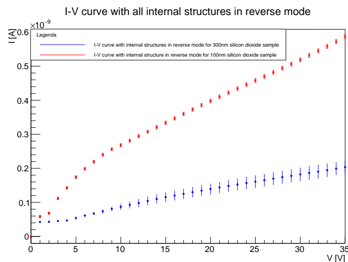


Real prototypes without graphene

A study of the I–V curves for the structures before the graphene transfer was performed in order to check in the successive study if the leakage current after the transfer in the bulk has increased consistently. That is necessary to check that no damage to the SiO_2 has occurred due to the problem experienced during production.
Observations:

- the cells in the border of the structures showed an higher leakage current;
- the 300 nm wafer as expected shows a lower leakage current respect to the 100 nm one.

Results on real prototypes without graphene



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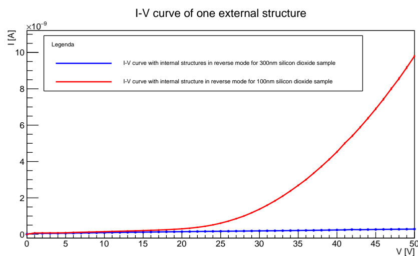

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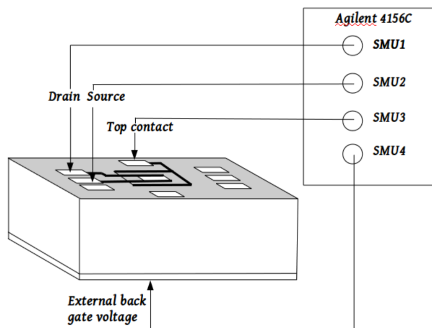
Measurements on the real prototypes with graphene

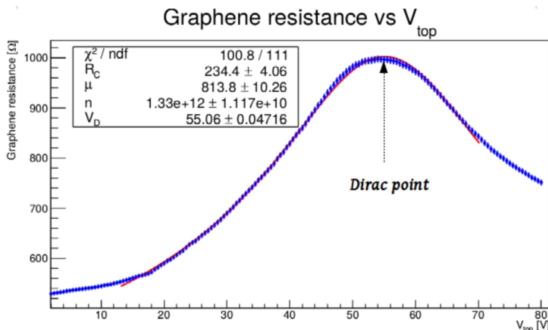
Run1, sampleX: 5 good G-FETs.



Dirac point on the first structure

As an example it is shown the ambipolar transfer curve of one of the GFET studied showing the Dirac point crossing at V_{top}=55V. The formula used for the fit is the following:

$$R_g = R_c + \frac{N_{sq}}{\mu e \sqrt{n^2 + (\frac{C_{ox}}{e})^2 (V_G - V_D)^2}} \tag{1}$$



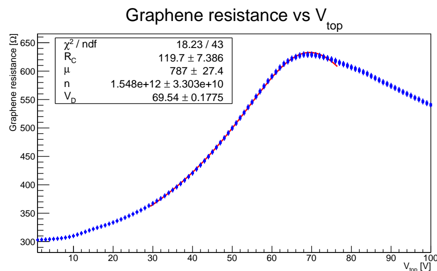
Further electrical characterization

The Dirac voltages obtained were furtherer studied in order to understand:

- how their position varies during time if exposed to air;
- if it's possible to obtain the Dirac points sweeping with an higher offset between the top and the back voltage to ensure always full depletion of the bulk.
- if it's possible to obtain them when sweeping only the top voltage at fixed bottom voltage and vice-versa;

Dirac voltage over time

We observed a shift in the Dirac voltage position after a week on our GFETs, left in atmosphere and at 20°C, both positive and negative with a maximum variation of *5 V* in module.



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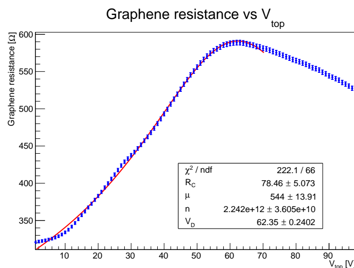
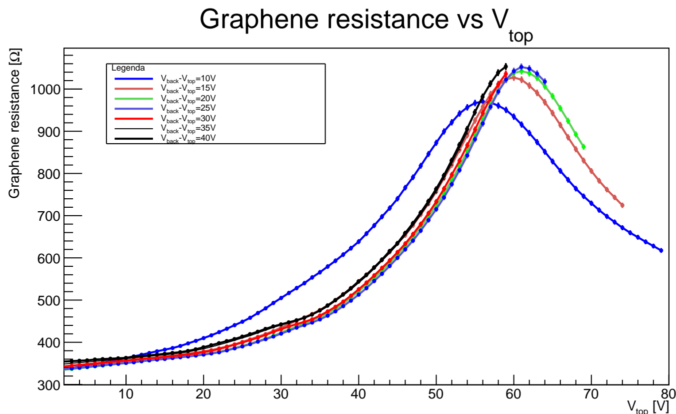


(d)

Dirac point imposing an offset between V_{back} and V_{top}

We imposed offset of different values between V_{back} and V_{top} to ensure always the depletion during the swept of these voltages. Also in this case we observe that over depletion seems to stabilize the DP position respect to V_{top}.



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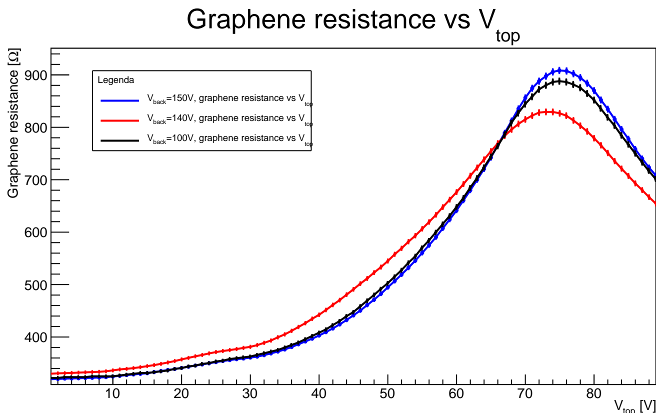
Dirac point crossing at V_{back} fixed and V_{top} swept

Dirac point crossing was clearly seen also with the strategy of fixing before, using the instrument ke 237, the back voltage and then sweeping the top contact. The Dirac point position is mostly unaffected by the back gate, provided that the bulk remains over depleted.



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Dirac point crossing sweeping V_{back} with V_{top} kept at ground

We tried to sweep the V_{back} from *0 V* to *100 V* keeping at ground the V_{top} but with that strategy no Dirac point crossing was observed, however was observable a clear modulation of the current in the graphene layer.

Current through graphene vs V_{back}

I_D [μ A]

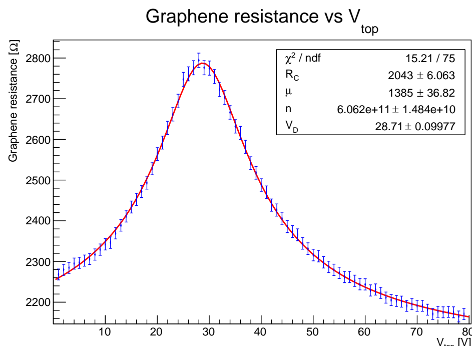
16
15.5
15
14.5
14
13.5
13

10 20 30 40 50 60 70 80

V_{back} [V]

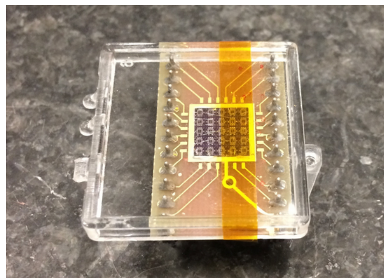
Dirac point on the second structure

Two weeks ago we received from NEST a second structure with graphene transfered. This sample was really promising since **10 graphene layers** were found and the **Dirac points position** respect to V_{top} were **at lower voltages** than the previous sample studied. All Dirac points voltages were found in the range V_{top}=[*10 V - 40 V*].



Work in progress

After we have inserted the structure on the holder inside the case we re-found the Dirac point position voltages on the devices previously tested.



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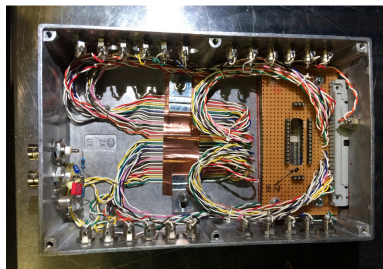

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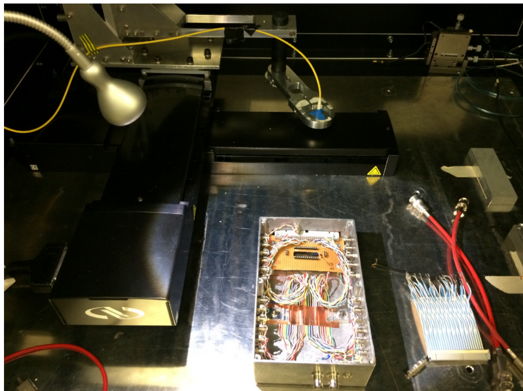
Work in progress

- A study of the response of the device to a laser beam.
- Test on new structures with gold/chromium contacts instead of aluminum contacts.



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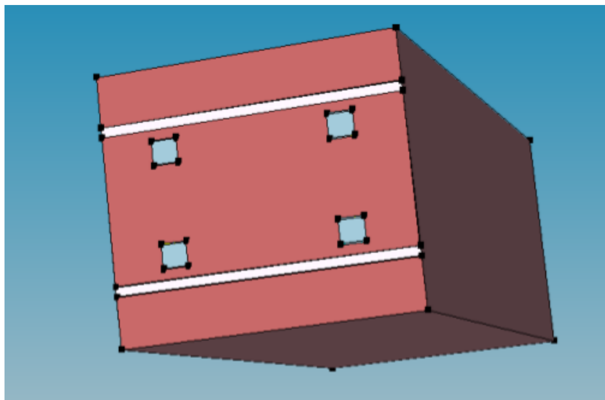
Backup slides

3D simulation

A 3D prototype was designed to be electro-statically studied as for the 2D one. In order to understand how refined the mesh must be defined some simulations were performed in order to check how much were varying the physical quantities at the contacts.



2D simulations specifics

The structure simulated is composed by a silicon bulk n-doped with a concentration od free carriers of $5{\cdot}10^{11}$ that correspond almost to the one measured during the characterization of the silicon wafer. The silicon bulk has a thickness of $300\ \mu m$ and is $\sim 70\ \mu m$ as length. In proximity of the back contact a n + implant with a concentration of $5{\cdot}10^{19}$ carriers is present . Two p + implants are present on top with a concentration of $1{\cdot}10^{19}$.

On top of the silicon bulk is textit300 nm SiO_2 thick and above it there are two graphene layers with a length equal to 10 μm.

2D simulations specifics

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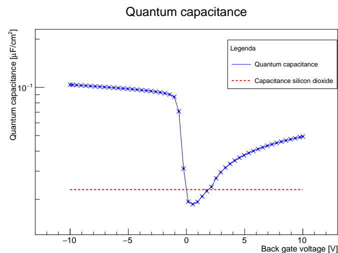
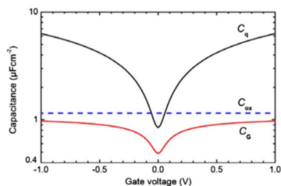
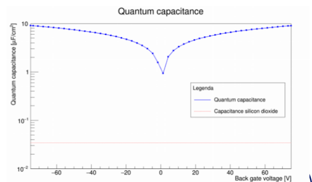
Quantum capacitance from simulations





(g)



(h)

kink-effect

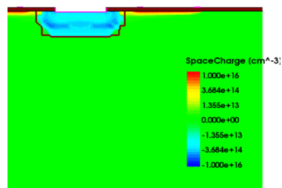


Figure : V_T=5 V, V_B=75 V and V_D=0.1 V

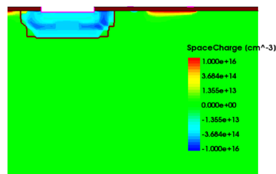


Figure : V_T=5 V, V_B=75 V and V_D=5 V

kink effect (2)

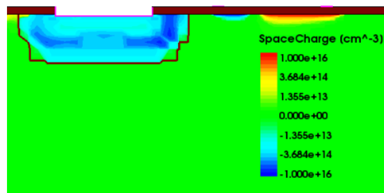


Figure : V_T=5 V, V_B=75 V and V_D=20 V

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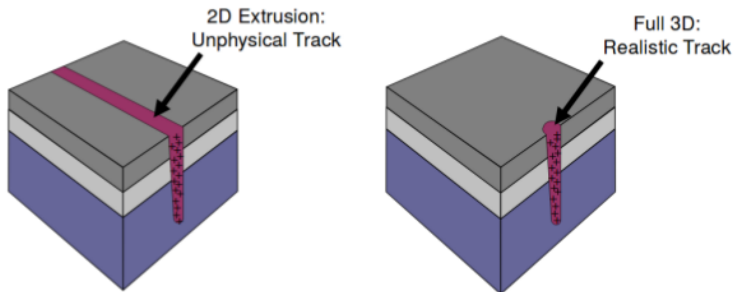
Reasons behind the choice to design a 3D simulation

A 3D simulation could in principle be of great help when we compare the results obtained in real prototypes with the simulated one. In fact a 3D simulation takes into account the presence of fringing fields and also the track of an optical beam that strikes at a certain point our device results more physical meaningful.



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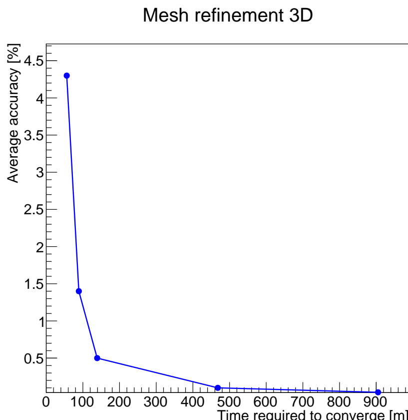
Mesh refinement choice

The mesh was chosen in order to be a good compromise between accuracy of the result and time of convergence of the simulation. The 3D design was then simulated in the electrostatic case with different mesh more and more dense in order to be able to choose the right compromise.



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Reasons behind the choice to not go further with the 3D study

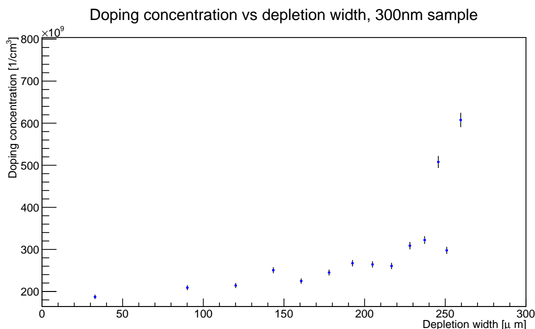
The real issue with the 3D simulation is the time required for convergence, the electrostatic simulation requires almost 10 hours to converge with an acceptable accuracy, that means that the transient simulation could requires almost 2 day to converge.

To proceed with this study in order to be complete as the one performed for the 2D design around two more months of work should be spent in 3D simulations.

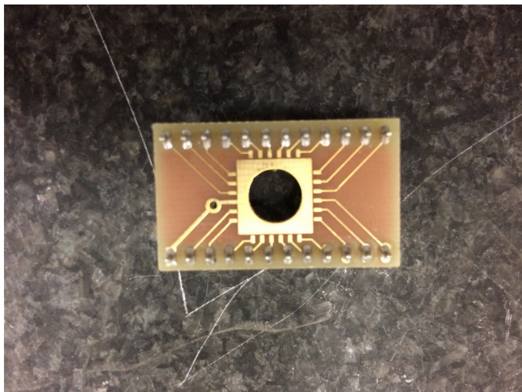
GRD fit function

$$C = \sqrt{(q \cdot \epsilon_r \cdot \epsilon_0 \cdot A^2 \cdot N_d)\frac{2}{\phi_i - V}} \quad (2)$$

The doping concentration was also extracted from the plot of $(\delta(1/C^2))/\delta V$



Work in progress backup



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References

1. Michael Foxe, Gabriel Lopez, Isaac Childres, Romaneh Jalilian, Amol Patil, Caleb Roecker, John Boguski, Igor Jovanovic, and Yong P Chen. Graphene field-effect transistors on undoped semiconductor substrates for radiation detection. Nanotechnology, IEEE Transactions on, 2012.

2. S. A. Thiele, J. A. Schaefer, and F. Schwierz. Modeling of graphene metal- oxide-semiconductor field-effect transistors with gapless large-area graphene channels. Journal of Applied Physics, 107(9), 2010