

Update on graphene structures: Dirac point study

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13/04/2018



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Status a week ago

- We have seen the Dirac points in 5 different G-FETs belonging to two cells (cell 7 and cell 8).
- Dirac points position was always at high voltages $\sim 70-90$ V seen when V_{back} and V_{top} were swept together maintaining an offset of 20 V between the two in order to grant depletion in Silicon.



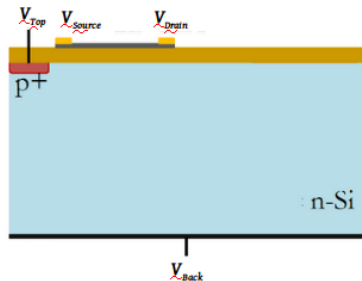
Study performed this week

It was checked the Dirac point behavior:

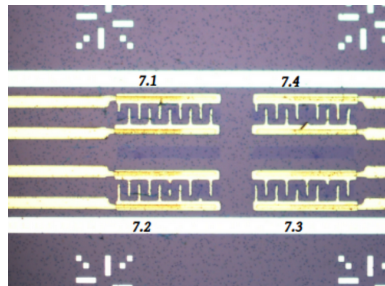
- after a week;
- when increasing the offset between V_{back} and V_{top} up to 40 V when possible;
- when it is changed $V_D - V_S$ in the range [-10 mV – 15 mV] ;
- when V_{back} is put at high values $\sim 130 - 150$ V and then it is swept V_{top} up to 100V.



Sketch on how the measure is done



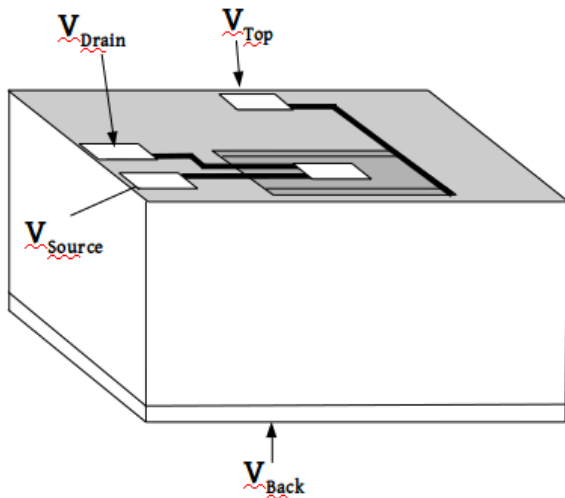
(a)



(b)

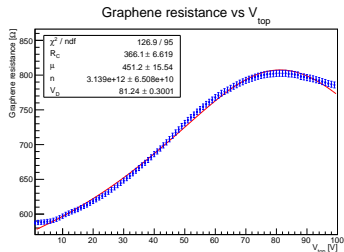


Sketch on how the measure is done

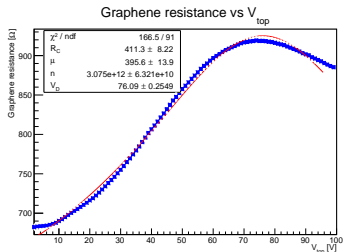


Dirac point position after a week

We observed a shift in the Dirac point position after a week on our structure of around 5 V. In figure the result for G-FET 7.1. Data obtained using Keithley 237 to provide a constant V_{back} of 130 V and sweeping, with Agilent 4156 C, V_{top} from 0 V to 100 V. $V_D - V_S = 5$ mV.



(c)

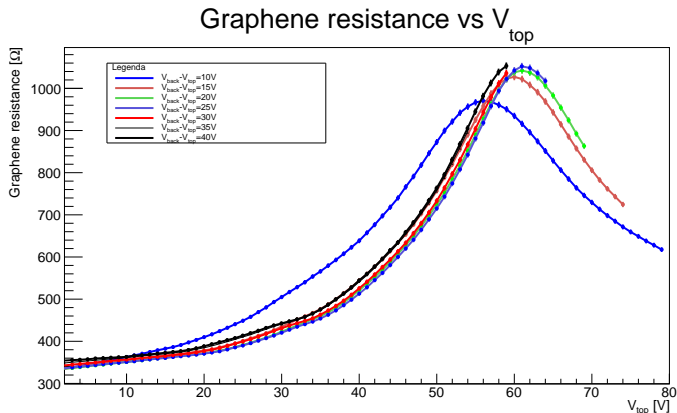


(d)



Dirac point increasing the offset between V_{back} and V_{top} up to 40 V

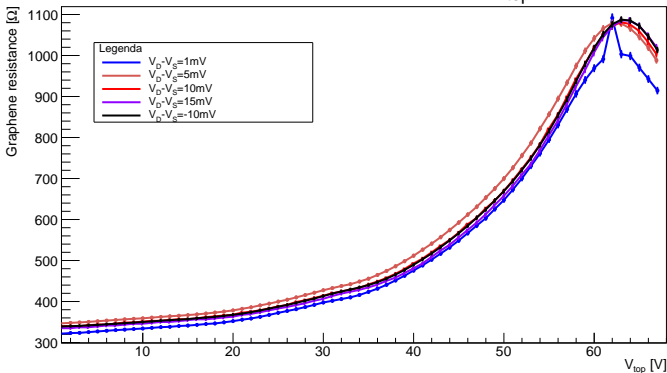
Data obtained using Agilent 4156 C to sweep synchronously V_{back} and V_{top} , while maintaining an offset of different voltages between the two contacts. $V_D - V_S = 5$ mV. The GFET is 8.4.



Dirac point changing V_D

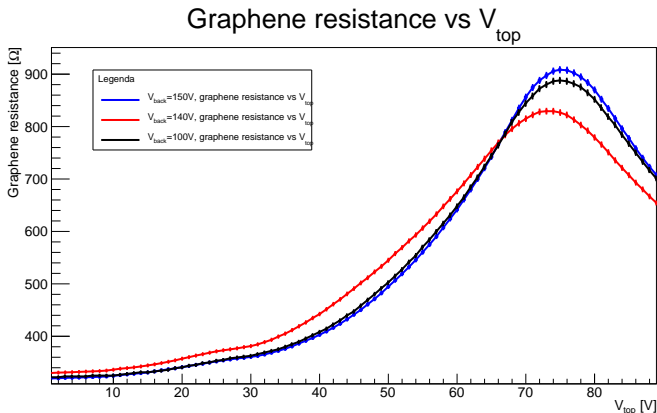
Data obtained using Agilent 4156 C to sweep synchronously V_{back} and V_{top} , while maintaining an offset of 30 V between the two contacts. $V_D - V_S = [-10 \text{ mV} - 15 \text{ mV}]$. The GFET is 8.4.

Graphene resistance vs V_{top}



Dirac point maintaining V_{back} t high voltages while sweeping V_{top}

Data obtained using Ke237 to provide an high constant value at V_{back} of 130 – 150 V, while Agilent 4156 C is used to sweep V_{top} from 0 to 100 V. $V_D - V_S = 5$ mV.



Conclusions

- Dirac point seem pretty stable when depletion is imposed in Silicon and over-deplete does not seem to shift at lower voltages the Dirac point position;
- respect to a time scale of 1 week Dirac point position shows a shift in the deposition of 5-10 % ;
- No dependence seems to be present in the Dirac point position due to different values of $V_D - V_S$;
- next week will receive a new chip with GFETs from NEST.



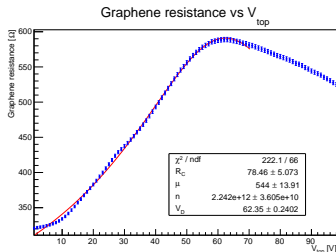
Back - up slides



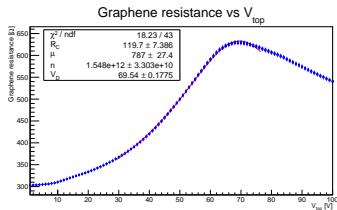
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Dirac point position after a week G-FET 7.3

Data obtained using Keithley 237 to provide a constant V_{back} of 130 V and sweeping, with Agilent 4156 C, V_{top} from 0 V to 100 V. $V_D - V_S = 5$ mV.



(e)

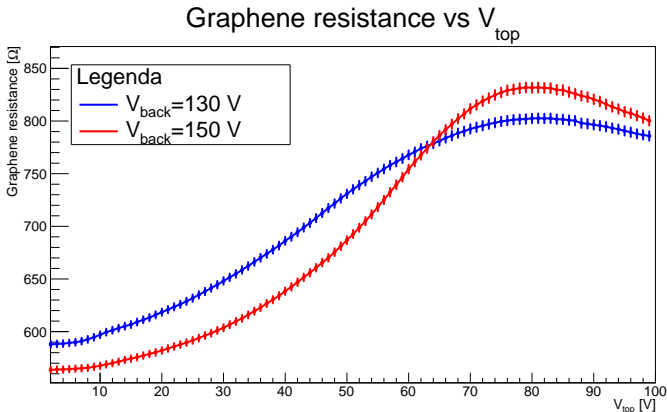


(f)



Dirac point maintaining V_{back} t high voltages while sweeping V_{top}

Data obtained using Ke237 to provide an high constant value at V_{back} of 130 – 150 V, while Agilent 4156 C is used to sweep V_{top} from 0 to 100 V. $V_D - V_S = 5$ mV. GFET 7.1.



Dirac point maintaining V_{back} t high voltages while sweeping V_{top}

Data obtained using Ke237 to provide an high constant value at V_{back} of 130 – 150 V, while Agilent 4156 C is used to sweep V_{top} from 0 to 100 V. $V_D - V_S = 5$ mV. GFET 7.3.

