Full sampling integrated ASIC for SiPM: some considerations

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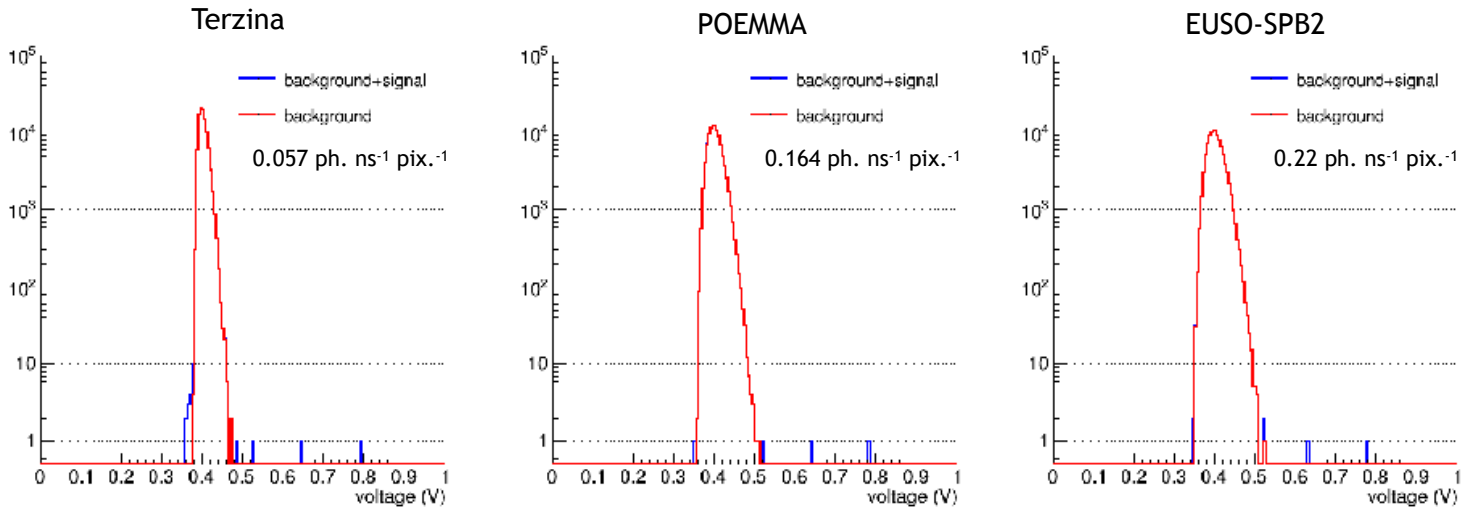
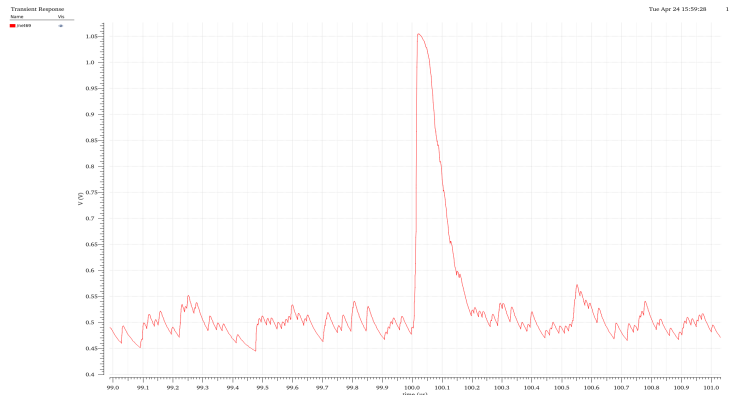
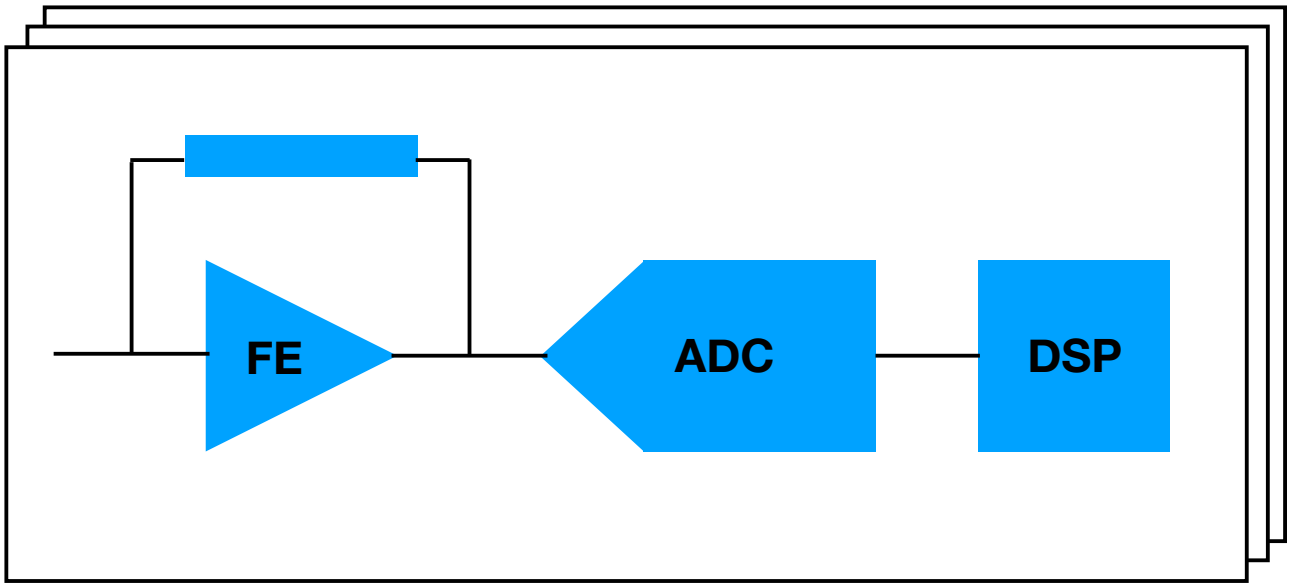
Starting point: the signal



- Physics signals of the simulated brightness is well separated from background
- Direct single photon counting problematic
- Statistical background monitoring can however be performed
- Many different architectures are possible



Full sampling architecture-1



- Signal is sampled and digitized directly at the front-end output
- Any further processing is done in the digital domain
- Baseline averaging to monitor the background
- Is this feasible with reasonable power?

A look at ADCs

This article has been accepted for inclusion in a future issue of this journal. Content is final as presented, with the exception of pagination.

A 12-bit 150-MS/s Sub-Radix-3 SAR ADC With Switching Miller Capacitance Reduction

Kwuang-Han Chang, *Member, IEEE*, and Chih-Cheng Hsieh, *Member, IEEE*

COMPARISON TABLE OF THE STATE-OF-THE-ART ADCS

	[25] Tseng, JSSC 2016		[8] Lin, TCASI 2016	[4] Hong, JSSC 2015	[9] Zhou, JSSC 2015	[10]Mathew, VLSI 2015	[26] Tsai, JSSC 2015	This work
Architecture	SAR		Pipelined-SAR (2-ch)	Pipelined	Two-step SAR	Flash-TDC SAR	SAR	SAR
Technology	28 nm		65 nm	65 nm	40 nm	45 nm	28 nm	40 nm
Supply Voltage	1.2V/1.1V		1.0 V	1.2 V	1.1 V	0.85 V	1.0 V	0.9 V
Resolution	12 bit		12 bit	12 bit	12 bit	12 bit	10 bit	12 bit
Sampling Rate	104 MS/s		210 MS/s	250 MS/s	160 MS/s	200 MS/s	240 MS/s	150 MS/s
SNDR @ peak (dB)	60.5*	63**	63.4	67.0	66.5	68.5	57.1	61.7
SFDR @ peak (dB)	76*	N/A**	77.5	84.6	85.9	N/A	73	74.4
SNDR @ Nyq (dB)	45*	N/A**	60.1	65.7	65.3	68.0	53	56.2
SFDR @ Nyq (dB)	52*	N/A**	74.8	79.0	86.9	N/A	63	63.5
DNL (LSB)	< 0.5		-0.57 / +0.66	-0.86 / +0.52	N/A	-0.60 / +0.40	+0.45 / -0.23	-0.91 / +1.77
INL (LSB)	< 1.1		-0.68 / +1.45	-0.90 / +1.08	N/A	-0.90 / +0.80	+0.55 / -0.45	-2.63 / +2.95
Power (mW)	3.06*	0.88**	49.7	5.3	4.96	3.4	0.68	1.5
FoM_w @ peak (fJ/conv.-step)	34*	7.3**	20.9	108.5	17.7	7.9	4.8	10.3
FoM_w @ Nyq (fJ/conv.-step)	203*	N/A**	30.3	126.8	20.7	8	7.8	18.9
Core Area (mm^2)	* 0.024	** 0.003	0.594	0.48	0.042	0.06	0.003	0.04

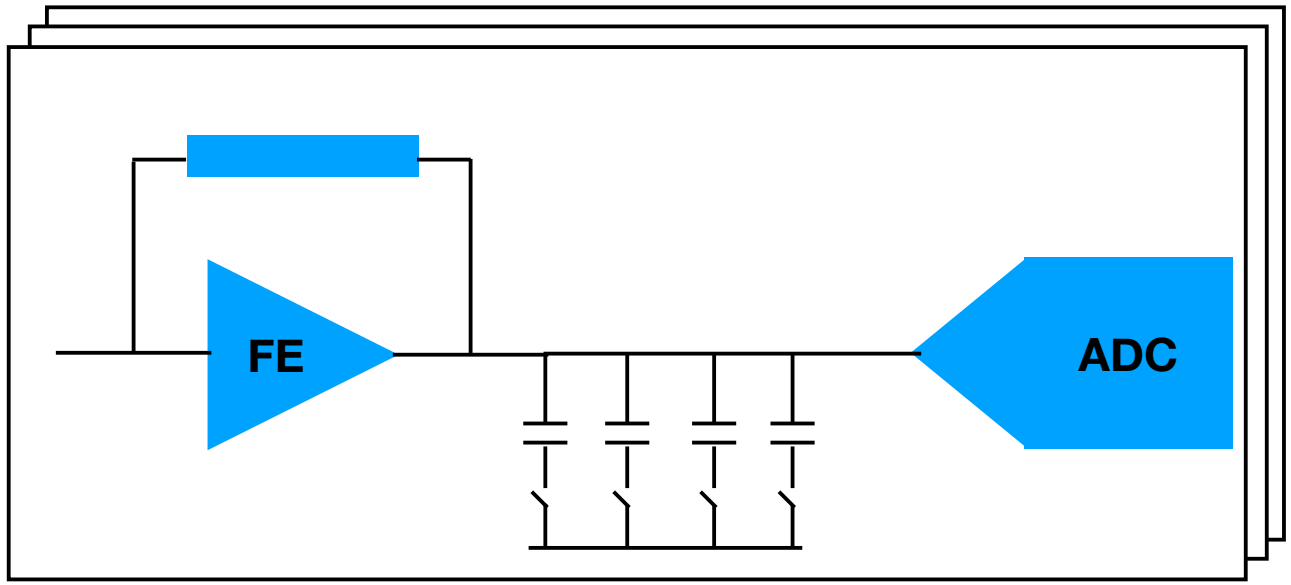
* : ADC+Ref+Buf
** : ADC only

A look at ADCs

Technology	Architecture	N of bit	Sampling rate (MS/s)	ENOB	Power (mW)	FOM (Fj/step)
90 nm	SAR	9	40	8.23	0.82	68
130 nm	SAR	10	50	9.11	0.82	30
65 nm	SAR	10	100	9.01	1.13	22
90 nm	FLASH+SAR	9	100-200	8.44-8.31	0.75/1.33	34.7
90 nm	SAR	10	50	9.5	0.32	9

- Design of SAR ADCs is "straightforward"
- A cheap 130 nm process can do the job as well
- Two 50 Ms/s can be time-interleaved
- Estimated power for 2, 50 Ms/s ADC at 8 bit: $1.2 \div 1.5$ mW/ch
- Total power can be kept below 10 mW/ch, probably around 5 mW/ch

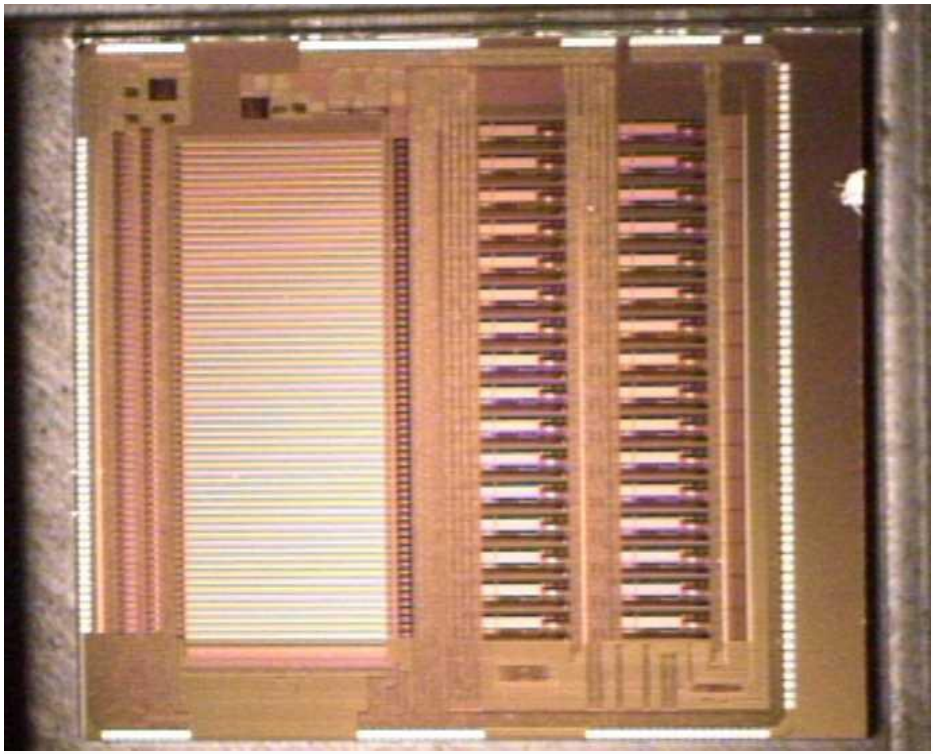
Full sampling architecture-2



- Signal is sampled in an analog memory
- Analog samples are digitized when a trigger is provided
- Internal trigger for physics signal.
- External trigger for periodic background monitoring
- Is this more convenient?

An example from the past

- Front-end for Silicon Drift Detectors (SDD) for ALICE at CERN

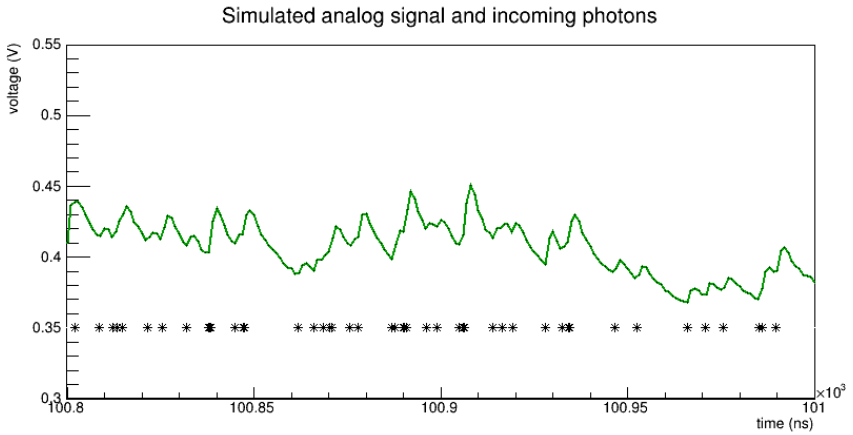


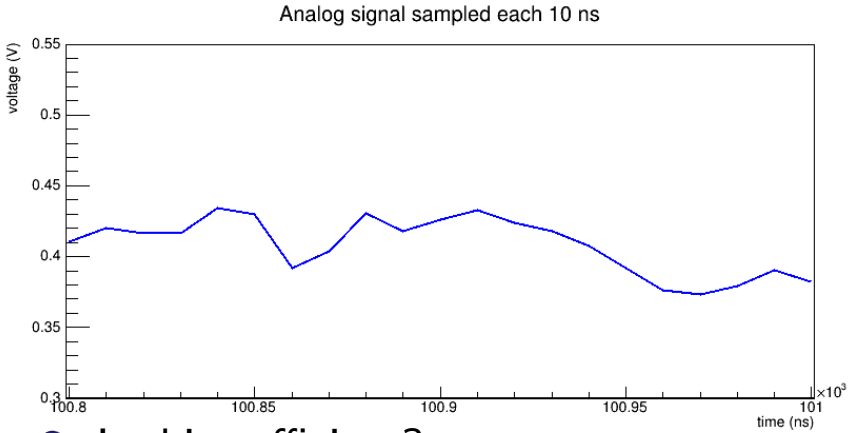
- 64 channels
- 40 MHz sampling
- 32 10-bits SAR ADCs
- LDOs, pulser, DACs on chip
- Only 4 1 μF SMD capacitors
- Power: 5 mW/ch
- CMOS 0.25 μm
- 2080 ASICs taking data since 2008
- All chips still alive

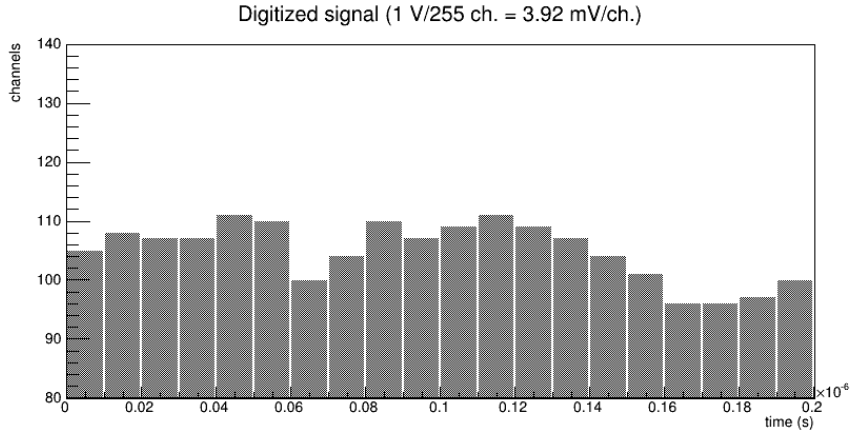
ADCs vs analog memories

- With today ADC performance, analog memory power advantage becomes marginal
- Analog memory offers more flexibility in term of maximum sampling frequency
- Event selection in the digital domain more powerful and safer

More on back-ground

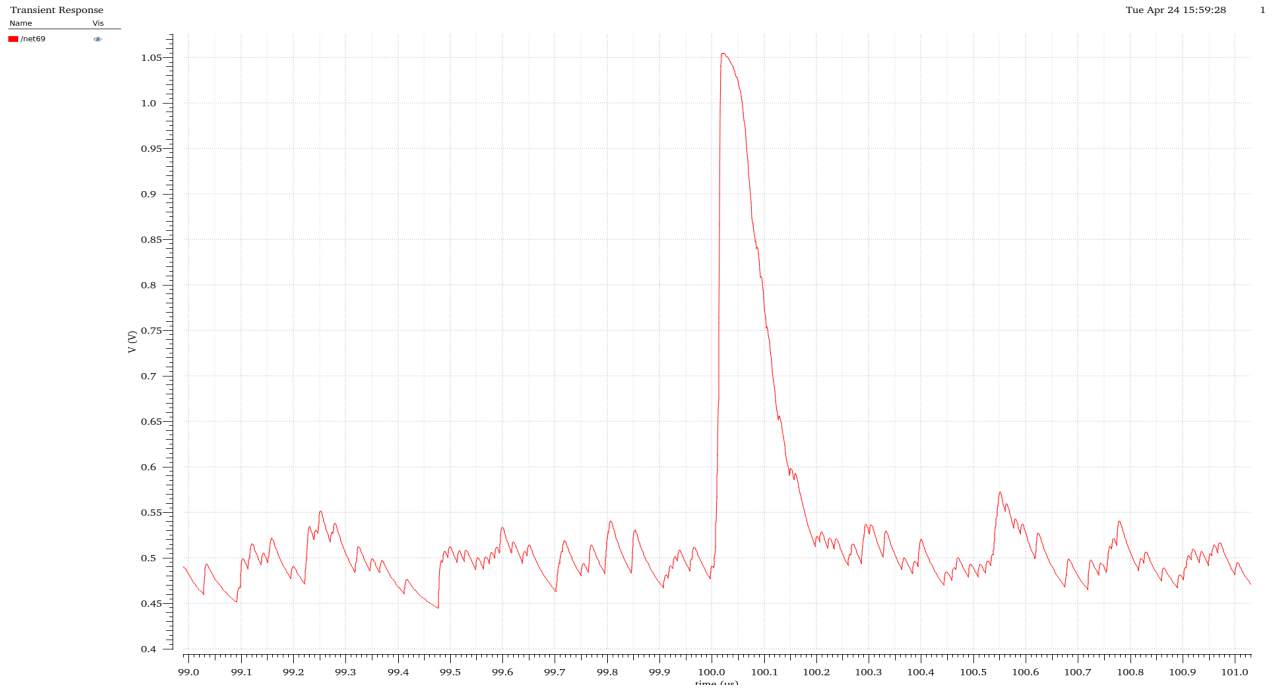






- Is this sufficient?
- How can we improve it?
- Straightforward: increase the ADC resolution
- Ok up to 10 bits (same ADC design)
- For more than 10 bits: self calibration. Complex and more power hungry
- With analog memory: try and re-digitize

Can we use different readout approaches?



- A slow integrator measures the "DC" current to monitor the background
- The signal is time-stamped and a parameter related to its total charge is captured: peak detector, ToT, etc
- Simpler architectures take less power

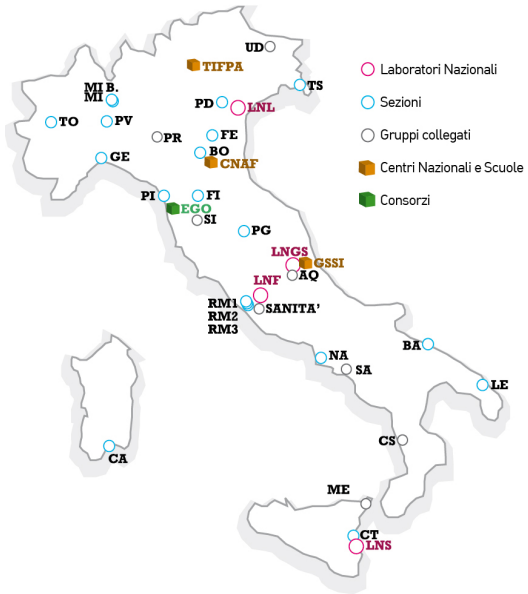
ASIC design process

- Work-out an architecture and define clear specifications: joint work of engineers and physicits
- Start the design: the chip has medium level of complexity. 12 months of two experienced post-docs for the first iteration
- Another year must be considered to arrive at the final integration in the system
- Effective use of CAD tools to minimize number of iteration and achieve full working silicon

The Torino ASIC design group

- The group is part of our electronics lab (14 permanent staff member)
- ASIC, FPGA, PCB design, integration...

- ASIC folks
  - 4 design engineers + 1 test engineer
  - 3 technicians
  - 15 PhD students and post-doc
- Activities
  - Design of mixed-signal front-end ASICs
  - From the idea to the system integration and follow-up
  - In stand-alone or in cooperation with other partners
  - Both R&D and system design

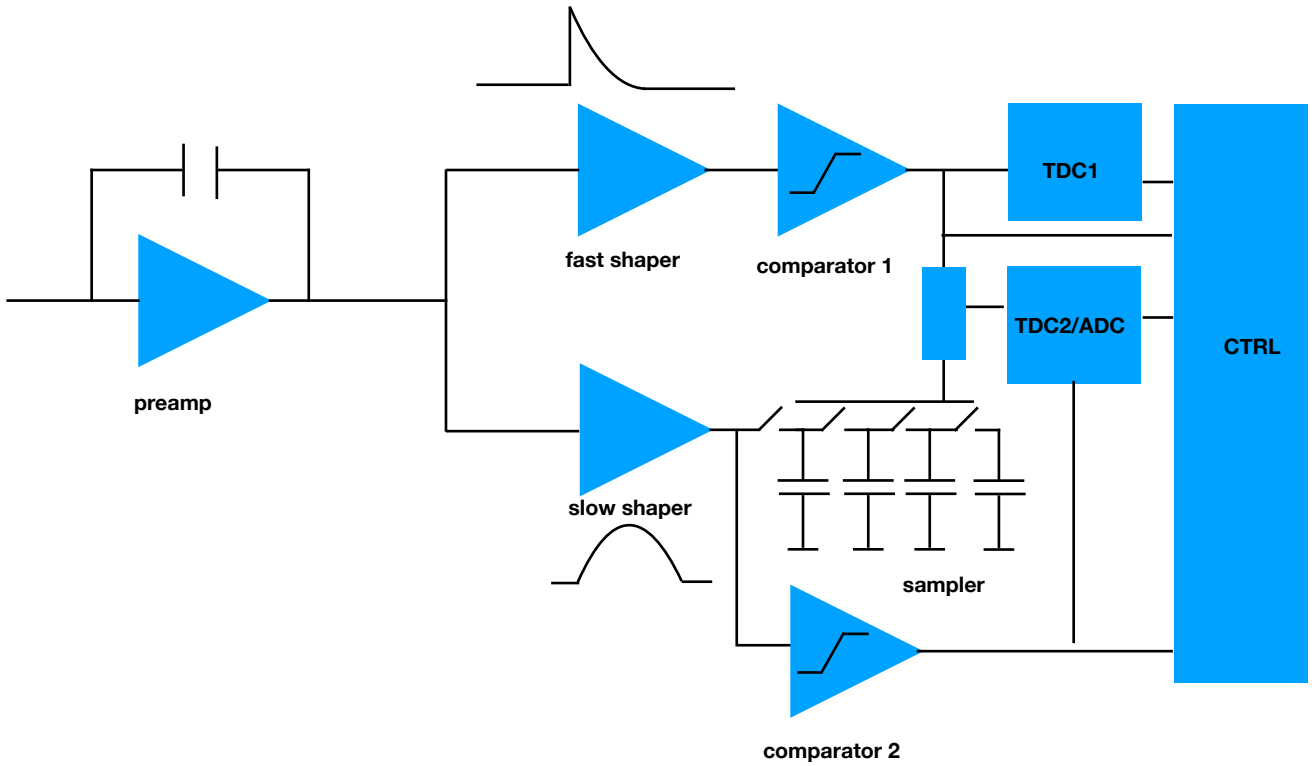


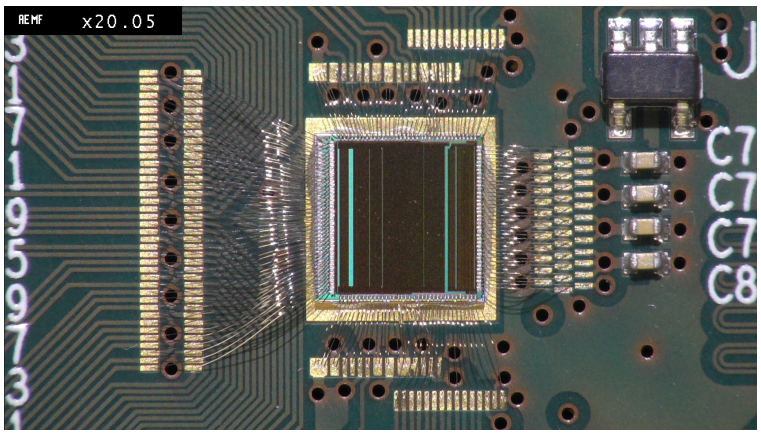
Project overview

- ALICE-ITS
- BESIII
- CHIPIX65
- COMPASS
- CMS-TK
- CMS-ECAL
- DARKSIDE
- FINFET16
- FOOT
- INSIDE
- MOVE-IT
- PANDA
- RD53
- SEED
- SYNCFEL
- TIMESPOT
- UFSD
- TT
- ALICE ZDC
- ASIDI
- AUGER
- CMS-DT
- BELLE II
- DIACELL
- DIESIS
- e-LIBANS
- EEE
- JEM-EUSO
- NA62
- NUMEN
- TOTEM
- TRIMAGE

- A dedicated ASIC could be designed, but dedicate extra resources are needed

A recent design example





- Dual mode: ToT or charge sampling
- Digital peak detector
- Re-use of part of the TDC to implement the ADC

Other recent developments