

ZCU111 RFSoc Characterisation, in the Context of a Cost Effective Microwave Readout System for MKIDs

Colm Bracken^{1,2}, Eoin Baldwin^{1,2}, Gerhard Ulbricht^{1,2}, Mario De Lucia^{1,2},
And Tom Ray^{1,2}

¹Dublin Institute for Advanced Studies, Ireland. ²Trinity College Dublin, Ireland

Abstract

State-of-the-art MKID arrays for optical/near-infrared detection require frequency spacing of ~ 2 MHz, allowing ~ 500 pixels to be read per GHz of RF bandwidth. As such, the Xilinx XCZU28DR RF-SoC chip with its 8 x 4.0 Giga samples per second (GSPS) ADCs could potentially digitise quadrature signals in I and Q from 8,000 MKIDs, albeit limited by the logic resources on the chip. A characterisation of the ZCU111 RF-SoC carrier board is presented in this poster, in the context of an RF-SoC MKID readout. Based on the expected logic resources required by the firmware design described herein, the ZCU111 board will need to be expanded if the full available bandwidth is to be utilised, allowing for real time photon counting for 8 K pixels. A description of how the FMC+ port can transfer the digitised data from all 8 ADCs to a secondary FPGA board, through GTY transceivers is shown. This method of coupling to an external FPGA board, with additional memory (HBM/HMC), will allow 8,000 MKIDs to be read with microsecond time resolution, in a compact, affordable format.

Processing System

Quad-Core
Arm
Cortex-A53

Memory
Subsystem
(DDR4)

System
Functions

DisplayPort
USB 3.0
SATA
PCIe® Gen2
GigE
CAN
SPI
SD/eMMC
NAND

Dual-Core
Arm
Cortex-R5

Platform
& Power
Management

Security

Programmable Logic

DSP

33G Transceivers

Embedded RAM

25G/100G Ethernet

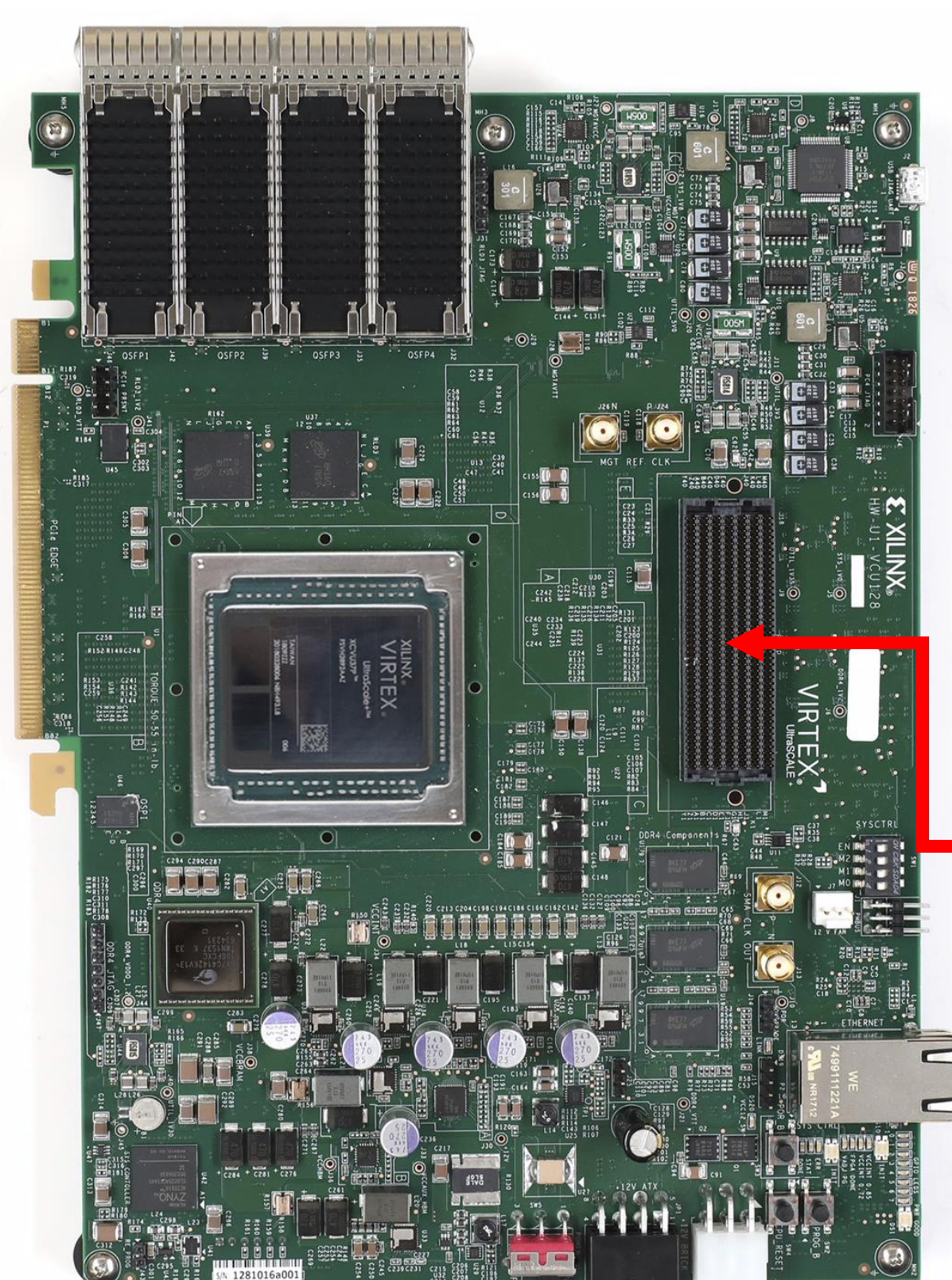
RF-ADCs

SD-FEC

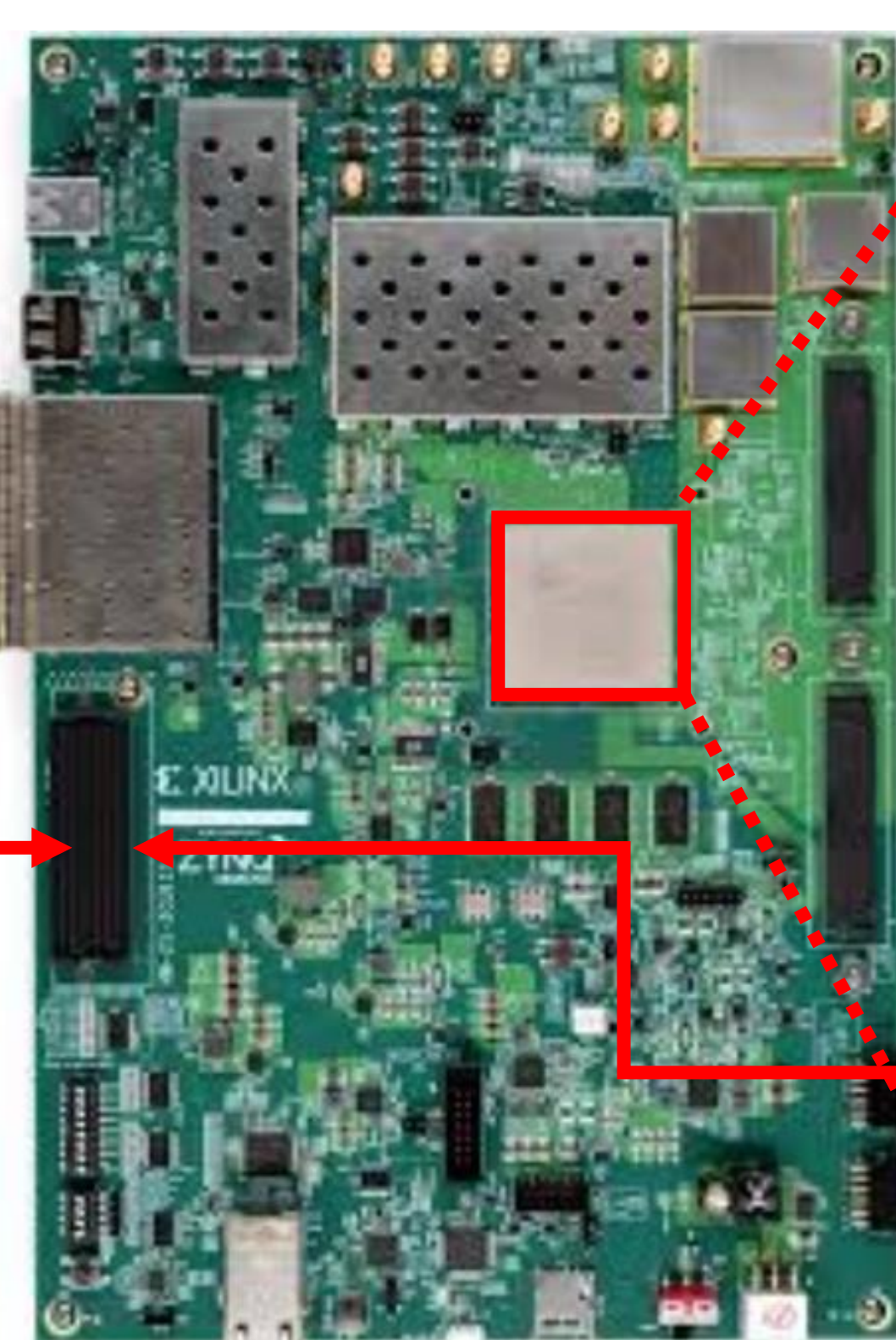
RF-DACs

XCZU28DR RFSoc Chip Architecture

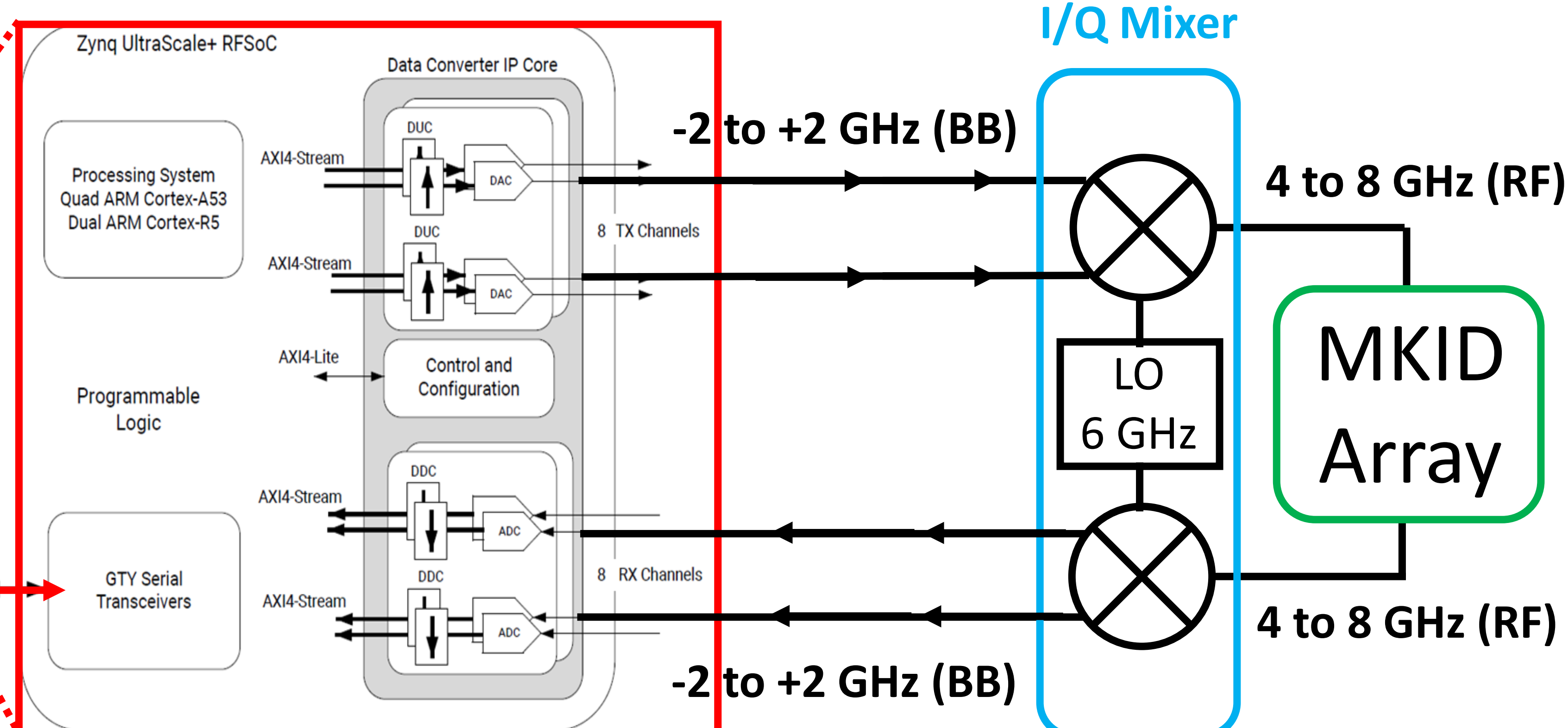
Showing all main chip subsystems [1]



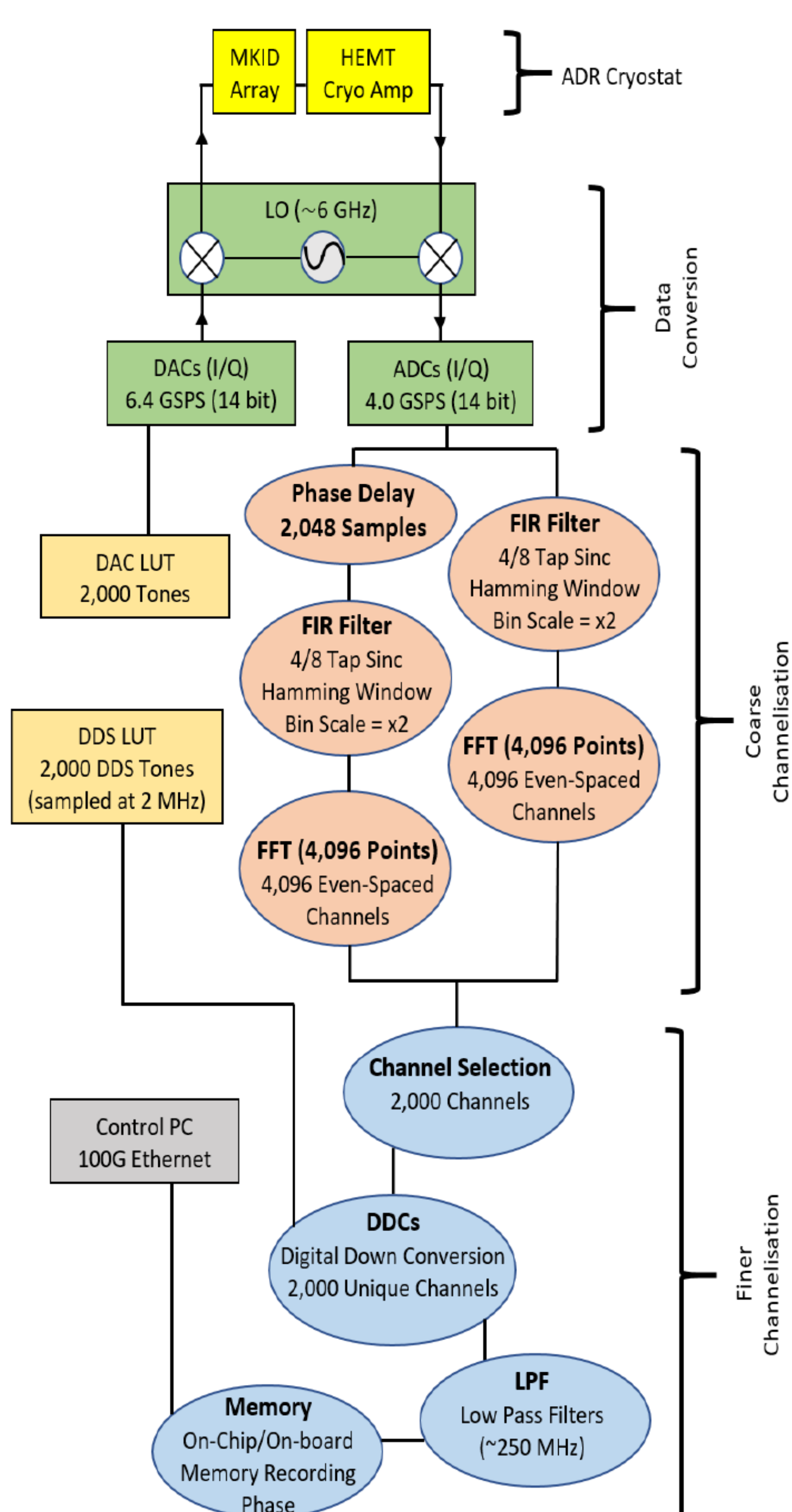
Xilinx VCU128 [3]: Virtex UltraScale+ HBM
ZCU111 FMC+ to VCU128 FMC+



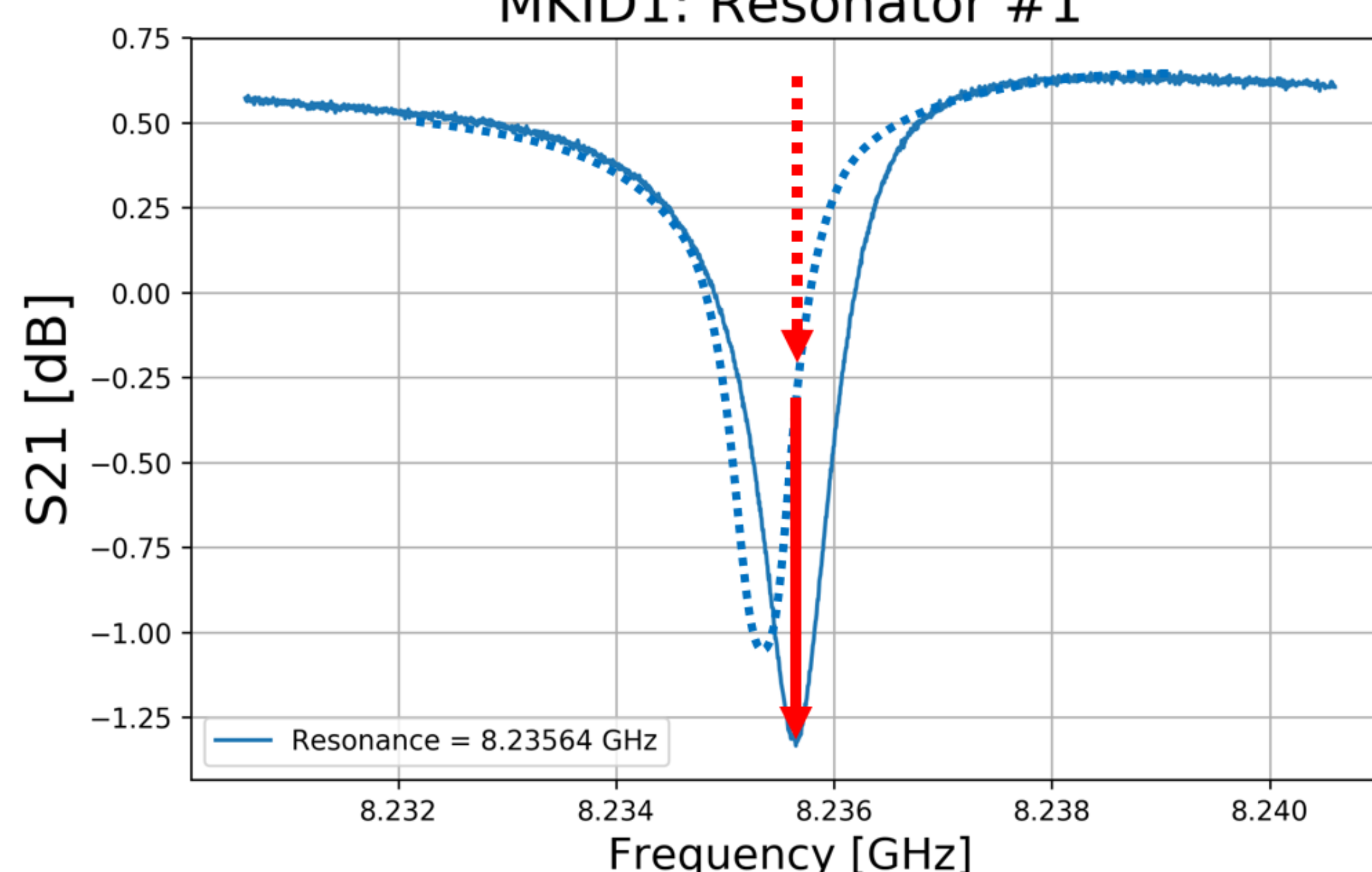
Xilinx ZCU111 [2]: Zynq UltraScale+ RF SoC
16 GTY (32 Tx) on FMC+ export all 8 x ADC data



Each 4 GSPS (12 bit) ADC generates 48 Gbps.
We will clock FMC+ GTY PLL at 12 GHz (24 times ADC reference clock (512 MHz))
2 GTY (4 Tx pins) per ADC [4]

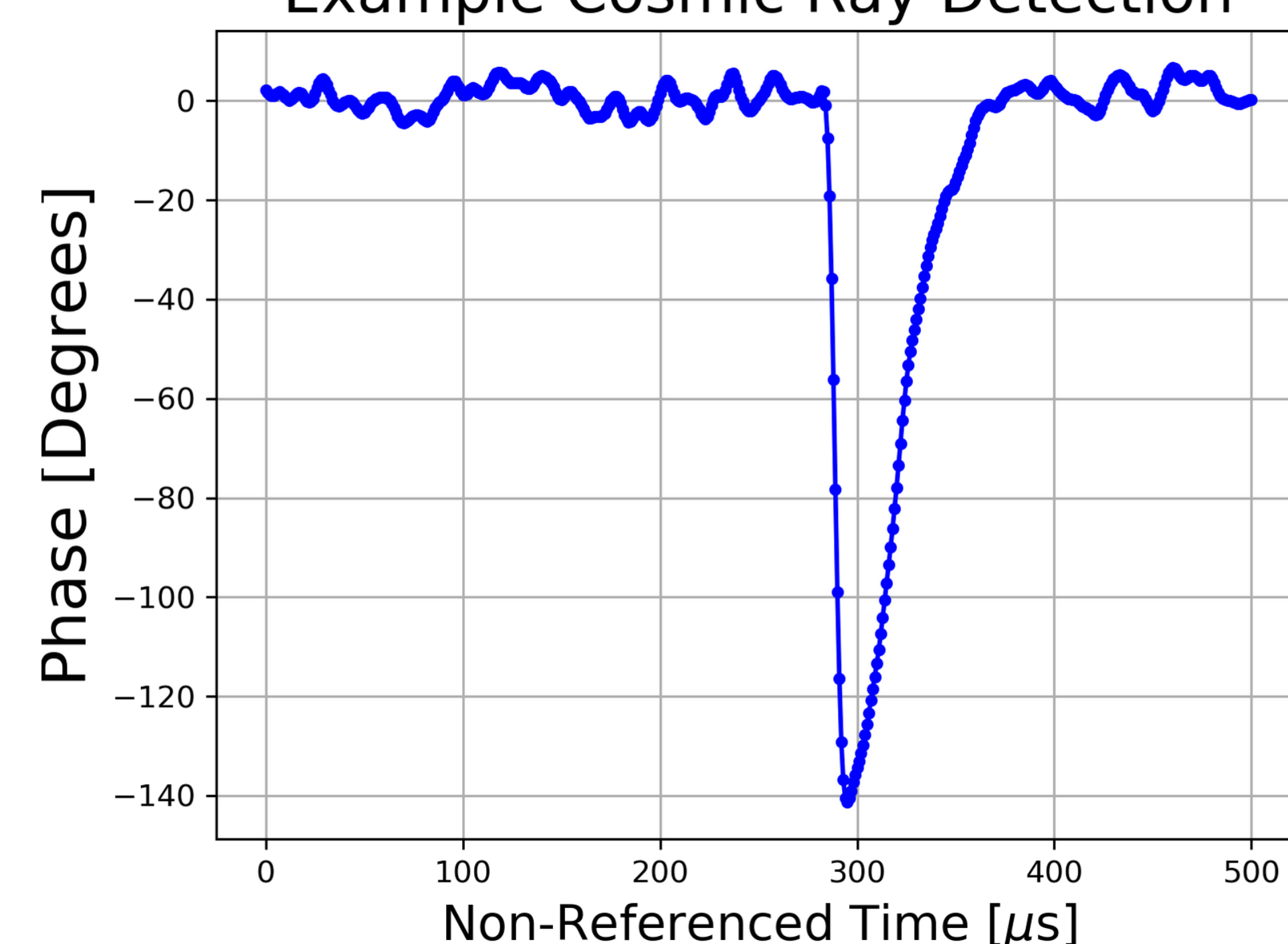


MKID1: Resonator #1



S21 transmission for a prototype AI MKID, fabricated & tested at DIAS/TCD, (blue-solid). Simulated response to photon incident (blue-dotted). Red arrow represents a probe tone.

Example Cosmic Ray Detection



Cosmic ray impact (ROACH 1 [5]), with high-Q resonators on loan to DIAS from Netherlands Institute for Space Research, Utrecht. Credit: P. de Visser, J. Baselmans.

References: [1], [2], [3] Xilinx Inc., '<https://www.xilinx.com/products>'

[4] Xilinx Inc., '*White Paper: UltraScale GTH/GTY Transceivers*'

[5] S. McHugh, et al., '*A readout for large arrays of Microwave Kinetic Inductance Detectors*', arXiv:1203.5861v1 [astro-ph.IM] 27 Mar 2012