Adaptable Firmware for Microwave SQUID Readout on a Commercial Hardware Platform

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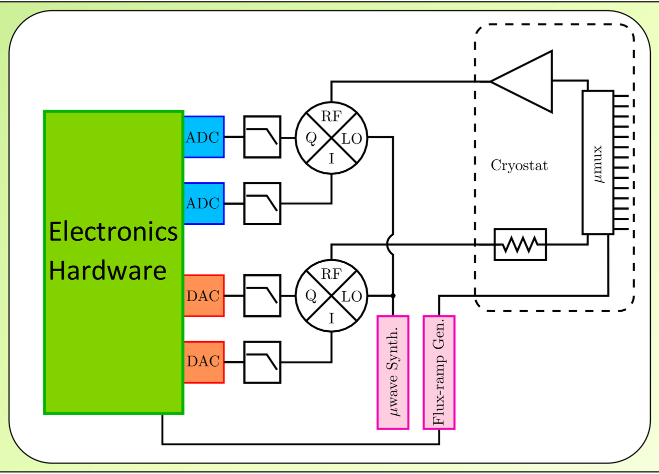
ABSTRACT:

As the size and scale of low temperature detector arrays continues to grow, the demands on the cryogenic multiplexing has dramatically increased. The microwave SQUID multiplexer is meant to address this issue by opening the possibility of multiple gigahertz of readout bandwidth per coax pair. With this readout technique, complexity is moved from the cryogenic stages to the room temperature hardware and digital signal processing firmware. With the variety of microwave SQUID multiplexer designs that are being developed at NIST, the signal processing firmware must have sufficient agility to accommodate different numbers of channels, resonator bandwidths, and resonator spacings. The necessary flexibility is possible with the advent of high-performance ADCs and DACs integrated with field programable gate arrays (FPGAs). Our firmware is implemented on a commercial, off-the-shelf data acquisition platform capable of manipulating up to four gigahertz of bandwidth. Depending on the application, we can modify the channelization module to achieve target resonator bandwidths and spacings. We will discuss the application space of microwave SQUID multiplexers and how that impacts the firmware modules that need to be implemented. This modular firmware architecture for microwave SQUID multiplexers can be ported to a wide variety of Xilinx FPGAs, including the current and future generations of Xilinx's RFSoCs.

Microwave Multiplexing

Microwave multiplexing is finding uses across a wide variety of TES sensor applications from X-ray and gamma ray calorimetry to Cosmic Microwave Background bolometry. This range of applications require over two orders of magnitude of resonator Full Width Half Max (FWHM) designs and accompanying firmware/hardware. The goal of the firmware and associated hardware is to digitize some bandwidth and extract the useful signals out of the band.



Channelization

Channelization is the act of taking the raw ADC bandwidth and segmenting it around each channel of interest. This process makes channelization the most resource intensive task in the firmware. Depending on the number of channels needed and the bandwidths required per channel there are two forms that are considered here:

- Digital Down-Conversion (DDC) with Finite Impulse Response Filter
  - Full ADC bandwidth complex mix
  - FIR Filter to Decimate down to $f_{SUB\_SAMPLING}$
  - Simple duplicative nature when increasing channel counts
- FFT Based Poly-Phase Filter Bank (PFB/FFT)
  - Largest Size of FFT determined by $f_{SUB\_SAMPLING}$
  - Far more resource efficient at higher channel counts
  - Greater out of band suppression than FIR filters

Microwave Mux System Attributes

Below is a description of pertinent variables the govern key design choices of the firmware. The table contains a list of current and future resonator bandwidths along with their associated attributes.

- Three attributes a firmware programmer needs to know about the microwave multiplexer to read the device out:
  - $\Delta f_{SPACING}$: The frequency spacing between adjacent channels, this determines how steep of a filter cutoff is needed
  - $f_{SUB\_SAMPLING}$: The sampling needed after channelization to resolve the flux ramp modulation
  - $N_{CHANNELS}$: The number of channels, can be represented in a per GHz value or number of channels per ADC set
- The below attributes can be calculated based on the device design characteristics and specific application:
  - BW_{FWHM} : Resonators full width half max bandwidth, this sets the scientific sampling rate and channel bandwidth
  - $N_{SPACING}$: Number of bandwidths between adjacent channels, this sets the required frequency for the stop-band
  - N_{FAB}: A generalized additional factor of resonator bandwidths that helps set the number of channels. This integrates all unused bandwidth (between sub-bands, between chips, between digitization bands) into a single, per-channel number.
  - $BW_{DIGITIZATION}$: Typically, the Nyquist sampling rate of the platform or pair of ADCs.

$$\Delta f_{SPACING} = BW_{FWHM} * N_{SPACING}$$

$$N_{CHANNELS} = \frac{BW_{DIGITIZATION}}{BW_{FWHM}(N_{SPACING} + N_{FAB})}$$

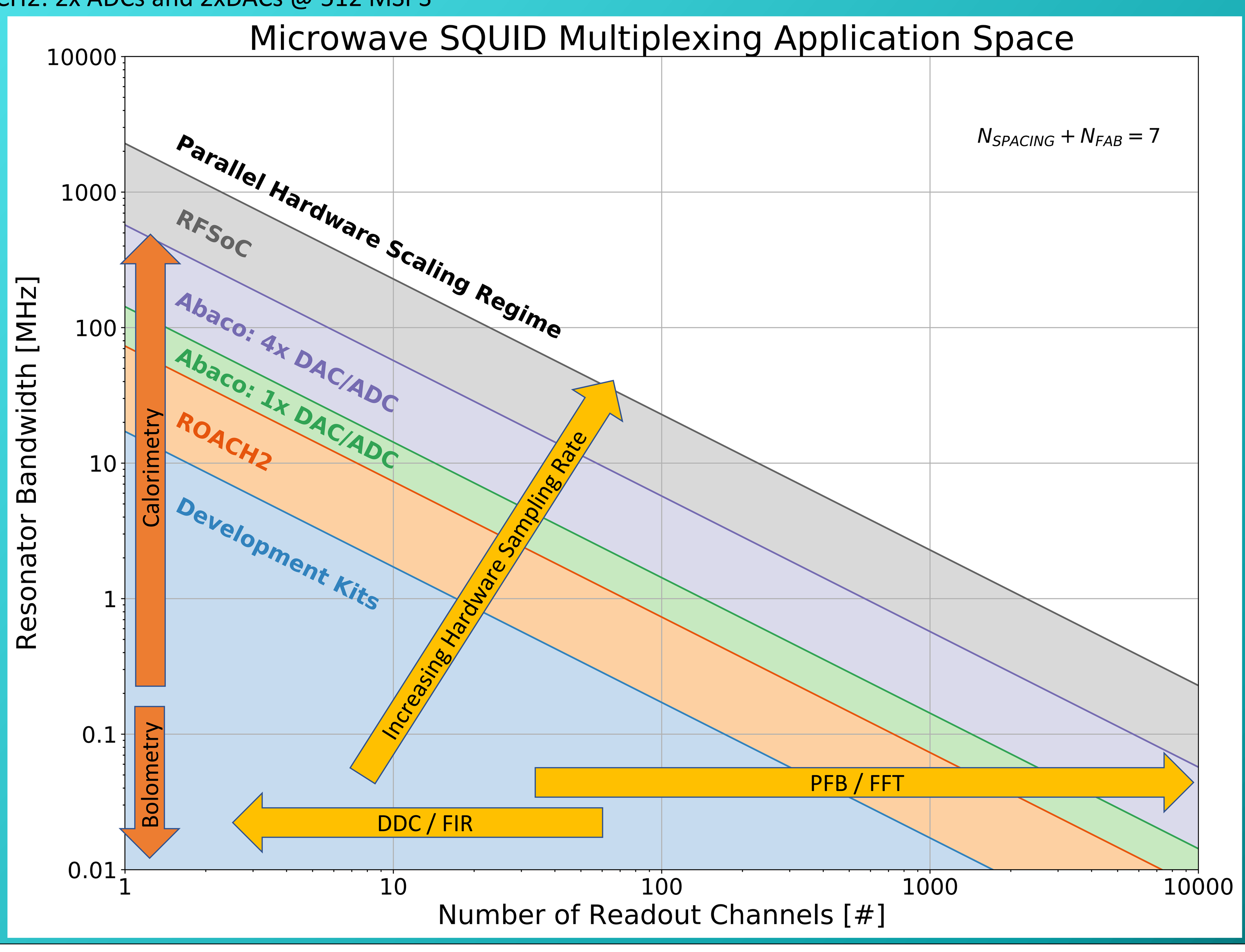
$$f_{SUB\_SAMPLING} \geq 2 * BW_{FWHM}$$

BW_{FWHM} [MHz]	$N_{SPACING}$ [#]	N_{FAB} [#]	$\Delta f_{SPACING}$ [MHz]	$N_{CHANNELS}$ [#/GHz]
60.00	-	-	-	2
8.00	8	1	64.00	16
5.60	6	1	33.60	25
2.00	7	0.8	14.00	64
1.40	6	1	8.40	100
0.86	6	1	5.16	166
0.30	10	3	3.00	256
0.10	18	2	1.80	500

Microwave Multiplexer Application Space

One way to visualize how these attributes affect the firmware design is to plot channel count versus bandwidth. A chart of several hardware platforms' bandwidths, presented as shaded areas, shows the possibilities for readout given a constant $N_{SPACING} + N_{FAB}$ of 7.

- Small Development Boards
  - RED PITAYA: 2x ADCs and 2xDACs @ 125 MSPS
  - XTRX PRO: 2x ADCs and 2xDACs @ 120 MSPS
- Intermediate DSP Boards
  - ROACH2: 2x ADCs and 2xDACs @ 512 MSPS
- Commercial off the Shelf Solutions
  - Abaco (detailed in next column of poster)
- Xilinx RF System on a Chip
  - 8x ADCs @ 5 GSPS
  - 8x DACs @ 10 GSPS



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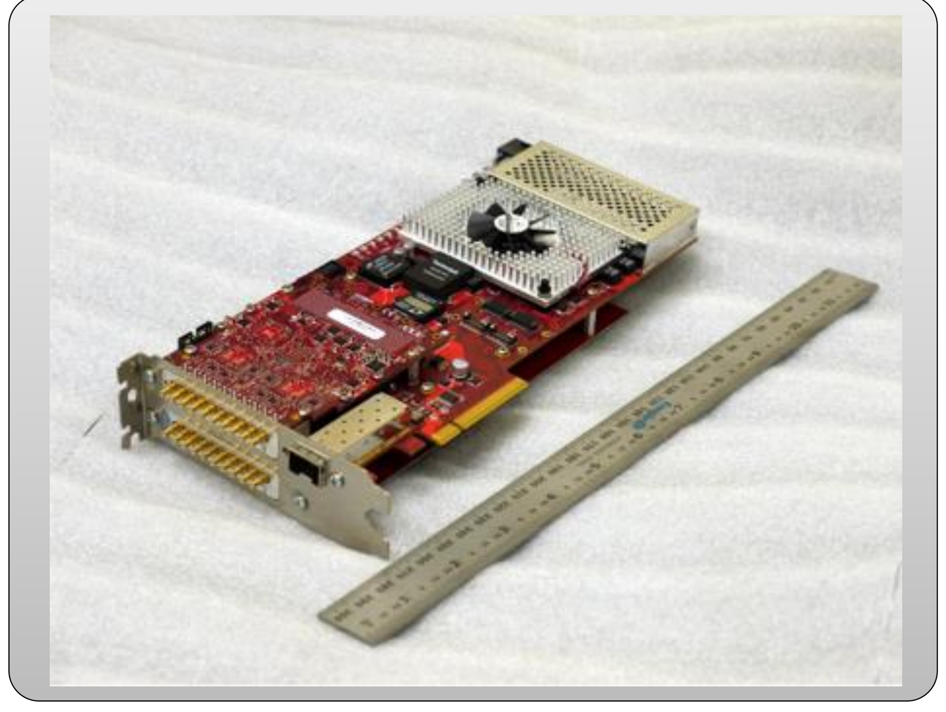


University of Colorado Boulder

NIST

Commercial off the Shelf Platform (COTS): Abaco PCIe Solution

PC821 PCIe FPGA Card

Xilinx Ultrascale KU115

- XCKU115-FLVB1760-1-C
  - 5,520 DSP Slices
  - 75.9Mb Block RAM
  - 1,451k Logic Cells
  - 1,326k Registers
  - 663k Look Up Table

Hardware Interfaces

- 1x FMC HSPC
- 1x FMC High Pin Count
- DDR4 RDIMM
  - 8 GB
  - 72 bit Interface to FPGA
  - 2133 Mb/s
- SFP+ Cage
- 2x Quad Lane FireFly
- PCIe x8 Edge Connection

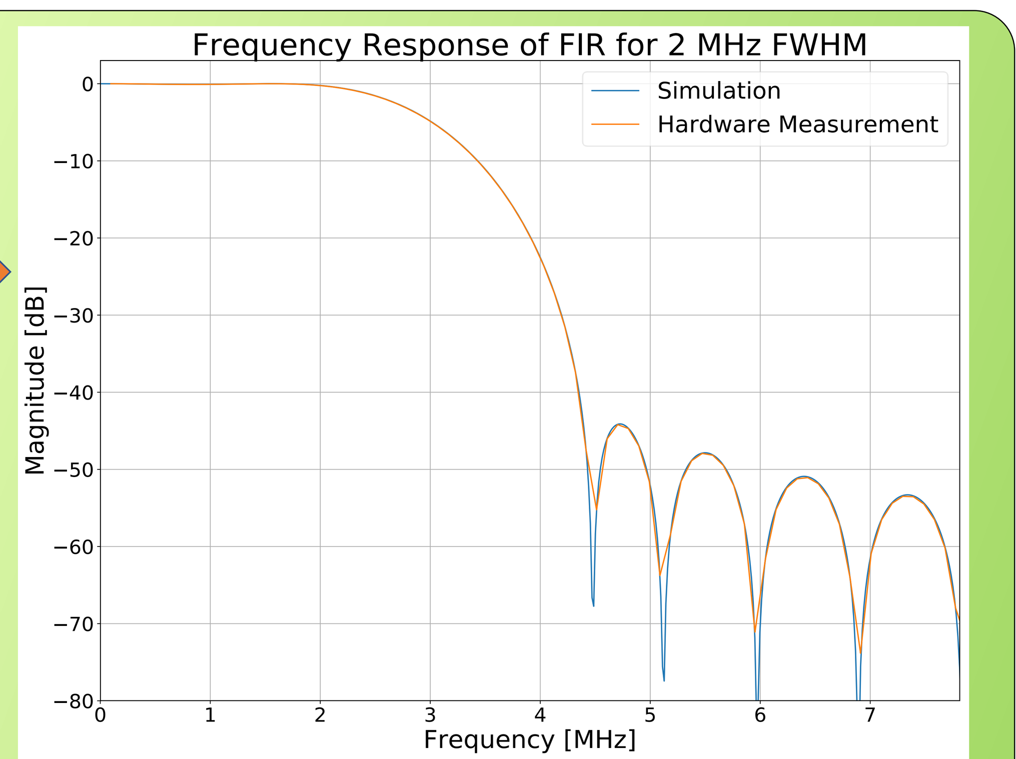
FMC120 Daughter Card (x2)

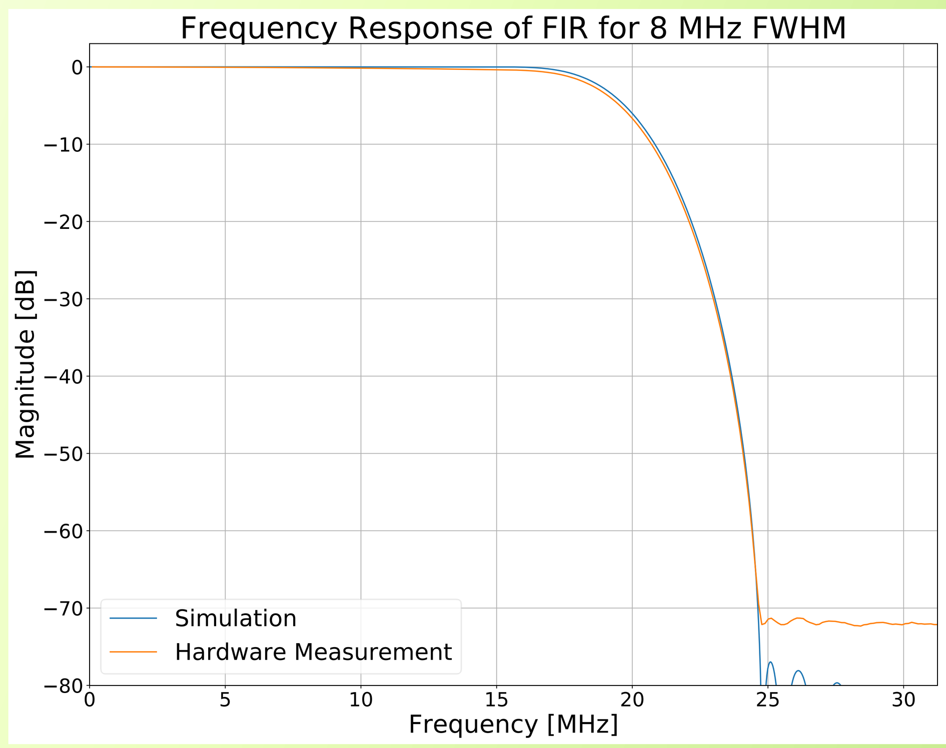
- 4x 16bit ADCs
  - ADS54J60
  - Operating @ 1 GSPS
  - 11.5 Effective Number of Bits
- 4x 16bit DACs
  - DAC39J84
  - Operating @ 2 GSPS

Implementations

64 Channel Abaco Firmware, 2 MHz FWHM

- Two Stage FIR Filter
  - Quarter-Band Filter
  - Fine FIR Filter (Response to the right)
- 15.625 MSPS, complex samples
  - Roll off starts at ~2 MHz
  - Calculated Magnitude of -61dB by center of next channel



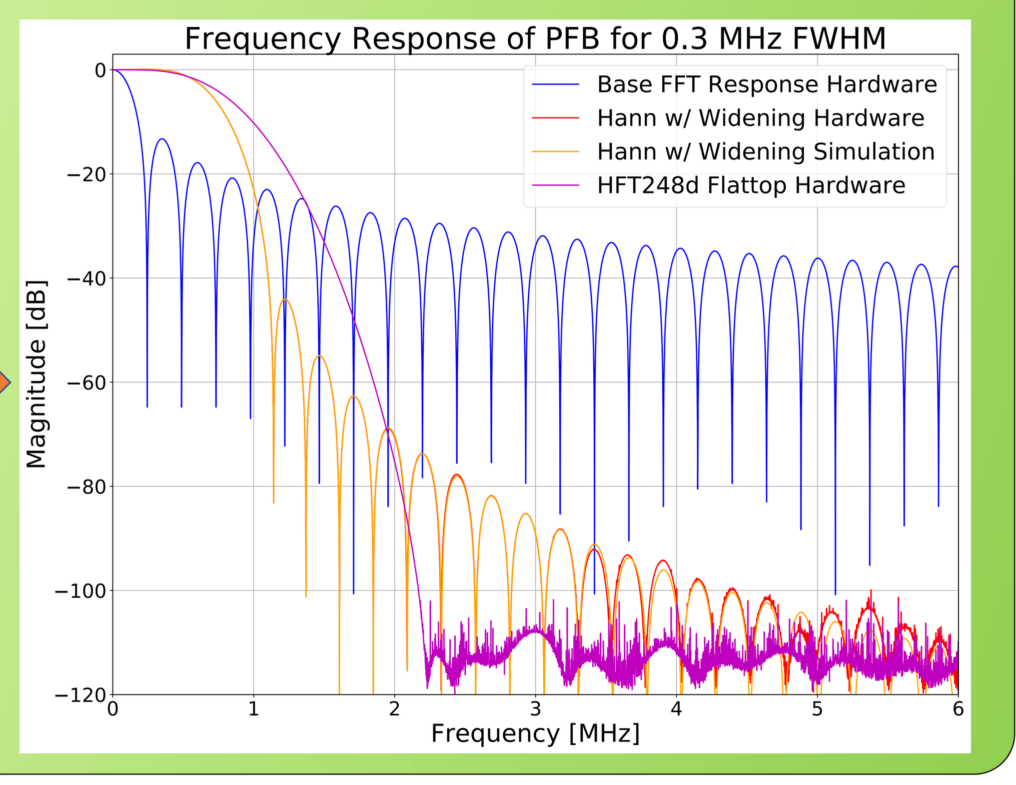


8 Channel Abaco Firmware, 8 MHz FWHM

- Two Stage FIR Filter
  - Quarter-Band Filter
  - Fine FIR Filter (Response to the left)
- 62.5 MSPS, complex samples
  - Roll off starts at ~16 MHz
  - Calculated Magnitude of -96 dB by center of next channel, but due to quantization can only resolve down to -73 dB
- Generated from the 64 Channel firmware in ~4 hours

256 Channel Abaco Firmware, 0.3 MHz FWHM

- PFB Based Channelization
  - 1024 Bin FFT
  - 4 Tap Window and co-add before FFT
  - Window coefficients programable on the fly
- 1.953125 MSPS, per bin, complex samples
  - Achieved by two PFBs in parallel with a half FFT frame offset for the second PFB
  - -85 dB and beyond for a channel 3 MHz away!!



Resource Utilization

For above implementations

% Utilization	64 Channel for 2MHz FWHM	8 Channel for 8 MHz FWHM	256 Channel for 0.3 MHz FWHM
LUT	48.02	21.99	5.44
FF	46.69	17.64	4.71
DSP	54.49	19.13	5.80
BRAM (18k)	58.89	19.63	11.13

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CONCLUSION:

With an ever-changing landscape of ADCs, DACs, and FPGA capabilities it becomes necessary to write firmware that is adaptable across multiple platforms. This puts the requirement on the firmware to be highly parameterizable. When the firmware is coded in a modular fashion, the parameterization becomes easier. We have produced such an adaptable firmware design.

Acknowledgements

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