SDR-based readout electronics for the ECHO experiment

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**ECHO-100k experiment**

The Electron Capture $^{165}$HoM experiment ECHO will investigate the electron neutrino mass with sub-eV$^2$ sensitivity by analyzing the energy spectrum in the electron capture process of $^{165}$Ho.

**ECHO-10k is the second generation targeting a decay rate of 10$^9$ events per second. To achieve this rate at least 10$^6$ sensors are needed. If two sensors are associated with one readout channel this leads to a total of 5000 channels.**

**Frequency division multiplex readout of Metallic Magnetic Calorimeters**

An additional periodic time-dependent flux is introduced to ramp over the SQUID response.

- Sensor sensitivity is independent of individual operation points (flux offsets) of the SQUIDs
- Linearization of multiplier input-to-output signal relation
- Sensor information modulated in signal phase

**Flux ramp modulation for MMCs**

- 400 channels, 4 GHz, 800 sensors in total
- 163Ho e$^+ - 165$Dy + ν + E_r
- Output signal in frequency domain

**Channelizer cascade**

1. **ADC – AD9680**
   - 2 DDC with 400 MHz BW each

2. **Interleaved poly-phase channelizer (PPC)**
   - Overlapping to avoid blind intervals
   - 32 bands, 521 coefficients
   - 6.1 / 10 MHz pass / stop-band
   - >80 dB stop-band attenuation

3. **Digital down conversion (DDC)**
   - 32 Channels TDM, 12 coefficients
   - 1 / 4 MHz pass / stop-band FIR
   - Digital mixer for tuning

4. **Further processing**
   - Flux ramp demodulation

**Scale-up for ECHO**

- 5 ADCs → 2 x 10 chains
- 800 MHz
- 400 MHz
- 16 MHz
- 16 MHz

**Software-defined radio hardware**

- 5x 1 GSample/s 14 Bit I/O ADC (AD9680, 800 MHz BW)
- 3x 1 GSample/s 16 Bit 2 x I/O DAC (AD9144, 2*800 MHz BW)
- 2 x 500 MSample/s DAC for Flux ramp generation
- Integrated PCB based approach for rf-conversion
- Custom FPGA board HiFlex2 with Xilinx Zynq US$+^7$EG

**Prototype measurement with channelization**

**Prototype hardware**

- Four channels $f_{L2} = 4.51$ GHz
- Gradiometric MMC sensor pixels
- Flux ramp modulation 62.5 kHz with HMF2550
- Amplitude modulated data was acquired
- Offline flux ramp demodulation

**Prototype measurement with channelization**

**Measurement type**

- ADC: AD054689, 500 MS/s, 16 Bit
- DAC: DAC38/84, 2.5 GSample/s, 16 Bit
- Xilinx ZCU102 SoC Board
- Custom Hi-Frontend
- Poly-phase channelizer
- Time sequential digital down conversion
- No cross talk visible

**Channelizer for FDM readout**

- FPGA / Channelizer
- Demultiplex
- Amplitude demodulation
- Time domain
- Frequency domain

**Prototype measurement with channelization**

- Ch9
- Ch10
- Ch11
- Ch12
- T = 200 ms
- Frequency [GHz]

**Channelizer Cascade**

1 Band 2x DDC 2 x Digital down conversion (DDC)
128 Bands 2 x Poly-phase channelizer
Further processing

**Channelizer Cascade**

1. 800 MHz
2. 400 MHz
3. –16 MHz
4. –16 MHz

**Channelizer Cascade**

- ADC
- 2 x DDC
- 2 x Digital down conversion (DDC)
- Further processing

**Software-defined radio hardware**

- 15 x for ECHO-100k experiment
- RF frontend and ADC/DAC
- 5x 1 GSample/s 14 Bit I/O ADC (AD9680, 800 MHz BW)
- 3x 1 GSample/s 16 Bit 2 x I/O DAC (AD9144, 2*800 MHz BW)
- 2 x 500 MSample/s DAC for Flux ramp generation
- Integrated PCB based approach for rf-conversion
- Digital electronics
  - Custom FPGA board HiFlex2 with Xilinx Zynq US$+^7$EG
- Small footprint
- 0 MHz DDC mixing frequency
- 2 MHz DDC mixing frequency
- One channel after poly-phase channelizer
- Some channel with digital down-conversion