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Analysing the FPGA processing capacity of the Xilinx ZCU111 RFSoC as a photon counting MKID readout system

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The recently released Xilinx ZCU111 Radio Frequency System-on-Chip (RFSoC) Evaluation Kit is a very promising option for a Microwave Kinetic Inductance Detector (MKID) readout system. It provides FPGA resources of 930,000 system logic cells and 4,272 DSP slices, as well as eight on-chip 14-bit digital-to-analogue converters (DACs) with 6.5 giga-samples per second (GSPS) and eight 12-bit analogue-to-digital converters (ADCs) with 4 GSPS. The on-chip data converters provide ample bandwidth for up to 8,000 MKID resonators with 2 MHz spacing at a 1.0 MHz pixel sampling rate, potentially reducing the per-pixel readout cost to roughly €2 per pixel. However, the channelisation and pulse analysis digital signal processing (DSP) necessary for 8,000 MKID pixels with microsecond sampling is far beyond the capacity of the ZCU111's FPGA. As such, an analysis of the limitations of the ZCU111's FPGA resources is presented, detailing the number of MKID pixels which it should be able to support. We will also discuss options for adding additional FPGAs via the board's mezzanine ports to take full advantage of the large available bandwidth.

Less than 5 years of experience since completion of Ph.D

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Student (Ph.D., M.Sc. or B.Sc.)

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