On the Development of a Reconfigurable Readout for Superconducting Arrays

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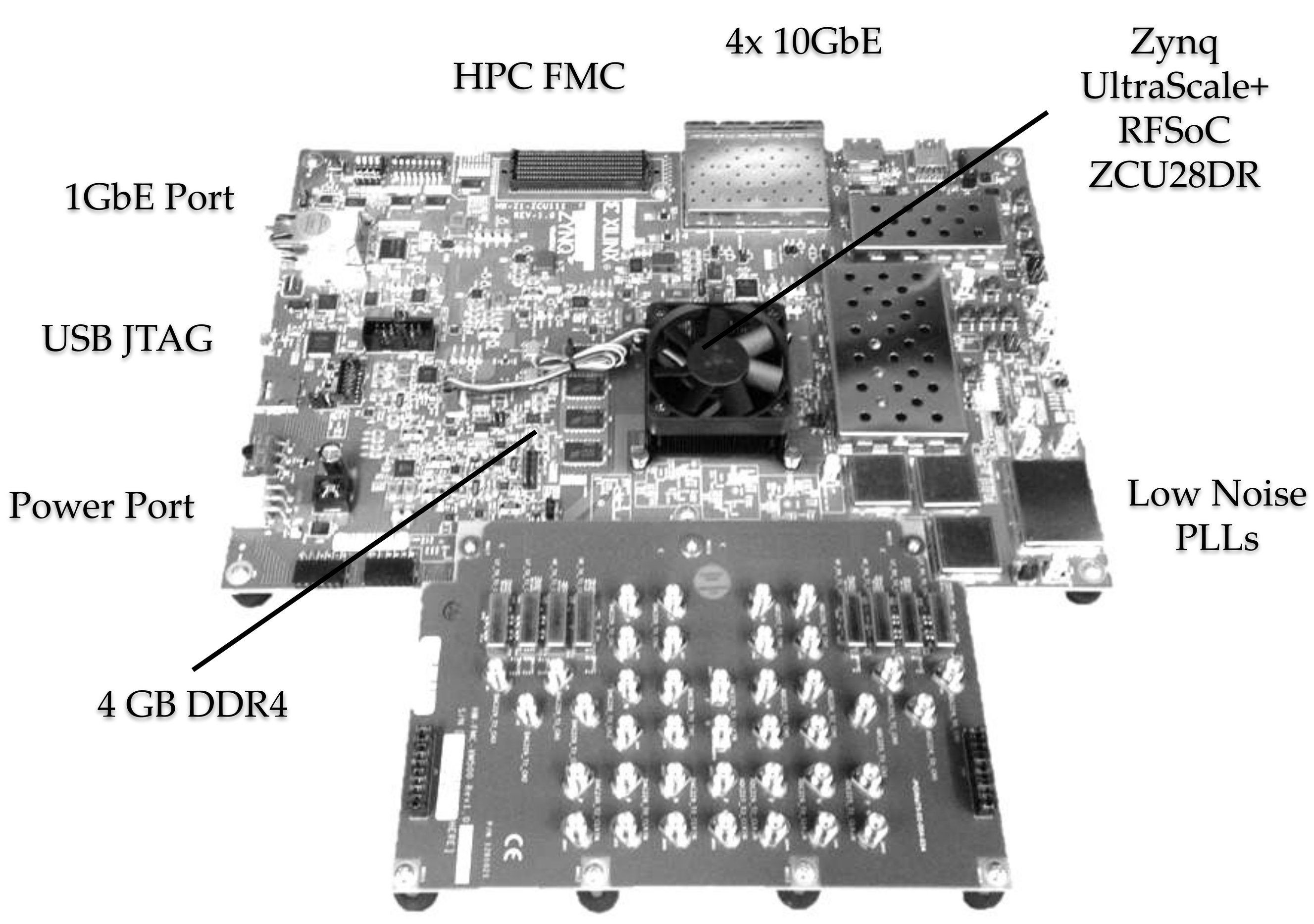
Abstract

The Xilinx Radio Frequency System on a Chip (RFSoC) will set the standard for future astronomical instruments which utilize superconducting arrays of Kinetic Inductance Detectors (**KID**), Transition Edge Sensors (**TES**), and Nanowire Single Photon Detectors (**SNSPD**). The RFSoC combines a fabric of reconfigurable logic, high speed digitizers and a microprocessor all onto a single integrated chip. This dramatically reduces the size, weight and power of the system while simultaneously increasing the instantaneous bandwidth. In parallel the open source community has developed a Python interface for high performance SoCs which has enabled rapid software development. Taking advantage of this product of Moore's law and leveraging previous work we have begun firmware development on the ZCU111 RFSoC evaluation board. We report on the algorithms, firmware and software implementation as well as preliminary measurements with superconducting arrays. We will also discuss the boards' potential as a platform for balloon-borne and space based telescopes.

Xilinx RFSoC ZCU111



Input/Output SMAs to RF digitizers
8x 4 GSPS ADCs
8x 6 GSPS DACs

Specs from references [1][2][3][4]
Size is **less than 1U** (excluding height of fan)

Mass of **less than 1 kg**

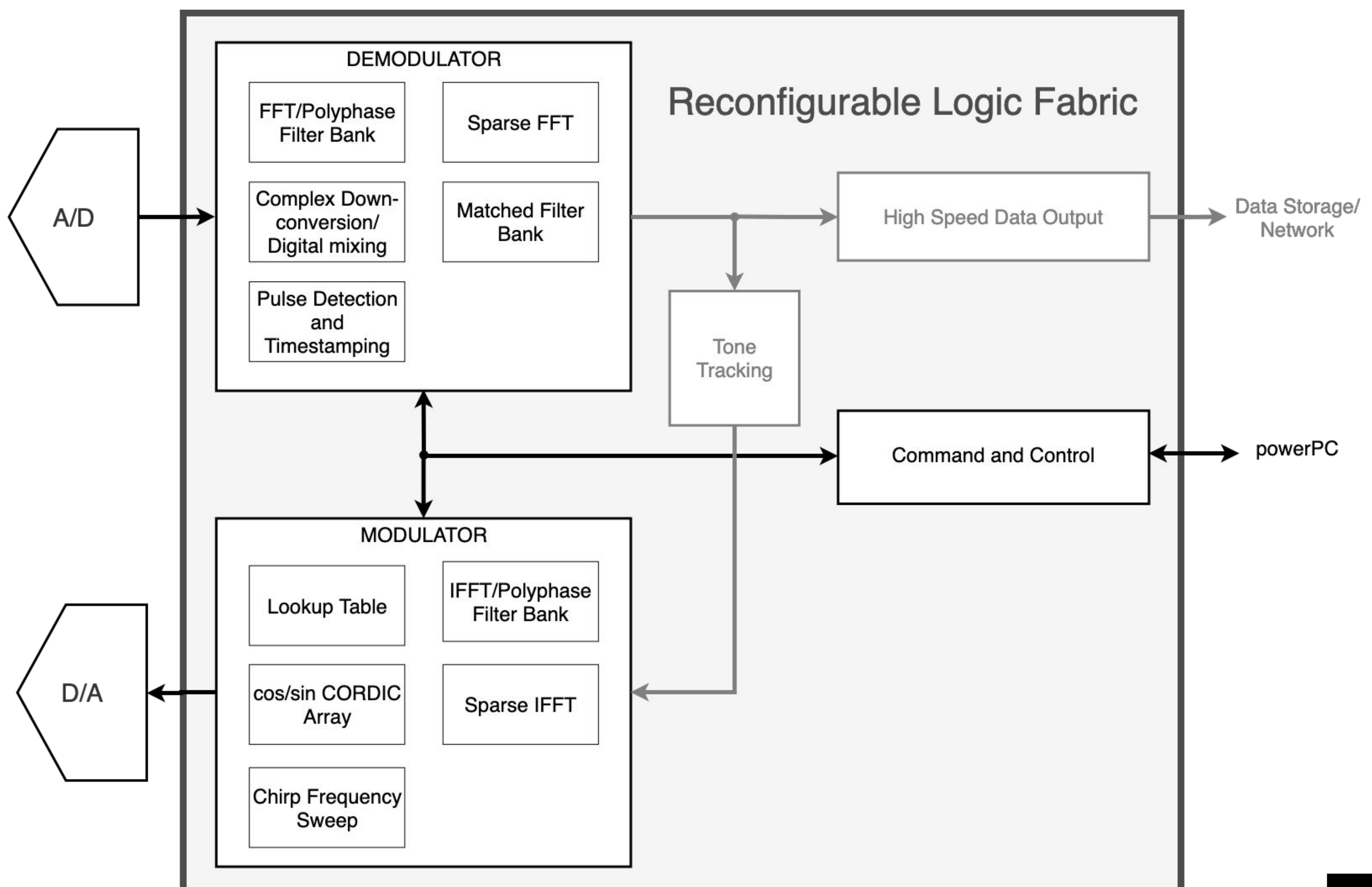
Full power draw **less than 30 W**

16 GHz total ADC bandwidth
24 GHz total DAC bandwidth

DAC/ADC noise spectral density single tone @ fin = 900MHz
less than -150 dBFs/Hz

ARM Cortex A53 64 bit quad-core processor and an ARM Cortex R5 dual-core real time processor

Zynq UltraScale+ ZCU28DR - 930,300 logic slices, 4,272 DSPs, 850,560 CLB flip-flops (**resources available exceed 8x BLAST-TNG firmware utilization requirement**)



Generic firmware architecture with multiple options for tone generation (modulation) and channelization/signal detection (demodulation). Detector data can be collected with the microprocessor on the chip or streamed directly out of the logic fabric. Depending on the requirements and limitations

Towards a General Firmware Architecture

Borrowing from the field of digital communications we can view the readout system architecture analogous to a modem. The modulator provides the bias to the detectors and the signal path between the A/D and D/A can be viewed as a noisy cryogenic communication channel. If there is a change in phase or amplitude caused by optical loading or temperature this will be detected by the demodulator. This analogy can be extended to characterize the channel capacities (or error rates) of different detector multiplexing and methods of modulation. There are many different algorithms and some of the most popular are listed in the above diagram.

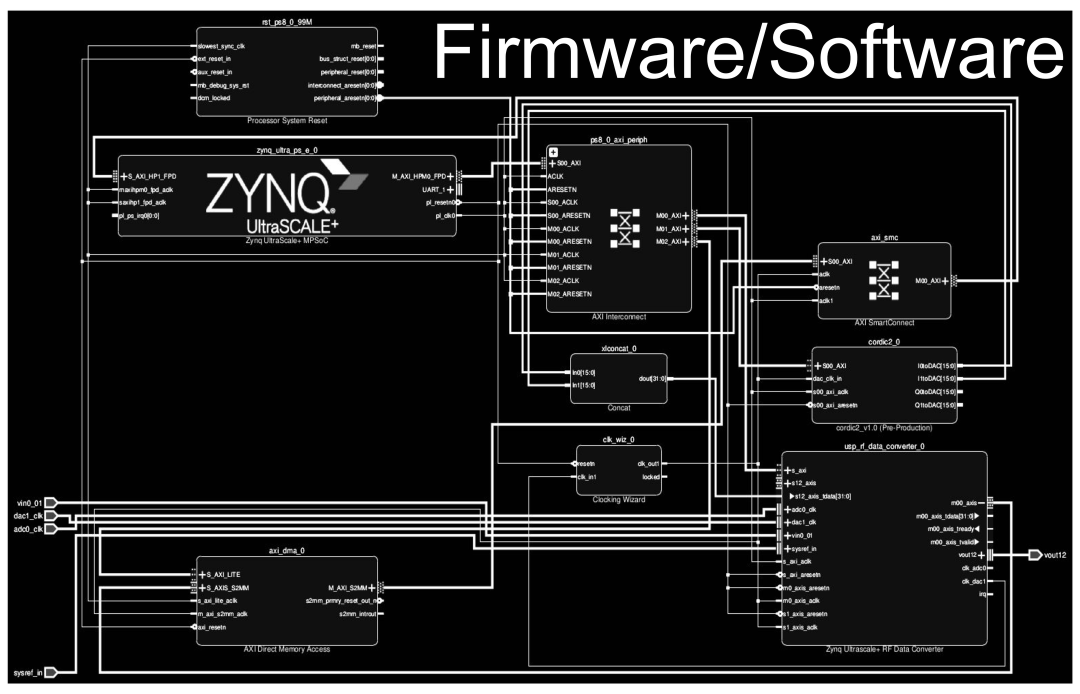
Our groups specific implementation will build upon the open source firmware of **BLAST-TNG**. Originally designed for the ROACH2 and relying heavily on the open source firmware development of CASPER. This firmware has also been used for **Olimpo**, **MUSCAT**, **TolTEC**, and **SuperSpec**. We are working to improve the performance by adding tone tracking capabilities. Tone tracking is a method which can help to increase the dynamic range of the detectors. The products of this work will be used for the future ground based telescope **Ali-CPT** and balloon-borne telescopes **EXCLAIM** , **TIM,** and **BFORE**.

Reconfigurable readout for balloon-borne and space based telescopes

The next generation of balloon-borne and space based telescopes demand an order of magnitude increase in performance over existing systems. An ideal candidate is a fully integrated system like the RFSoC having improved the SWAP&B in every category. Additionally the **DSP firmware can be platform independent** therefore individual modules **TRL can be raised across platforms**.

The Next Generation Balloon-borne Large Aperture Submillimeter Telescope (BLAST-TNG) from the 18-19 Antarctic campaign. BLAST-TNG uses five ROACH2 boards to readout over 2500 lumped element kinetic inductance detectors.

Firmware/Software Implementation



Vivado block diagram of recent general platform work. The above design contains an ADC/DAC pair, microprocessor, custom parallel CORDIC sine wave generator connected to the DAC, and a direct memory access block for capturing ADC data.

After developing firmware modules in **VHDL/Verilog**, **MATLAB-Simulink System Generator**, and simulating with Simulink, **Vivado**, or **GHDL** we import the modules into Vivado for synthesis, elaboration, and implementation. To accelerate this process for future instruments we have been working on a general firmware shell which contains the minimum required modules to run a pipelined(streaming) design to let you **drop in your custom mod or demod block of choice.** Taking advantage of the recent open source Python productivity for the zYNQ (**PYNQ**) we also are developing control software for the general firmware design. We will be uploading this general RFSoC design to github, stay tuned...

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