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Energy consumption, conversion, and transfer in nanometric Field-Effect-Transistors (FET) used in readout electronics at cryogenic temperatures

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For integrated FET based circuitry in close proximity to the front-end detectors or semiconductor or superconducting qubit generating hardware held at cryogenic temperatures, any transfer of heat produced in the FET circuitry alters the performance conditions of the system and results in noise and spurious signals. Therefore, it is of great interest to analyze and experimentally characterize the processes of heat generation at the transistor level, the heat transport mechanisms from the intrinsic active region of the transistor to the interconnection metal lines, the substrate, and finally the entire circuit itself.
We introduce the analysis and experimental results of the energy consumption, the energy transfer mechanisms, and the process of conversion of electrical energy into heat. The different heat transfer mechanisms that consider the contributions of phonons and electrons, respectively, are modeled as a function of the FET technology parameters including gate oxide thickness, bulk and source/drain doping, and the device geometry and structure. This model serves the purpose of calculating the intrinsic device temperature, the amount of self-heating, and the coupled electro-thermal transport effects at sub-Kelvin temperatures.
We prove that as the temperature is reduced down to the sub-Kelvin regime, more than 70% of the heat in the transistor is transferred by electrons rather than phonons, and that such a heat transfer is a function of the gate oxide thickness, as well as the bulk and source/drain doping levels. The characterization and modeling of the thermal behavior and its coupling to the electrical performance is crucial in determining the electrical-thermal cross coupling. FETs fabricated in 65nm and 14nm CMOS technologies are characterized from room temperature down to 250 mK.

Less than 5 years of experience since completion of Ph.D

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Student (Ph.D., M.Sc. or B.Sc.)

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Primary authors: Mr LÓPEZ-LÓPEZ, Omar (National Institute of Astrophysics, Optics, and Electronics (INAOE)); Mr MARTÍNEZ, Ismael (1National Institute of Astrophysics, Optics, and Electronics (INAOE)); Mr CABRERA, Alfonso (National Institute of Astrophysics, Optics, and Electronics (INAOE)); Dr GUTIÉRREZ-D., Edmundo A. (1National Institute of Astrophysics, Optics, and Electronics (INAOE)); Dr FERRUSCA, Daniel (National Institute of Astrophysics, Optics, and Electronics (INAOE)); Dr DURINI, Daniel (National Institute of Astrophysics, Optics, and Electronics (INAOE)); Dr DE LA HIDALGA-WADE, Javier (National Institute of Astrophysics, Optics, and Electronics (INAOE)); Dr VELAZQUEZ, Miguel (National Institute of Astrophysics, Optics, and Electronics (INAOE)); Dr QUIROGA, Ivan (National Institute of Astrophysics, Optics, and Electronics (INAOE)); Dr KRUTH, Andre (Central Institute of Engineering, Electronics and Analytics ZEA-2 – Electronic Systems, Forschungszentrum

Jülich GmbH); Dr DEGENHARDT, Carsten (Central Institute of Engineering, Electronics and Analytics ZEA-2 – Electronic Systems, Forschungszentrum Jülich GmbH); Mr ARTANOV, Anton (Central Institute of Engineering, Electronics and Analytics ZEA-2 – Electronic Systems, Forschungszentrum Jülich GmbH); Dr VAN WAASEN, Stefan (Central Institute of Engineering, Electronics and Analytics ZEA-2 – Electronic Systems, Forschungszentrum Jülich GmbH)

Presenter: Mr CABRERA, Alfonso (National Institute of Astrophysics, Optics, and Electronics (INAOE))

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